MURI 01: Effects of High Power Microwaves and Chaos in 21st Century Analog & Digital Electronics* (www.ireap.umd.edu/MURI-2001))

Overview of Research Progress

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Boise State Univ.: R.J. Baker, W.B. Knowlton

Presented at the MURI 01 Final Review

July 14, 200, Albuquerque, NM

*(Administered by AFOSR)

MURI 01 Final Review

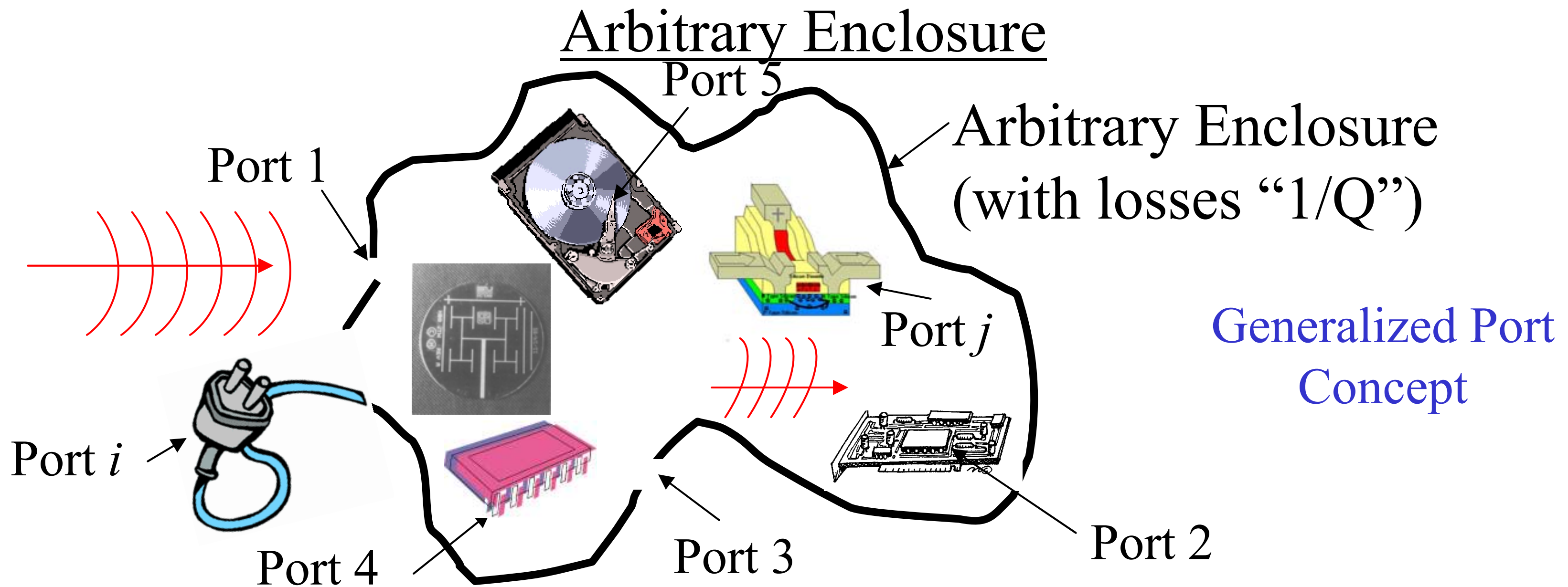
Effects of HPM and Chaos on Electronics

Three Interrelated Parts of the Study

- **A**. Statistical prediction of microwave coupling to electronics inside enclosures
- **B.** Electronics vulnerabilities (upset and degradation)
- **C.** Microwave Detection and Mitigation

A. Statistical Prediction of Microwave Coupling

A1. Random Coupling Model: Induced Field Distributions for an Arbitrary Enclosure



Generalized Port Concept

What minimum information do we need to predict the range of voltages on port j because of 1 Watt injected through port i?

Minimum Information:

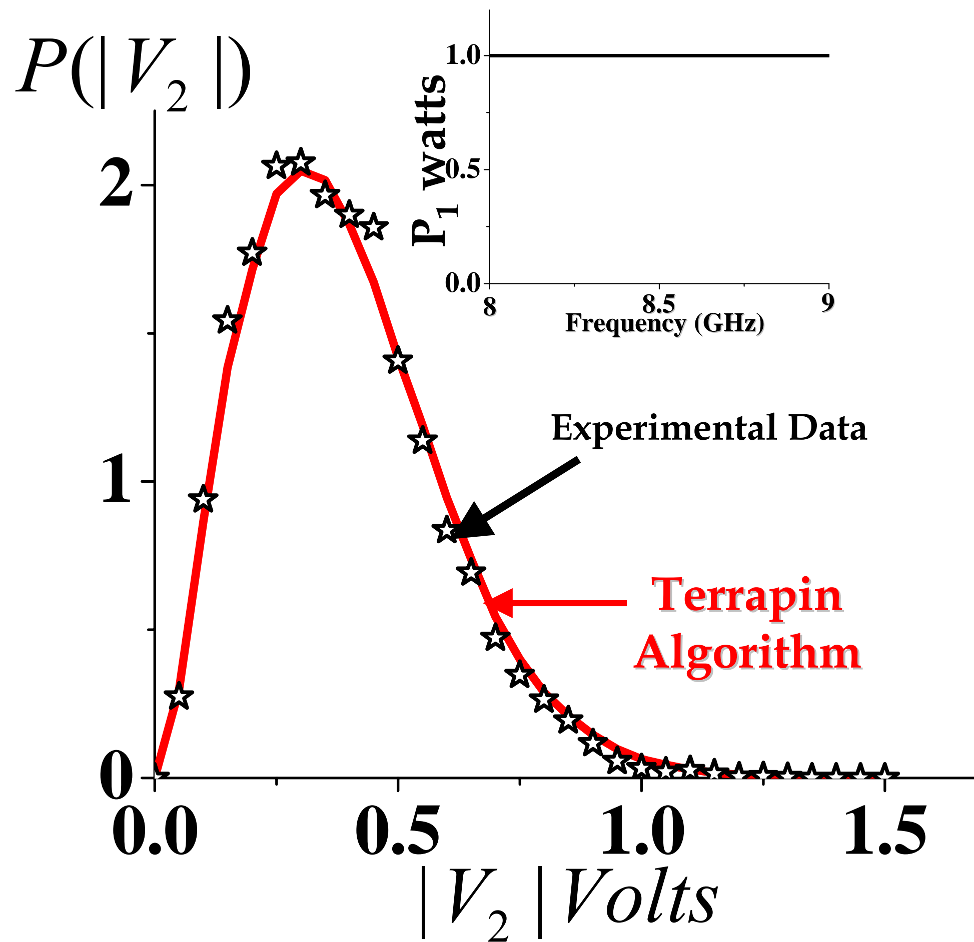
Frequency, Volume
Losses
Radiation impedance of the ports

Determine the shape and scales of the Z_{Cavity} and Field PDFs

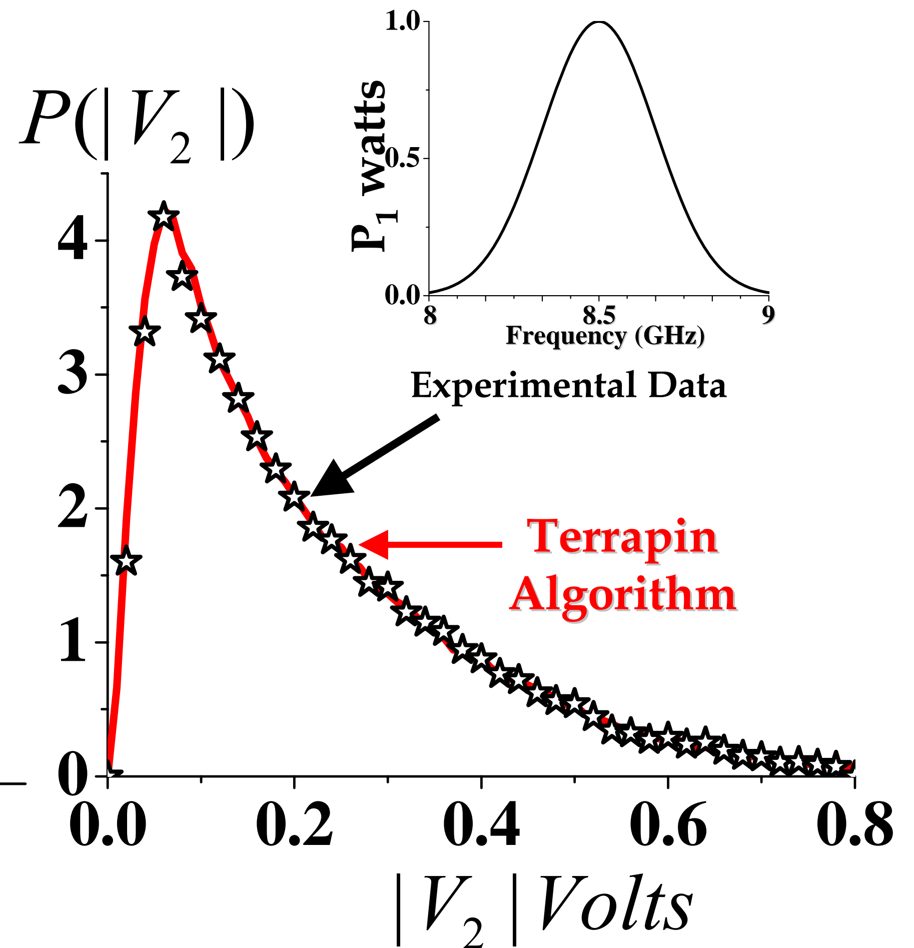
A. Statistical Prediction of Microwave Coupling

A2. Experimental Study: PDF of induced voltages on port 2 of computer-box for different power profiles radiated from Port 1

Flat power-profile radiated from port 1



Gaussian-shaped power-profile radiated from port 1



A. Wave Chaos : SUMMARY

- A random coupling model has been developed and verified through:
  - random matrix theory
  - HFSS simulations
  - Experiments (1-port, 2-port, 2D, 3D)

- Time Domain analysis of Pulsed Signals
  - Random Coupling Model extended into the time domain
  - Experimental verification in progress

- Generalize to systems consisting of circuits and fields

B. Electronics Vulnerability

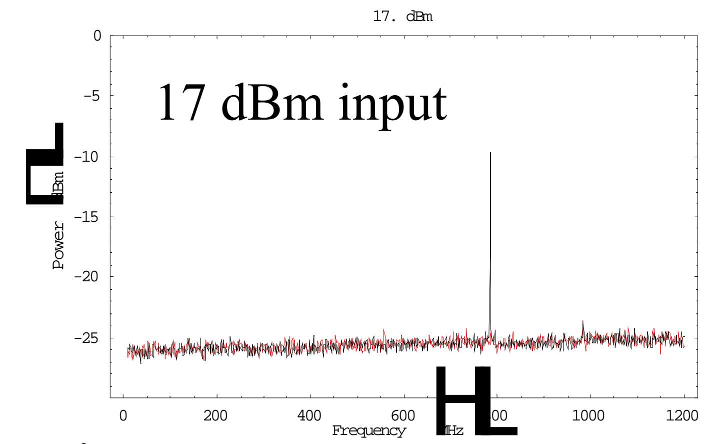
B1. Electronics Vulnerability: Circuit Chaos

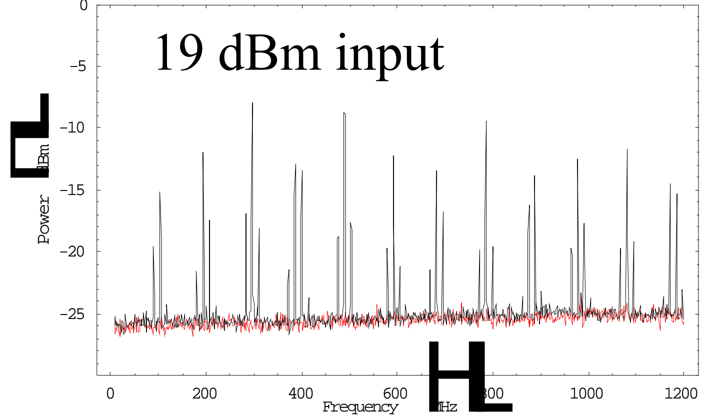
- Basic investigation of nonlinearity and chaos from the p/n junction:
  - Role of time scales – reverse recovery time
  - Distributed systems
  - Experiments (lumped, distributed)

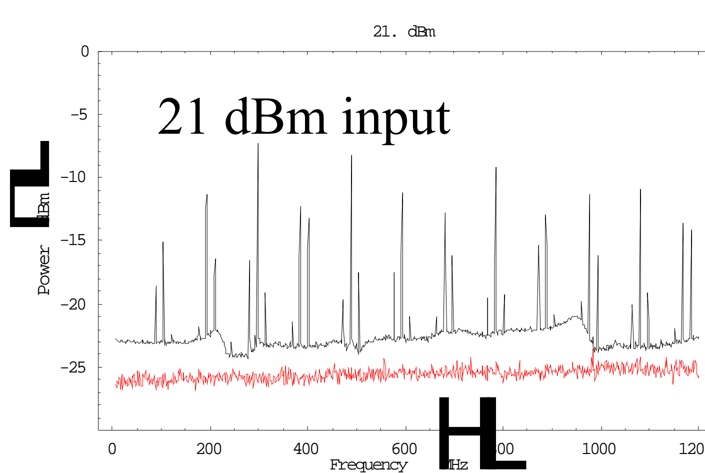
- New modes of circuit disruption identified
  - Electrostatic Discharge Circuits
  - Model + Experiment in agreement for GHz-scale chaos

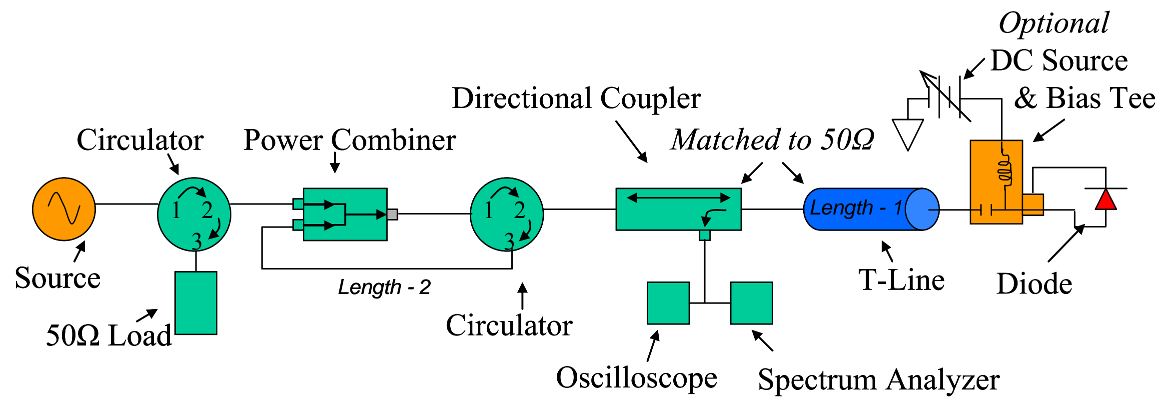
- New opportunities for circuit disruption through p/n junction

Distributed Transmission Line Diode Chaos at 785 MHz









NTE519

785 MHz

T ~ 3.5 ns

DC Bias=6.5 Volts

http://arxiv.org/abs/nlin.cd/0605037

B. Electronics Vulnerability

B2. RF Upset & Nonlinear Effects in Electronics

Device Level: The response of nonlinear junctions (e.g. ESD diodes) to microwave pulses has been studied and characterized in terms of physical and electrical parameters.

Circuit Level: The most probable upset mechanisms have been identified and clearly attributed to effects at the device level.

Systems Level: How circuit function and hierarchy determines the distribution of parasitic resonances and consequently susceptibility in electronic systems has been demonstrated.

•**Modeling:** A generalized circuit susceptibility model that is based on basic, scalable semiconductor parameters has been developed and successfully benchmarked against experiment

B. Electronics Vulnerability

B3. Modeling Effects on Semiconductor Devices, Gates & Interconnects

- Developed Semiconductor simulation tool that models breakdown inside MOS transistors

  -Shows location of oxide and avalanche breakdown

  - Predict the effect of EM radiation on devices not yet built.

  - In contrast to circuit simulator (SPICE), device simulator probes inside transistor to tell exactly where damage occurs.

- Developed Electromagnetic Simulator for Transmission Lines and other Passive Structures on Integrated Circuits
  - Shows precisely where loses occur, and the effects of intrinsic unintentional IC coupling network
  - Extracted modes of propagation in MSIM structures and how they depend on semiconductor doping and geometry:
- Developed a Random Impulse Response Method for Characterizing EM Effects for On-Chip Interconnects.
  - Method uses a coupled time and space domain impulse response (Green’s Function) approach to fully characterize a chip.
  - Once chip is characterized, its response to any EM input can be predicted, the EM input can be random or deterministic.

B. Electronics Vulnerability

B4. MOSFET Reliability and Lifetime Studies

(Boise State University)

- **Goal**: Determine gate dielectric/oxide (SiO_2) degradation mechanisms by EM radiation in MOSFETs & effects on simple IC building blocks.
- **Accomplishments**:
  - Developed two reliability test and measurement techniques
  - Developed EM noise model for device lifetime
  - *Multiple devices analyzed:* SiO_2 (3.2 nm, 2 nm) and HfO_2
  - *Multiple circuits analyzed:* inverter; T, NAND & NOR gates
  - Developed energy band diagram simulation software for multi-gate dielectric stacks

C. Microwave Detection and Mitigation
C1. On-Chip RF Detectors

Work done:

- designed and fabricated on-chip RF pulse power detectors, 3 kinds:
  - FIB Schottky diodes, modified CMOS, MOSFET power detector
- tested and evaluated detectors to determine best performance
  (dynamic range 36dB, sensitivity (1GHz) -21dBm, pulse rise time 56nsec)
  - measured RF incident on chip
  - measured RF incident on circuit board with chip

Future & on-going work:

- fabricate chips with detectors and built in signal processing,
- harvesting of RF power for RFID tags, e.g. with sensors

C. Microwave Detection & Mitigation

C2.System Level RF Effects Mitigation

- External Vulnerability (how easily outside EMI gets in)
  - DUT: Test chip fabricated in AMI's 0.5µm process
  - Comparison of vulnerability: DUT's clock/data inputs
- Internal Vulnerability (how easily inside EMI affects state)
  - Predictive 45nm BSIM4 models integrated w/ Spectre
  - Simulations for Drowsy & DR-Gated-GND SRAM cells
- Mitigation
  - Robust computer architecture (TERPS), which can compensate for detected HPM attack, implemented & prototype chipset fabricated
  - System verification

C. Microwave Detection and Mitigation

EM Noise Mitigation in Cavities and on Circuit Boards

- Reduction of coupling between cavities using electromagnetic band gap structures
- Using lossy material coating to reduce aperture radiation
- Reducing noise in printed circuit boards using electromagnetic band gap structures

Students and Publications

•University of Maryland

20 Graduate Students supported by MURI 01 with 16 Ph. D.s granted or expected
2005: X.Zheng, L.Li, X. Wu
2006: M. Kermani, S.Hemmady, T. Firestone, W. Jeon, Z. Dilli, J. Qin, S. Shaparina
2007: K. Kim, C. Dirik, J. Hart, B. Mahajer-Iravani

12 Undergraduate Research Projects

20 MURI-supported PAPERS in refereeed journals

13 MURI-supported PAPERS in conference proceedings

PATENT: "RF Sense and Protect on-Chip Circuit"

INTERACTIONS: DoD Chaos group, NRL, AFRL, ARL, DIA, NATO-GENEC, DTRA, DEPS, Philips Semiconductor, Jaycor, SAIC

•Boise State

- Over 20 MURI supported graduate and undergraduate students
- 15 MURI supported journal & conference publications
- INTERACTIONS: Micron Technology, SEMANTECH, Motorola, Cypress Semiconductor

A. Statistical Prediction of Microwave Coupling to Electronics inside Enclosures

8:20 a.m. E. Ott, T.M. Antonsen, Jr., J. Hart, X. Zheng, S. Hemmady, S.M. Anlage

"Statistics of E.M. Waves in Complex Enclosures"

8:50 a.m. S. Hemmady, X. Zheng, T. M. Antonsen Jr., E. Ott, S.M. Anlage,

"Prediction & Measurement of Induced Voltage & Current Distributions Inside Complicated Enclosures Using Wave Chaos"

B. Electronics Vulnerability (Upset & Degradation)

9:15 a.m. S.M. Anlage, V. Demergis, A. Glasser, M. Miller, T.M. Antonsen, Jr., E. Ott,
"Delayed Feedback and GHz-Scale Chaos on the Driven Diode-Terminated Transmission Line"

9:40 a.m. J. Rodgers, T. Firestone, V.L. Granatstein, S.M. Anlage, R.M. de Moraes,
"Diffusion Model of Nonlin. HPM Effects in Advanced Electronics"

10:05 ***BREAK***

B. Electronics Vulnerability (Upset & Degradation) *continued*

10:15 a.m. N. Goldsman , Zeynep Dilli,

"A Time-dependent Green's Function Method for Modeling Interference Effects in Integrated Circuits"

10:40 a.m. R.G. Southwick III, W.B. Knowlton and R.J. Baker

"Degradation in Gate Dielectrics and the Effects on Simple Integrated Circuit Building Blocks (SICBBs)"

C. Microwave Detection and Mitigation

11:10a.m. W. Jeon, T. Firestone, J. Rodgers, J. Melngalis,

"On Chip Microwave Power Detectors"

11:35 a.m. B. Jacob, H. Wong, S. Rodriguez and C. Dirik

"System-level Vulnerability & Mitigation"