Part I: Degradation in 3.2 nm Gate Oxides: Effects on Inverter Performance and MOSFET Characteristics

Part II: Noise in Circuits – Effects on Ultra-Thin Gate Oxide Degradation

Bill Knowlton and Jake Baker
Department of Electrical and Computer Engineering, Boise State University, Boise, ID
Acknowledgments

University and Industry Involvement
- Betsy Cheek (G), ECE
- Nate Stutzke (UG), ECE
- Santosh Kumar, Cypress Semiconductor
- Amy Moll, ME Faculty
- Dr. Amr Haggag, Motorola
- Carrie Lawrence (G), ECE

University and Industry Involvement
- Michael Ogas (UG), ECE
- Tim Lawrence (G), ECE
- Richard G. Southwick III (UG), ECE
- Kloy Debban (G), ECE
- Terry Lowman (UG), ECE
- Miles Wiscombe (UG), ECE

Funding
- 2001 DOD Multidisciplinary Research Initiative (MURI)
- NSF-Idaho EPSCoR Program
- Cypress Semiconductor
- NSF Major Research Instrumentation Grant
- DARPA Grant
- Governor’s Higher Education Initiative - Idaho State Board of Education
- 2003 Micron Campus Engineering Research Program
Part I:
Degradation in 3.2 nm Gate Oxides:
Effects on Inverter Performance and MOSFET Characteristics

Bill Knowlton and Jake Baker
Department of Electrical and Computer Engineering, Boise State University, Boise, ID
Outline

- Motivation and Statement of work
- Introduction & Background
- Experimental
- Circuit Stress Induced Dielectric Breakdown
- Circuit Implications
- Circuit Model
- Summary and Conclusion
Motivation:

- As gate oxides become thinner, new degradation modes appear and may cause reliability issues.
- Worldwide semiconductor market is over $200 billion/year.
- Cost of reliability & functionality assurance is estimated >$25 billion/year.
Question: As a device is used, what occurs to the oxide over time?

Answer: It wears out. Known as “wearout”.

- Occurs prior to dielectric breakdown.
- Causes oxide degradation
  - increased gate oxide leakage current
- Defects or traps are generated inside & at interfaces of Si/SiO₂
- Trap generation caused by:
  - Electric fields applied across the oxide
  - Tunneling current through the oxide
- Dielectric breakdown eventually occurs
Background: Reliability of Ultrathin Gate Oxides in MOS Devices

Fowler-Nordheim Tunneling

\[ E_{f,m} \]

\[ \text{SiO}_2 \text{ (9eV)} \]

\[ \text{p-type Si} \]

\[ E_{f,S} \]

Modification Carrier Affinity

\[ e^-: \sim 3.1 \text{ eV} \]
\[ h^+: \sim 4.9 \text{ eV} \]

Triangular barrier

Direct Tunneling

\[ E_{f,m} \]

\[ \text{SiO}_2 \]

\[ \text{p-type Si} \]

\[ E_{f,S} \]

Trapezoidal barrier

Band diagrams not to scale
Oxide Reliability: Study Wearout Degradation Mechanisms in Ultrathin Oxides

- Induce *wearout* prematurely – Use **Stress Testing**:
  - Constant Voltage Stress (CVS): *typically used*
  - Constant Current Stress (CCS)
  - Pulsed Voltage Stress (PVS)
  - Ramped Voltage Stress (RVS)

---

$I_G - V_G$ Sense Results: Degradation Mechanisms

Metrics Technology Interactive Characterization Software (Controls 4156C system)
Agilent 4156C Precision Semiconductor Parameter Analyzer
Agilent 16440A SMU/Pulse Generator Selector
Agilent E5250A Low Leakage Switch Matrix
8 Cascade Mirotech DCM-Series MicroManipulators and Micromanipulator Probe station & Camera

Materials Characterization & Device & IC Reliability Lab
W. Knowlton & A. Moll, Boise State University

Betsy Cheek, Grad Student
Electrical Engineering
Agilent 81110A Pulse/Pattern Generator Unit (2 channels)
Keithley 595 Quasistatic CV Meter
Keithley 4200 Semiconductor Characterization System
High Speed Oscilloscope
HP 4284A LCR meter
4 Cascade Mirotech DCM-Series MicroManipulators and Wafer Top and Bottom Probestation
Femto-Ampere and milli-Ohm resolution at room temperature

nMOSFET 3.2 nm Gate Oxide Tunneling Current

$t_{ox} = 3.2$ nm

$A_{ox} = 6.25 \times 10^{-6}$ cm$^2$

Room Temp.
Equipment Capability

Probes:
- Top and bottom of wafers
- < 5 um contacts

Through-wafer Cu vias: 50um dia. & 500 um length
Motivation

Oxide Reliability
MOS Devices

Integrated Circuit
Reliability

- Extensive studies on MOSCAPs and some on MOSFETs
- Gate oxide breakdown related circuit reliability?
  - Minimal work reported\textsuperscript{1-3}
  - Consequences are uncertain\textsuperscript{1,2}
  - Future scaling of high-performance CMOS ICs\textsuperscript{4,5}

  ✓ Word lines in a DRAM cell are pumped to a voltage above $V_{DD}$\textsuperscript{6}
    - Increased stress?
    - Breakdown mechanisms?

\textsuperscript{1}J. H. Stathis et al, WoDim, 2002. \hspace{1cm} \textsuperscript{2}R. Rodriguez et al, Transactions on Device Letters, pp. 559-561, 2002. \hspace{1cm} \textsuperscript{3}B. Kaczer et al, Transactions on Electron Devices, pp. 500-506, 2002.

Statement of Work

Gate Oxide degradation in CMOS Inverters
- Stress at Circuit Level

What happens to circuit operation?

- SPICE circuit model
  - Physical description

What happens to MOSFET characteristics?
Experimental

- Inverter parameters defined

- Sample voltage transfer characteristics ($VTC$)

- Sample voltage-time ($V$-$t$) domain

![Diagrams showing voltage output transfer characteristics and sample voltage-time domain.]
MOSFET Schematics
- Devices fabricated in a 0.16-µm CMOS technology
- $t_{ox}$: 3.2 nm
- $A_{ox}$: $6.25 \times 10^{-6}$ cm²
- $W_p/L_p$: 25 µm /25 µm
- $W_N/L_N$: 25 µm /25 µm

Inverter Circuit Schematic
- Nominal operating voltage
  - $V_{DD}$: 1.8 V
- Voltage transfer characteristics ($VTC$)
  - $V_{IN}$: 0 to 1.8 V sweep
- Voltage-time domain response ($V-t$)
  - $V_{IN}$: 1.8 V
  - Frequency: 2.5 kHz
  - Duty cycle: 50 %
Experimental Setup

- **Inverter configuration**
  - Off-wafer via switch matrix
  - Stressing and characterization at transistor and circuit level

- **Stress Configuration**
  - Stress applied from input to output
  - Stress test
    - Ramped Voltage Stress (RVS)
  - Test conditions
    - Positive and negative stress
    - $V_{IN}$: 8 V, 10 V, 12 V, 14 V
    - $V_{OUT}$: 0 V
    - $V_{DD}$ and GND nodes floating\(^1\)

\(^1\) J. H. Stathis et al, WoDim, 2002.
Experimental Procedure

**Pre-Stress Response**
- Configure Inverter Measure: $VTC, V-t$
- Disconnect Circuit /Isolate MOSFET
- Stress Testing? [n  y]
- **End Test** [y  n]

**Post-Stress Response**
- Induce Stress
- Both MOSFETs Simultaneously [n  y]
- Both MOSFETs Individually [y  n]
- 1 MOSFET Individually [y  n]
Circuit Stress Induced Breakdown - MOSFETs

**MOSFET gate leakage currents**

(LHBD = limited hard breakdown $^1, ^2, ^3$)

Positive Voltage Stress

$n$MOSFET

$|I_g| (A)$ vs $V_g (V)$

$|J_g| (A/cm^2)$ vs $V_g (V)$

$p$MOSFET

$|I_g| (A)$ vs $V_g (V)$

$|J_g| (A/cm^2)$ vs $V_g (V)$

Negative Voltage Stress

$|I_g| (A)$ vs $V_g (V)$

$|J_g| (A/cm^2)$ vs $V_g (V)$

[References]


Circuit Stress Induced Breakdown - MOSFETs

- MOSFET log $I_D-V_G$ Characteristics

**nMOSFET**

- $V_D = 1.8$ V
- $\Delta I_{On} = 38 \ \mu$A, -V
- $\Delta I_{On} = 37 \ \mu$A, +V
- $\Delta I_{Off} = 1.9$ pA, -V
- $\Delta I_{Off} = 0.2$ pA, +V

**pMOSFET**

- $V_D = -1.8$ V
- $\Delta I_{On} = 8.8 \ \mu$A, -V
- $\Delta I_{On} = 5.6 \ \mu$A, +V
- $\Delta I_{Off} = 1.1$ pA, -V
- $\Delta I_{Off} = 2.2$ pA, +V
Circuit Stress Induced Breakdown - MOSFETs

- nMOSFET $I_D-V_D$ Characteristics:

Positive stress voltage

- $V_G = 1.8$ V

Negative stress voltage

- $V_G = 1.8$ V

- Fresh
- 8 V
- 10 V
- 12 V
- 14 V
Circuit Stress Induced Breakdown - Inverter

- Inverter voltage transfer characteristics (VTC)

Positive Voltage Stress

Negative Voltage Stress

- Fresh
- $8\text{ V}$
- $10\text{ V}$
- $12\text{ V}$
- $14\text{ V}$
VTC – Comparison of Only Other Publication

- Inverter voltage transfer characteristics (VTC)

- What about time domain?
- Individual MOSFETS?

---

Circuit Stress Induced Breakdown - Inverter

- Inverter voltage-time domain ($V$-$t$) response

**Positive Voltage Stress**

**Negative Voltage Stress**

- Fresh
- 8 V
- 10 V
- 12 V
- 14 V
## Circuit Implications

<table>
<thead>
<tr>
<th>Problem</th>
<th>Consequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increased off-state leakage current</td>
<td>✓ Increased power consumption¹</td>
</tr>
<tr>
<td></td>
<td>✓ Circuit failure (&gt;1 billion transistors on a chip)</td>
</tr>
<tr>
<td>Increased gate leakage current</td>
<td>✓ Loading of circuit stages¹</td>
</tr>
<tr>
<td>Increased rise/fall/delay times</td>
<td>✓ Timing issues in high-speed circuits¹</td>
</tr>
</tbody>
</table>

Circuit Model

- Circuit elements
  - Resistor-diode pairs
    - Connected from gate-drain
  - Resistors
    - Connected from gate-source
  - Diode emission equation\(^2\)
    - \(I_D = I_S \cdot [\exp \left( \frac{V_D}{N \cdot V_T} \right) - 1]\)
    - \(I_S\) (saturation current), \(V_D\) (diode voltage), \(N\) (emission coefficient), \(V_T\) (thermal voltage)

- MOSFET threshold voltage \((V_{th})\)

---

Inverter voltage transfer characteristics (VTC)

Positive Voltage Stress

Negative Voltage Stress

Line = Data
Symbol = Model

VSP
VOL
VOUT (V)
VIN (V)
VOH

Inc. (+) Stress

Fresh

Inc. (-) Stress

Fresh

8 V 10 V 12 V 14 V
Conclusion

- Circuit level stress
  - Determine degradation in individual devices
  - Ability to connect device degradation to circuit degradation

- VTC measurements may show negligible inverter degradation
  - Suggests Oxide degradation effects in Inverters are not a reliability issue

- Time-domain behavior may be severely degraded!
  - Suggests Oxide degradation effects in Inverters are a reliability issue

- V-t data introduces another characteristic for digital circuit reliability
  - Need for more suitable reliability criterion\textsuperscript{1-3}

Study suggests that the time domain is the more suitable criteria

Future Publications and Work

- Other SICBBs: T-gates, current mirrors, etc.
- Thinner gate dielectrics: 2.1 nm & thinner, high-k (Cypress & Semitech)
- Determine Trap identity WRT Oxide Degradation Mechanism – Penn State
- Interconnect coupling/crosstalk effects on oxides

Betsy J. Cheek, Nate Stutzke, Miles Wiscombe, Terry Lowman, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton

*Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*


Betsy J. Cheek, Student Member, IEEE, Nate Stutzke, Student Member, Santosh Kumar, Member, IEEE, R. Jacob Baker, Senior Member, IEEE, Amy J.Moll, William B. Knowlton, Member, IEEE

*Investigation of Gate Oxide Reliability: Consequences of Dielectric Breakdown on MOSFET Characteristics and CMOS Inverter Performance*

Part II: Noise in Circuits – Effects on Ultra-Thin Gate Oxide Degradation

Bill Knowlton and Jake Baker

*Department of Electrical and Computer Engineering, Boise State University, Boise, ID*
Project Definition and Motivation

- Investigate the effects of noise in circuits using MWPVS

- Model noise as a voltage spike constructively interfering with a carrier signal due to superposition of waves
  - Noise on signal lines due to:
    - Electromagnetic radiation (space applications)
    - Very close interconnect proximity
    - Capacitive coupling

\[ V_{\text{gate}} + \text{spike} = \text{output} \]

\[ ^{0}\text{Baker et. al., CMOS: Circuit Design, Layout, and Simulation (Wiley, 1998).} \]
Reliability Test Methods

CVS (constant voltage stress)
- NOT typical for digital circuit operation

PVS (pulse voltage stress)
- Better mimics digital device behavior

MWPVS
- Represents circuit operation with noise
Combined signals from two Waveform Generators (WFG) programmed with:

- Frequency
  - 5 kHz
- Voltage Amplitude
  - Carrier Signal: -5 V
  - Noise Signal: 0 V, -1 V, -3 V, -5 V
- Duty Cycle
  - Carrier Signal: 75 %
  - Noise Signal: 5 % & 25 %
I_G-V_G Sense Results

\[ t_{ox} = 3.2 \text{ nm} \]
\[ A_{ox} = 2.1 \times 10^{-4} \text{ cm}^2 \]

MWPVS: (carrier & noise)
- 5 kHz(-5 V & 0 V)
- 5 kHz(-5 V & -3 V)
- 5 kHz(-5 V & -1 V)
- 5 kHz(-5 V & -5 V)

- HBD @ -2 V ~ 0.1 A
- LHBD
- SILC
- Fresh
MWPVS Weibull Distribution

ln[-ln(1-F)] vs. time-to-breakdown (s)

MWPVS: 5 kHz
Carrier signal: –5 V
Noise signal:
- 0 V (baseline)
D. C. 5 %:
- 1 V
- 3 V
- 5 V
D. C. 25 %:
- 1 V
- 3 V
- 5 V
CVS:
- 5 V

β
Initial data indicates that increasing the noise signal decreases device lifetime exponentially†

- $d$, constant proportional to $DC_{BASE}$ of carrier signal
- $d'$, constant proportional to $DC_{SPIKE}$ of noise signal
- $c$, voltage accelerator factor
- $dV$, noise amplitude

\[
\frac{1}{t_{bd,2}} \approx d \cdot e^{c |V|} + d' \cdot e^{c(|V|+|dV|)}
\]

Experimental Setup for MWPVS

- **Carrier signal parameters:**
  - 20 kHz and 100 kHz frequency (F)
  - 75% duty cycle (DC\textsubscript{BASE})
  - -5 V base amplitude (V\textsubscript{BASE})

- **Noise signal parameters:**

- **Stress effects:**
  - Monitored through gate leakage current (I\textsubscript{GATE} - V\textsubscript{GATE})
  - End test when leakage current reaches \( \approx 1 \text{ mA} \) (Limited Hard Breakdown)\textsuperscript{1-2}

<table>
<thead>
<tr>
<th>Duty Cycle (DC\textsubscript{SPIKE})</th>
<th>25 %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Spike Voltage Amplitude (V\textsubscript{SPIKE})</td>
<td>-1 -3 -5</td>
</tr>
</tbody>
</table>

Devices: nMOSCAPs
- \( t\textsubscript{ox} = 3.2 \text{nm} \)
- \( A\textsubscript{ox} = 2.1 \times 10^{-4} \text{ cm}^2 \)

---


Pre- and post- MWPVS

I_{\text{GATE}}-V_{\text{GATE}} results:

- Degradation mechanisms observed:
  - SILC (Stress Induced Leakage Current)\(^3\)\(^-\)\(^4\)
  - SBD and Softer SBD (Soft Breakdown)\(^5\)
  - LHBD (Limited Hard Breakdown)\(^2\)

Example of nMOSCAP degradation at \(V_{\text{BASE}} = -5\) V, \(V_{\text{SPIKE}} = -1\) V, \(F = 20\) kHz, \(DC_{\text{BASE}} = 75\%\), \(DC_{\text{SPIKE}} = 25\%\).

---


MWPVS Vs. CVS

Weibull plots indicate device lifetime decreases by orders of magnitudes when compared to preliminary CVS data.
Conclusions

- Designed a MWPVS technique to simulate noise
- Reliability Issues
  - Constructive Interference occurs due Superposition of waveforms
    - Electromagnetic radiation
    - Capacitive Coupling
    - Mixed Signals
- Device lifetime shorter for MWPVS than PVS

Data corresponds to the noise model: Device lifetime exponentially decreases with increase in noise voltage
Future Work

- Further testing of 20 kHz and 100 kHz with PVS method
- Further testing of 20 kHz and 100 kHz with spike duty cycle of 5% with MWPVS method
- Lower Stress Voltage to replicate lower voltages being used in circuits
- Breakdown mechanisms as a function of higher frequency noise
- Accumulation breakdown effects on inversion
Thank You

Questions?
The (100) Si/SiO₂ Interface:
Two closely related interface state defects $P_{b0}$ and $P_{b1}$

SiO₂ Trapping Centers:
Intrinsic oxygen deficient silicon E’ centers (some coupled to hydrogen)

Many extrinsic defects:
We know about these centers from electron spin resonance (ESR) studies.

Courtesy: Patrick Lenahan, Penn State
$P_{b1}$

Tourist: Patrick Lenahan, Penn State
TEOS BPSG Trapping Centers

P1
Spin density decreases with hole injection

P2
Spin density decreases with hole injection

P4
Spin density decreases with electron injection

E’
Spin density generally increases with hole injection; generally decreases with electron injection

Methanol Radical
One of several organic radicals present in these films. Some organic spin densities increase with hole injection other increase with electron injection

Courtesy: Patrick Lenahan, Penn State
Effects of Dielectric Breakdown

MOSFET linear $I_D-V_G$ Characteristics

nMOSFET

pMOSFET
Circuit Stress Induced Breakdown - MOSFETs

- MOSFET $I_D-V_D$ Characteristics: *Negative voltage stress*

### nMOSFET

- $V_G = 1.8$ V
- $V_D$ ranges from 0 to 1.8 V
- $I_D$ ranges from $10^{-4}$ A to $10^{-5}$ A

### pMOSFET

- $V_G = -1.8$ V
- $V_D$ ranges from 0 to -1.8 V
- $I_D$ ranges from $10^{-5}$ A to $10^{-6}$ A

Legend:
- ■ Fresh
- △ 8 V
- ◇ 10 V
- ○ 12 V
- □ 14 V
Inverter input leakage current results
(CLHBD = circuit limited hard breakdown)

Positive Voltage Stress

Negative Voltage Stress

| \( |I_{\text{Input}}| \ (A) \) |
|------------------|
| \( V_{\text{IN}} \ (V) \) |

| \( |J_{\text{Input}}| \ (A/cm^2) \) |
|------------------|
| \( V_{\text{IN}} \ (V) \) |

- Fresh
- \( 8 \) V
- \( 10 \) V
- \( 12 \) V
- \( 14 \) V
Equipment Capability

- Resistance resolution: $m\Omega$ resolution (Cu vias)

Four Point Probe Measurement on Cu TWI

- Voltage (V) vs. Current (A) graph showing resistance values ranging from 2.369 m$\Omega$ to 4.659 m$\Omega$. Each resistance value is represented by a different line color and marker style on the graph.
2.1 nm Gate Oxides

- Tunneling current is Direct

![Graph showing nMOSFET I_G-V_G characteristics with the following details:

- $t_{ox} = 2.1$ nm
- $A_{ox} = 6.25 \times 10^{-6}$ cm$^2$
- Room Temp.

- Fresh $I_G$-V$_G$ points

- Accumulation and Inversion regions highlighted.](image-url)
Summary

What type of oxide degradation has been introduced into the gate oxide to cause these types of VTCs?

- MOSFET LHBD
- Inverter CLHBD
  - Similar to the MOSFET degradation mechanism LHBD
  - Suggests oxide degradation mechanisms in simple circuits are similar to MOSFETs

How do the individual devices respond to this type of degradation?

- Increased off-state leakage current
- Increased gate leakage currents
- Decreased $g_m$, increased $V_{th}$
Importantly, how does this affect the time domain?

- Reduced output swing
  - $V_{OH}$ decreases
    - Positive or negative stress
  - $V_{OL}$
    - Positive, *increases* with increasing stress
    - Negative, *decreases* with increasing stress
- Increased rise- and fall-times

Circuit model

- Observed both Ohmic and non-Ohmic (exponential) behavior in data
- Physical Explanation
  - Resistor = Ohmic
  - Diode = non-Ohmic
- Result: Both Positive and negative data fit well