BOISE STATE UNIVERSITY

Part I: Degradation in 3.2 nm Gate Oxides: Effects on Inverter Performance and MOSFET Characteristics

Part II: Noise in Circuits – Effects on Ultra-Thin Gate Oxide Degradation

Bill Knowlton and Jake Baker

Department of Electrical and Computer Engineering, Boise State University, Boise, ID

College of Engineering

Acknowledgments

- University and Industry Involvement
  - Betsy Cheek (G), ECE
  - Nate Stutzke (UG), ECE
  - Santosh Kumar, Cypress Semiconductor
  - Amy Moll, ME Faculty
  - Dr. Amr Haggag, Motorola
  - Carrie Lawrence (G), ECE
- University and Industry Involvement
  - Michael Ogas (UG), ECE
  - Tim Lawrence (G), ECE
  - Richard G. Southwick III (UG), ECE
  - Kloy Debban (G), ECE
  - Terry Lowman (UG), ECE
  - Miles Wiscombe (UG), ECE
- Funding
  - 2001 DOD Multidisciplinary Research Initiative (MURI)
  - NSF-Idaho EPSCoR Program
  - Cypress Semiconductor
  - NSF Major Research Instrumentation Grant
  - DARPA Grant
  - Governor's Higher Education Initiative - Idaho State Board of Education
  - 2003 Micron Campus Engineering Research Program

BOISE STATE UNIVERSITY

Part I:
Degradation in 3.2 nm Gate Oxides: Effects on Inverter Performance and MOSFET Characteristics

Bill Knowlton and Jake Baker

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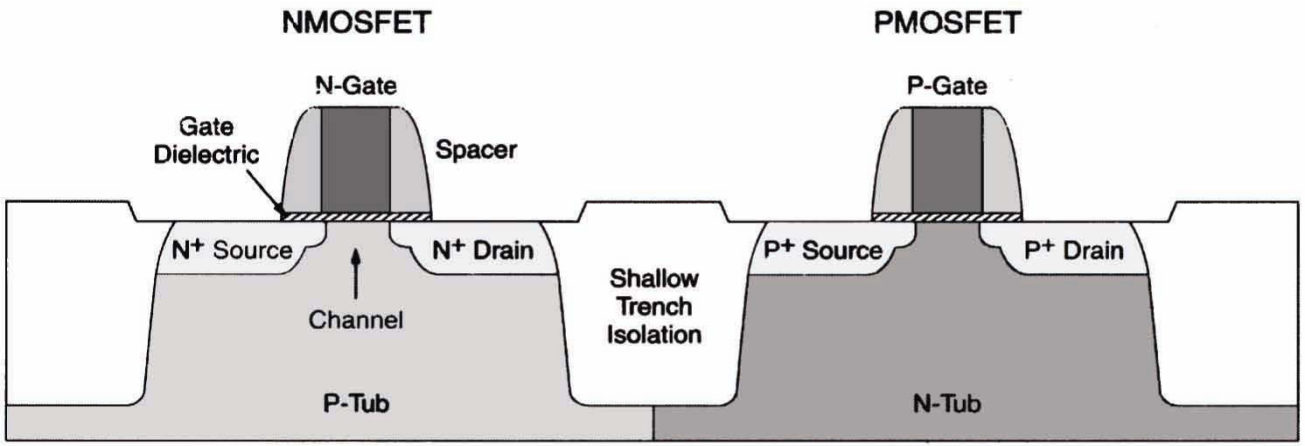
College of Engineering

Outline

- Motivation and Statement of work
- Introduction & Background
- Experimental
- Circuit Stress Induced Dielectric Breakdown
- Circuit Implications
- Circuit Model
- Summary and Conclusion

Reliability of Ultrathin Gate Oxides in MOS Devices

- Motivation:
  - As gate oxides become thinner, new degradation modes appear and may cause reliability issues.
  - Worldwide semiconductor market is over $200 billion/year.
  - Cost of reliability & functionality assurance is estimated >$25 billion/year.

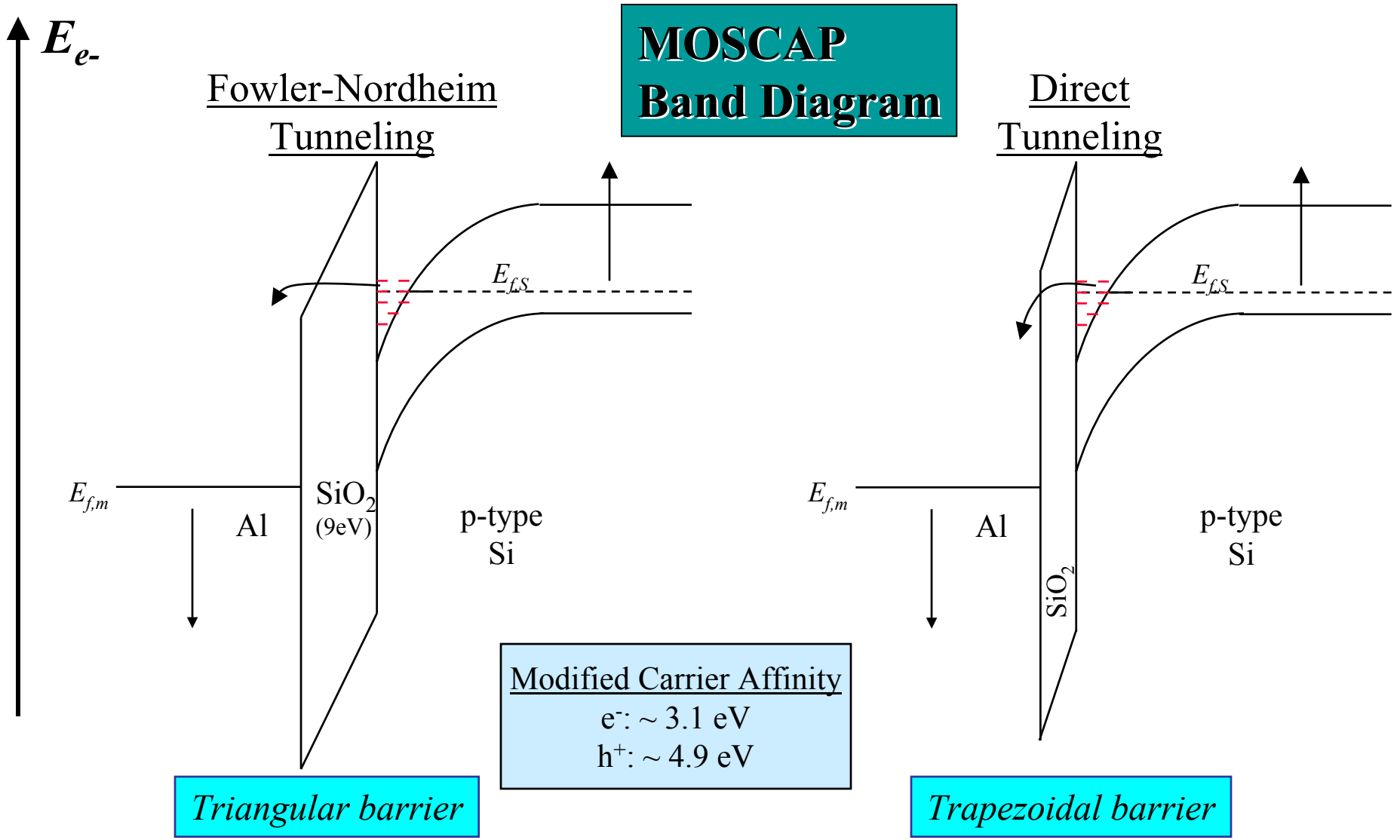


Green *et al.*, J. Appl. Phys., **90** (2001) 2057

Background: Reliability of Ultrathin Gate Oxides in MOS Devices

- Question: As a device is used, what occurs to the oxide over time?
- Answer: It wears out. Known as "*wearout*".
  - ✓Occurs prior to dielectric breakdown.
  - ✓Causes oxide degradation
    - increased gate oxide leakage current
  - ✓Defects or traps are generated inside & at interfaces of Si/SiO_2
  - ✓Trap generation caused by:
    - Electric fields applied across the oxide
    - Tunneling current through the oxide
  - ✓Dielectric breakdown eventually occurs

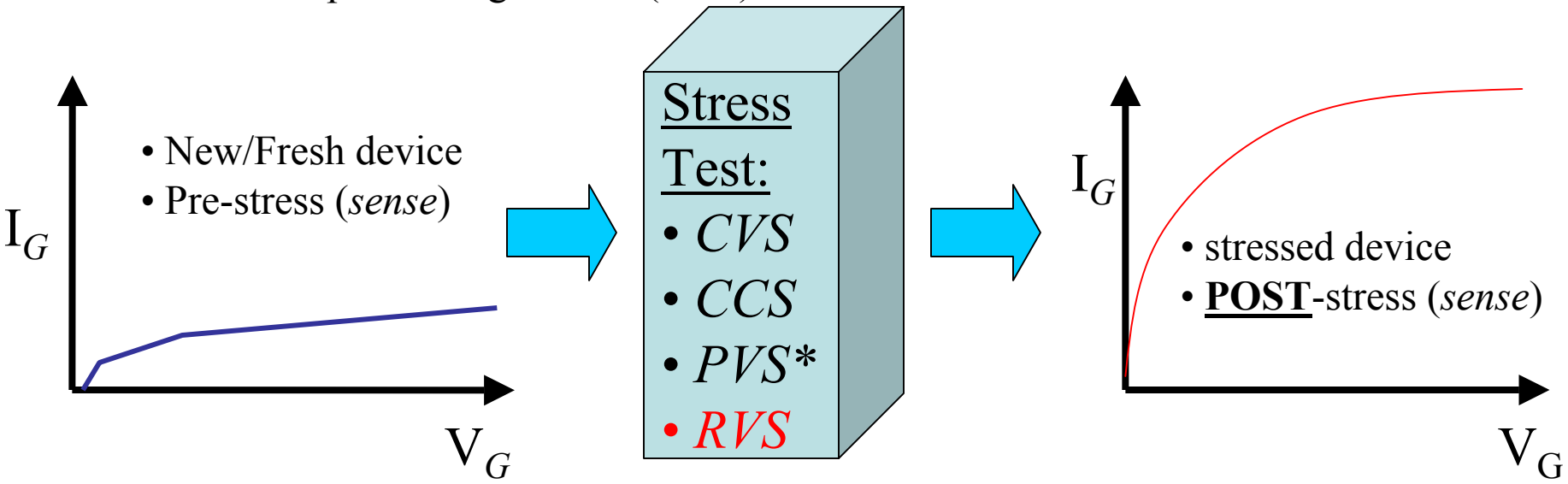
Background: Reliability of Ultrathin Gate Oxides in MOS Devices



Band diagrams not to scale

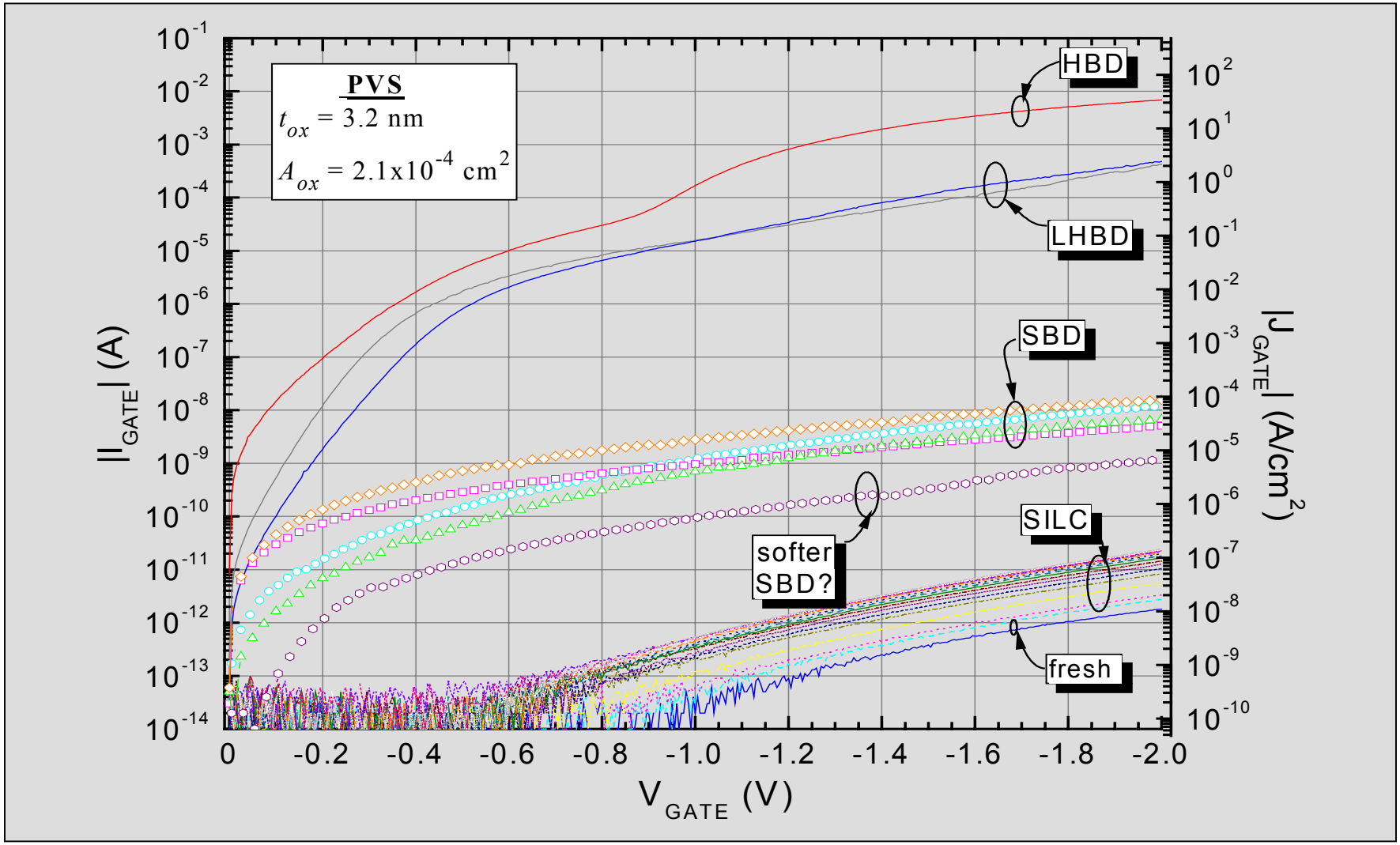
Background: Reliability Test Methods

- Oxide Reliability: Study Wearout Degradation Mechanisms in Ultrathin Oxides
  - Induce *wearout* prematurely – Use Stress Testing:
    - ✓ Constant Voltage Stress (CVS): *typically used*
    - ✓ Constant Current Stress (CCS)
    - ✓ Pulsed Voltage Stress (PVS)
    - ✓ Ramped Voltage Stress (RVS)



*Lawrence, C.E., B.J. Cheek, T.E. Lawrence, Santosh Kumar, A. Haggag, R.J. Baker, and W.B. Knowlton, *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, in Proceedings of the 15th Biennial IEEE UGIM Symposium (2003), pp.263-266.

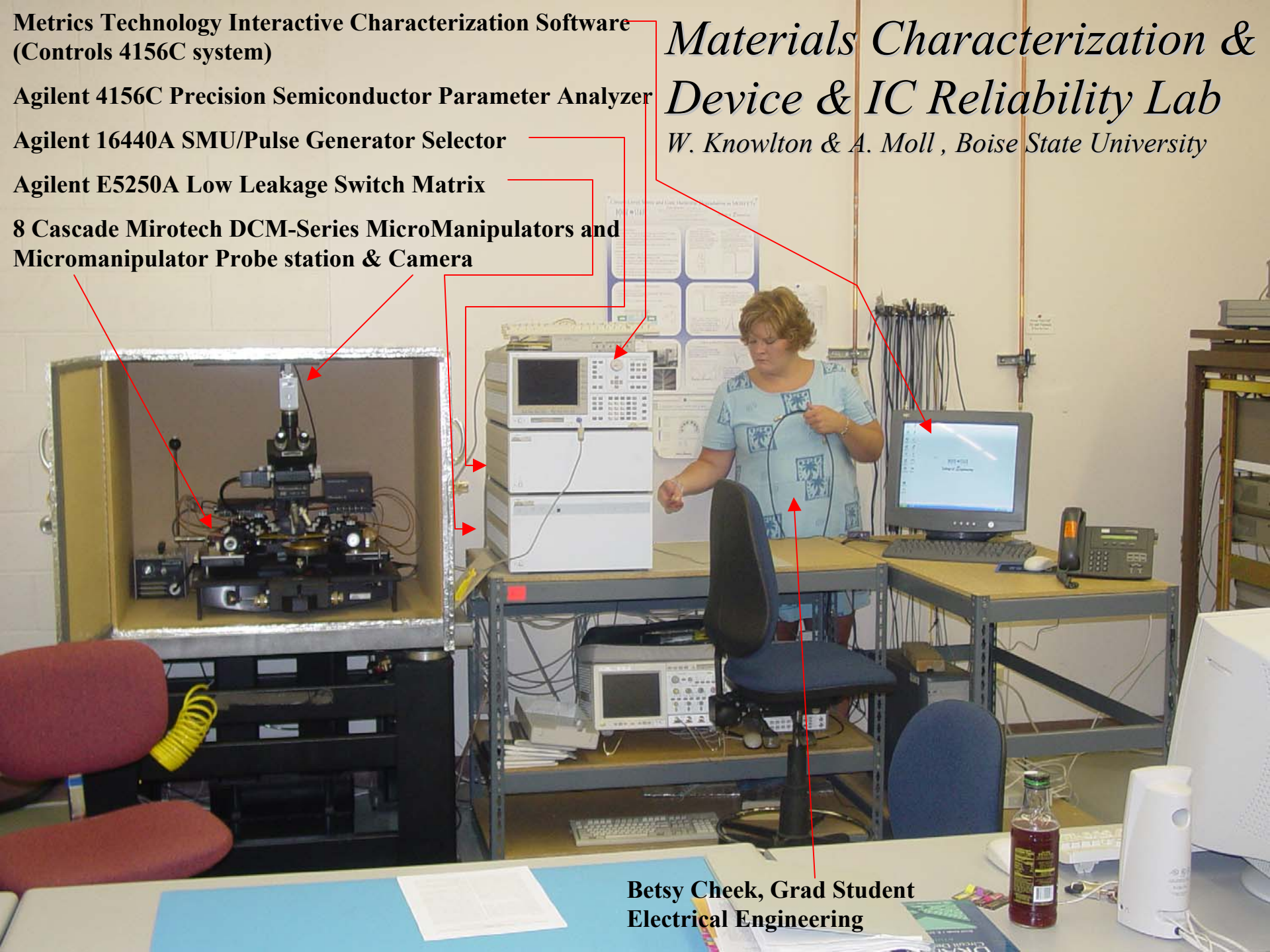
I_G-V_G Sense Results: Degradation Mechanisms



Knowlton, W.B., T. Caldwell, J.J. Gomez, and S. Kumar. *On the nature of ultrathin gate oxide degradation during pulse stressing of nMOSCAPs in accumulation.* in IEEE International Integrated Reliability Workshop, (2001) pp. 87-88.

Materials Characterization & Device & IC Reliability Lab

W. Knowlton & A. Moll , Boise State University



Materials Characterization & Device & IC Reliability Lab

W. Knowlton & A. Moll, Boise State University

Agilent 81110A Pulse/Pattern Generator Unit (2 channels)

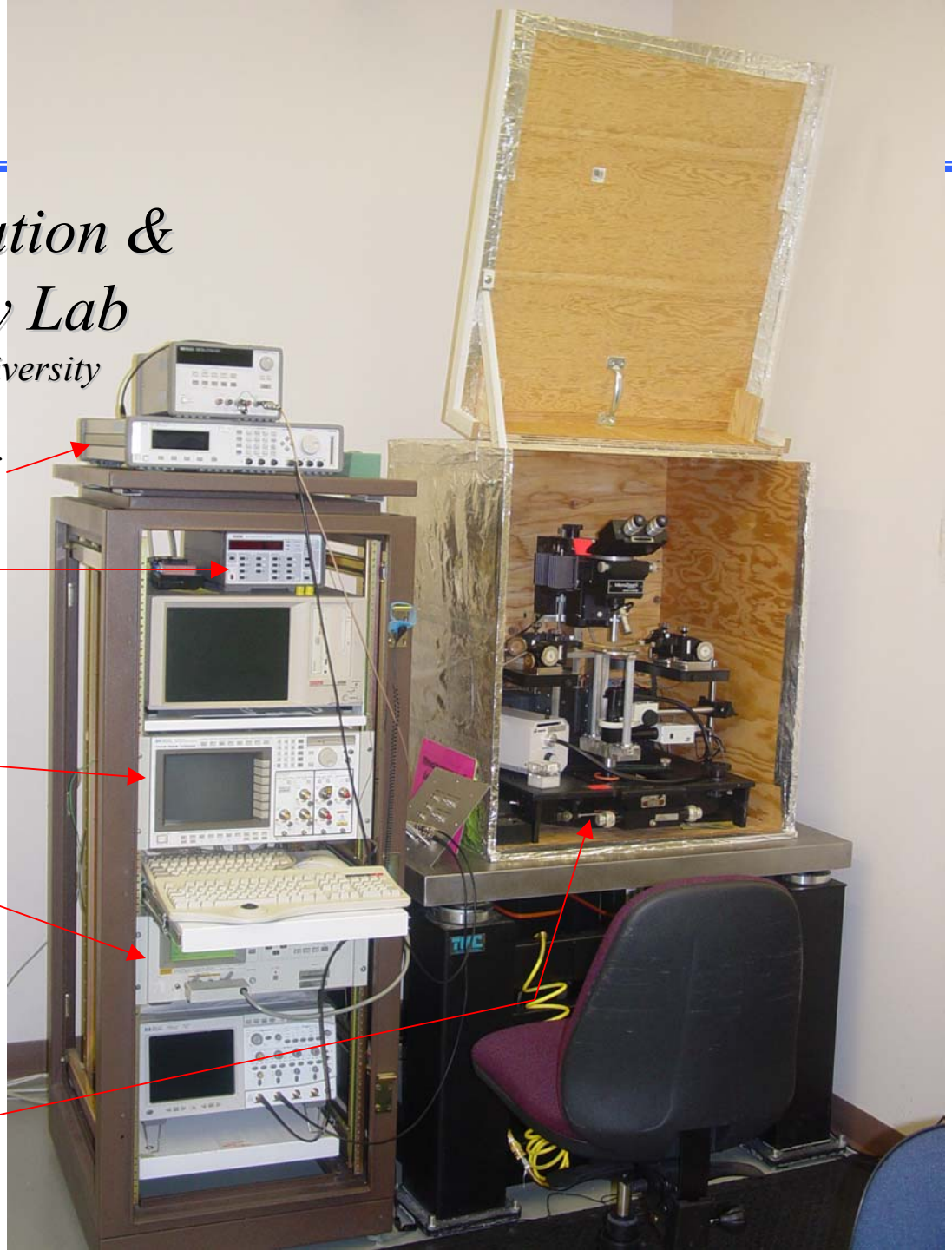
Keithley 595 Quasistatic CV Meter

Keithley 4200 Semiconductor Characterization System

High Speed Oscilloscope

HP 4284A LCR meter

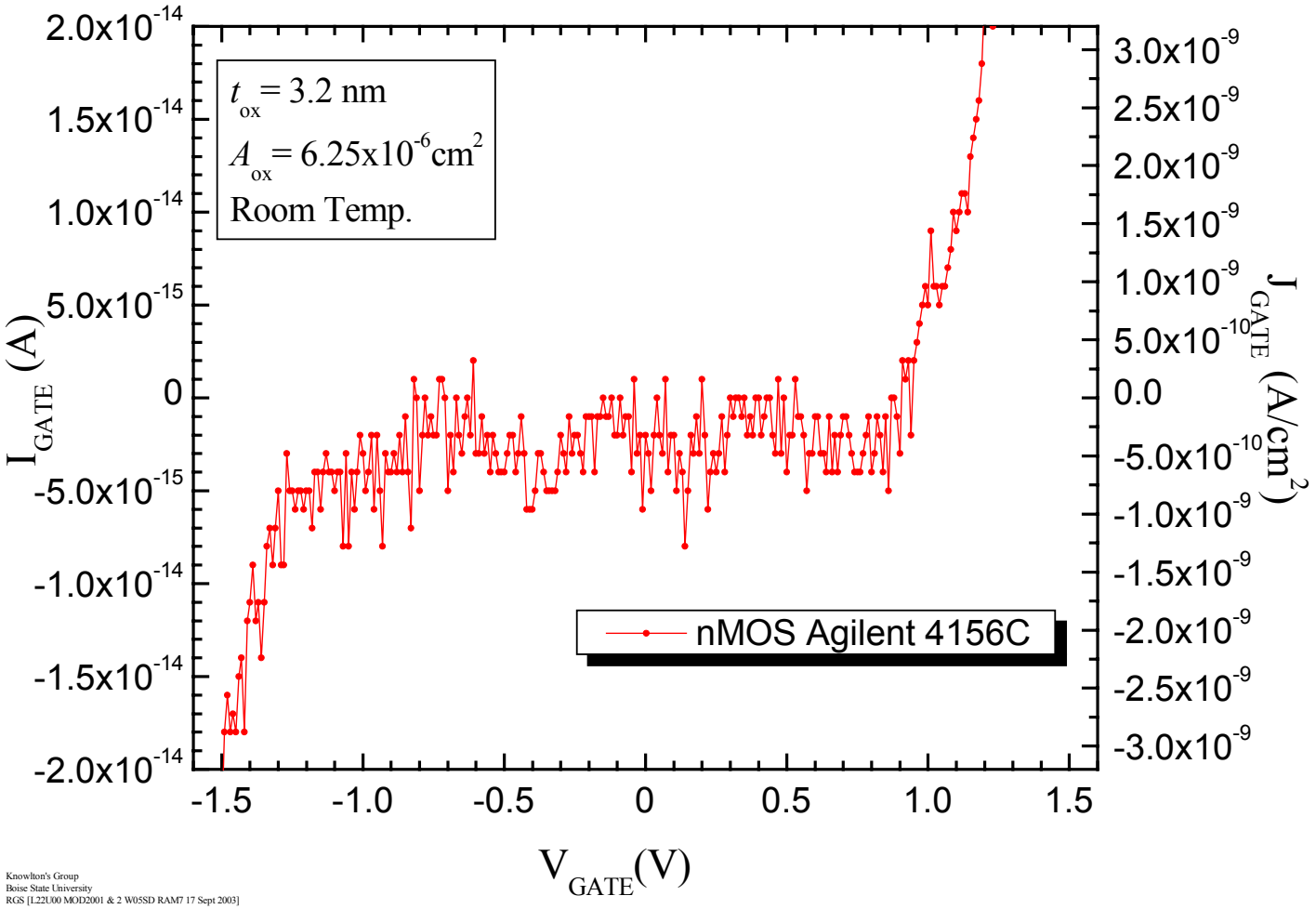
4 Cascade Mirotech DCM-Series MicroManipulators and Wafer Top and Bottom Probestation



Equipment Capability

- Femto-Ampere and milli-Ohm resolution at room temperature

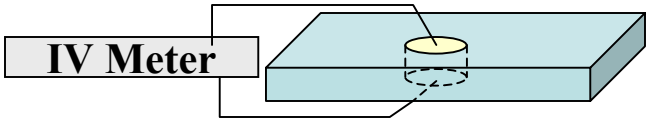
nMOSFET 3.2 nm Gate Oxide Tunneling Current

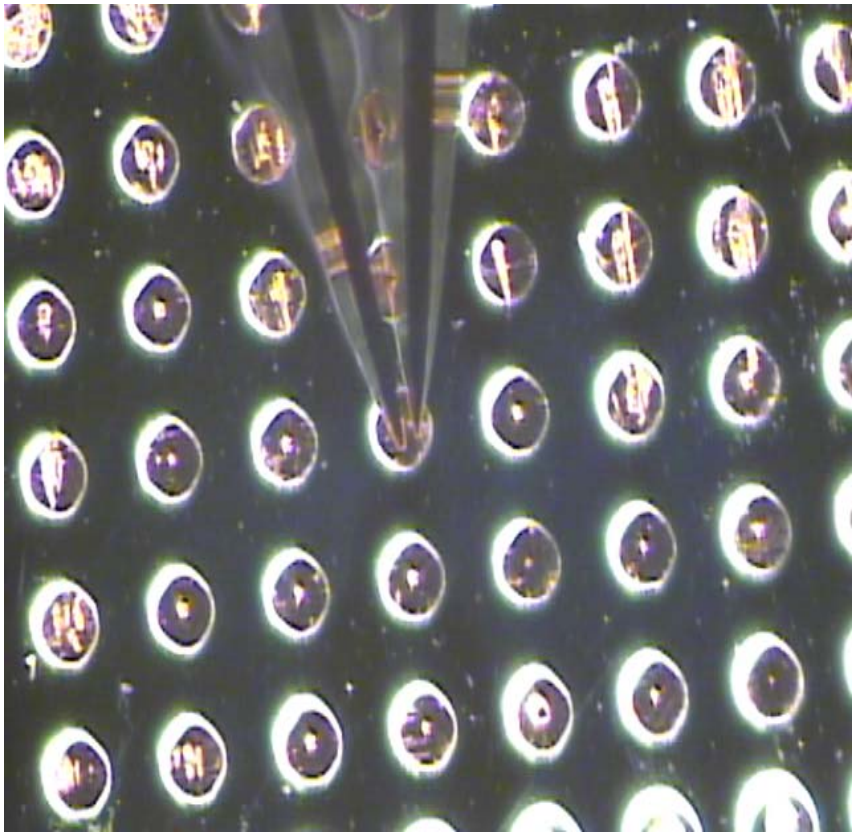


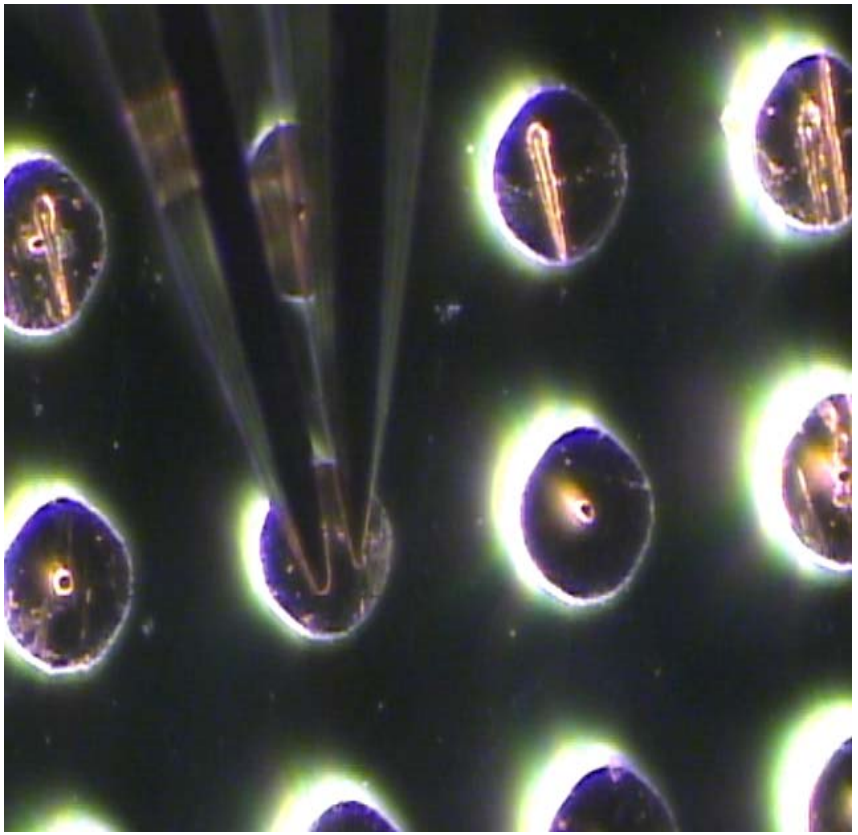
Knowlton's Group
Boise State University
RGS [L22U00 MOD2001 & 2 W05SD RAM7 17 Sept 2003]

Equipment Capability

- Probes:
  - Top and bottom of wafers
  - < 5 um contacts







Through-wafer Cu vias: 50um dia. & 500 um length

Motivation

Oxide Reliability
MOS Devices

Integrated Circuit
Reliability

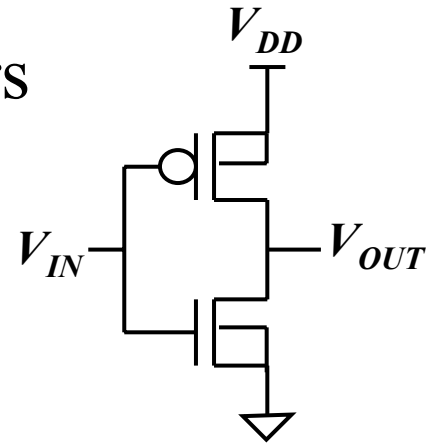
- Extensive studies on MOSCAPs and some on MOSFETs
- Gate oxide breakdown related circuit reliability?
  - Minimal work reported[1-3]
  - Consequences are uncertain[1,2]
  - Future scaling of high-performance CMOS ICs[4,5]
    - ✓ Word lines in a DRAM cell are pumped to a voltage above V_{DD}[6]
      - *Increased stress?*
      - *Breakdown mechanisms?*

[1]J. H. Stathis et al, WoDim, 2002. [2]R. Rodriguez et al, *Transactions on Device Letters*, pp. 559-561, 2002. [3]B. Kaczer et al, *Transactions on Electron Devices*, pp. 500-506, 2002.

[4]H. Iwai et al, IEDM., pp. 163-166, 1998. [5]J. H. Stathis et al, IEDM, pp. 167-169, 1998. [6]B. Keeth et al, IEEE Press, pp. 1-33,2001.

Statement of Work

- Gate Oxide degradation in CMOS Inverters
  - Stress at Circuit Level



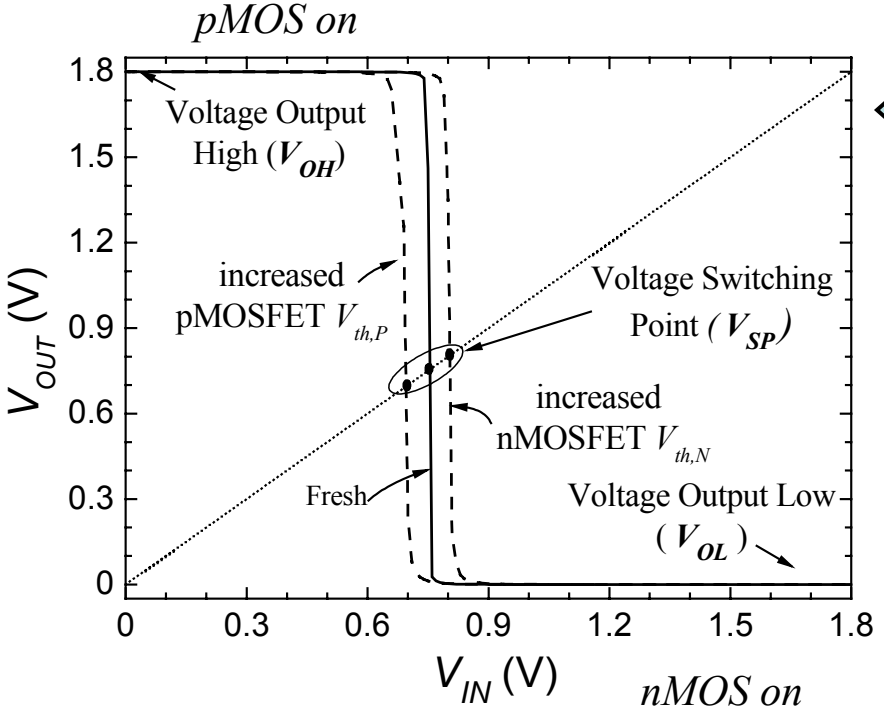
What happens to circuit operation?

What happens to MOSFET characteristics?

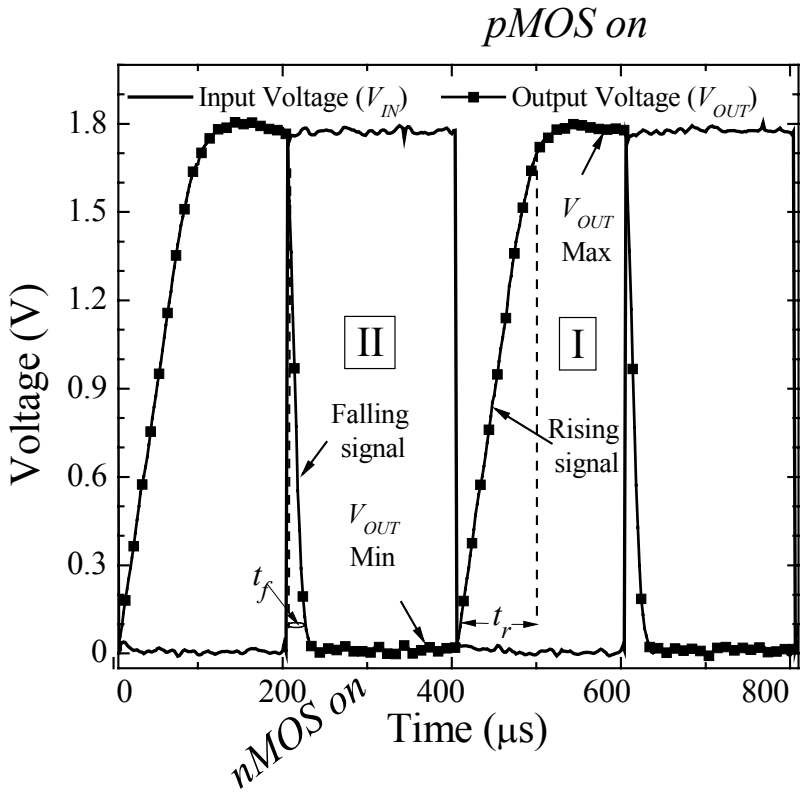
- SPICE circuit model
  - Physical description

Experimental

- Inverter parameters defined



Sample voltage transfer characteristics (*VTC*)

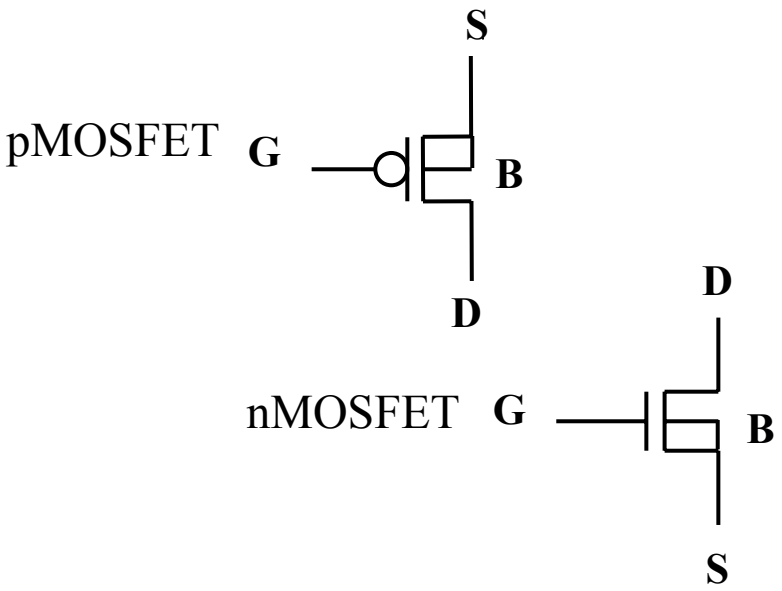


Sample voltage-time (*V-t*) domain

Experimental

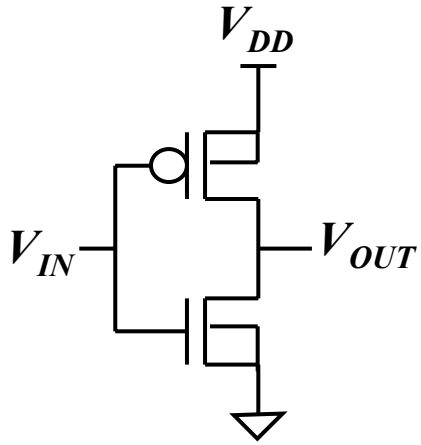
❑ MOSFET Schematics

- Devices fabricated in a 0.16-μm CMOS technology
- t_{ox}: 3.2 nm
- A_{ox}: 6.25 x 10^{-6} cm^2
- W_P/L_P: 25 μm /25 μm
- W_N/L_N: 25 μm /25 μm



❑ Inverter Circuit Schematic

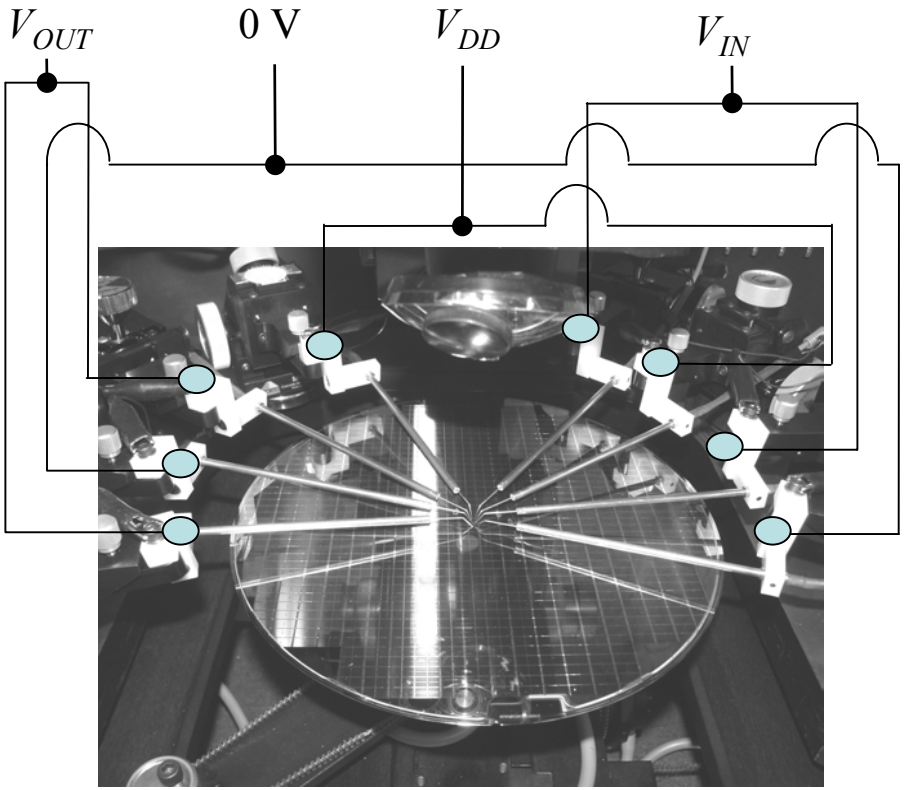
- Nominal operating voltage
  - ✓ V_{DD}: 1.8 V
- Voltage transfer characteristics (*VTC*)
  - ✓ V_{IN}: 0 to 1.8 V sweep
- Voltage-time domain response (*V-t*)
  - ✓ V_{IN}: 1.8 V
  - ✓ Frequency: 2.5 kHz
  - ✓ Duty cycle: 50 %



Experimental Setup

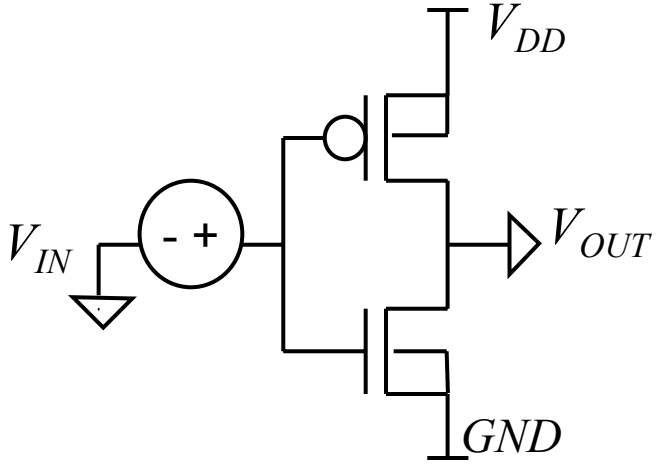
❑ Inverter configuration

- Off-wafer via switch matrix
- Stressing and characterization at transistor and circuit level



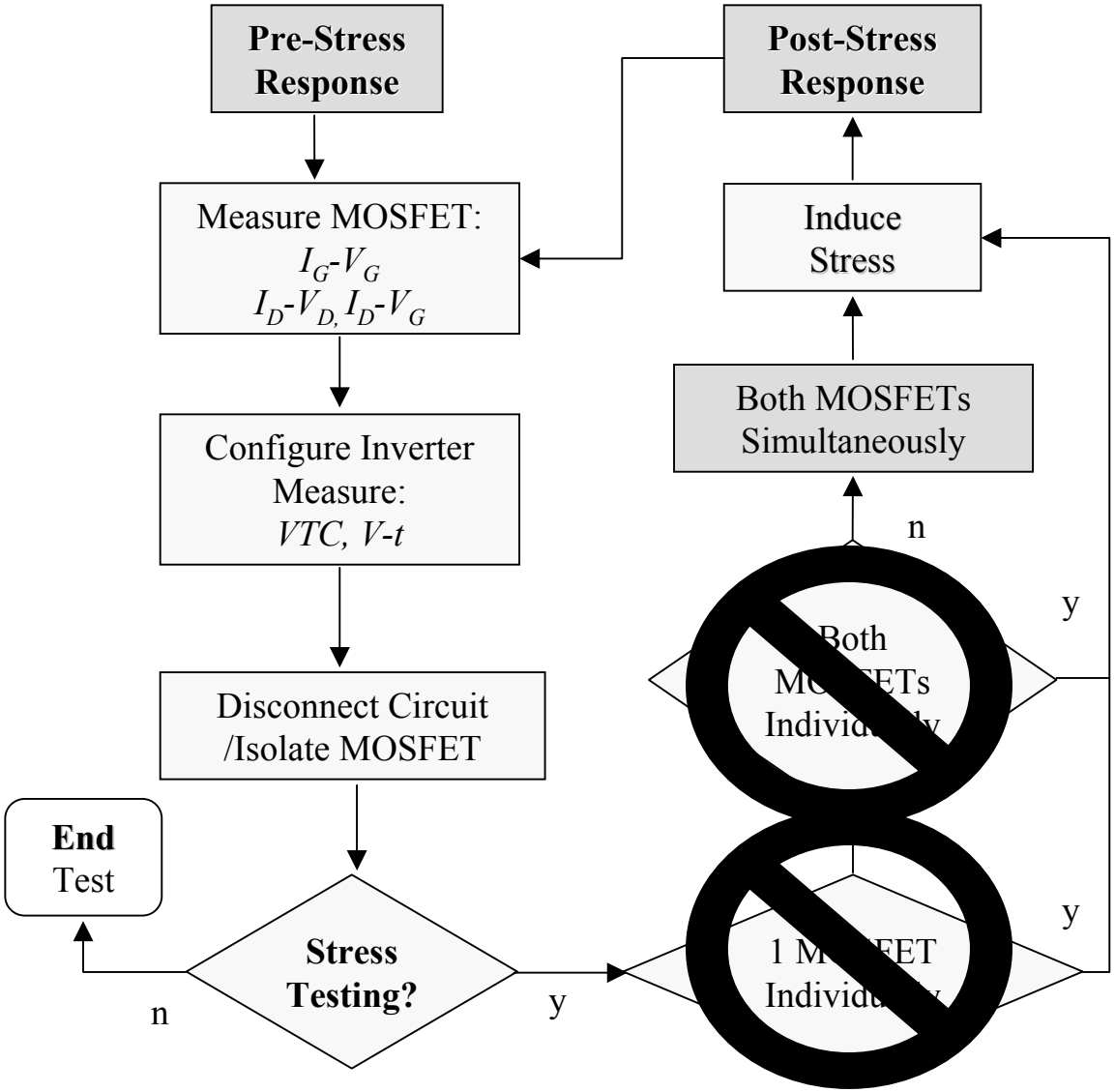
❑ Stress Configuration

- Stress applied from input to output
- Stress test
  - ✓ Ramped Voltage Stress (RVS)
- Test conditions
  - ✓ Positive and negative stress
  - ✓ V_{IN}: 8 V, 10 V, 12 V, 14 V
  - ✓ V_{OUT}: 0 V
  - ✓ V_{DD} and *GND* nodes floating[1]



[1] J. H. Stathis et al, WoDim, 2002.

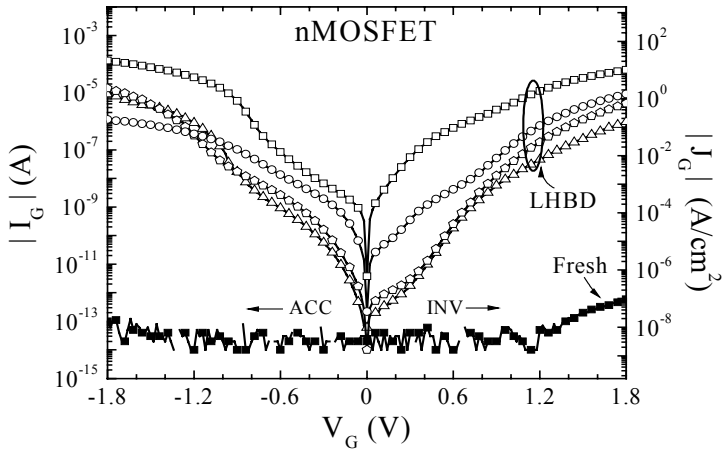
Experimental Procedure

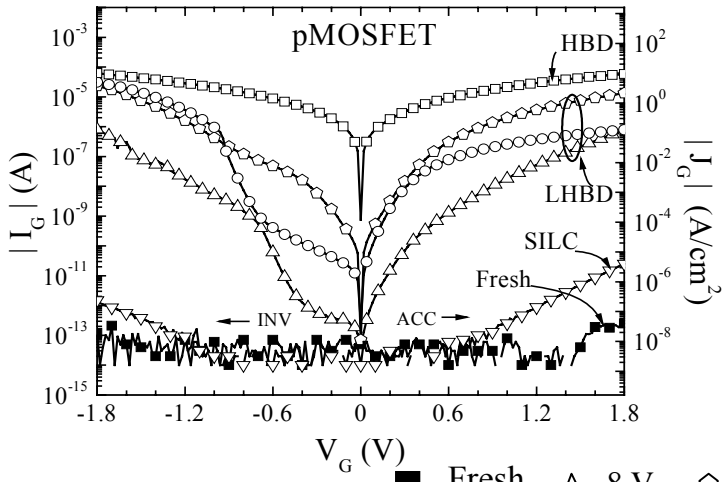


Circuit Stress Induced Breakdown - MOSFETs

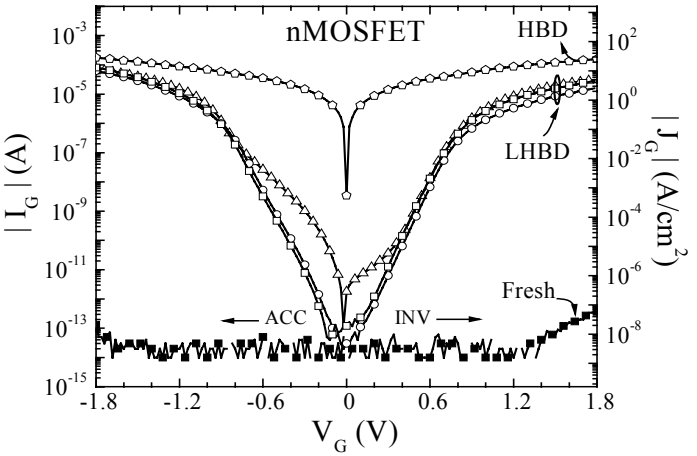
- MOSFET *gate* leakage currents (LHBD = limited hard breakdown [1, 2, 3])

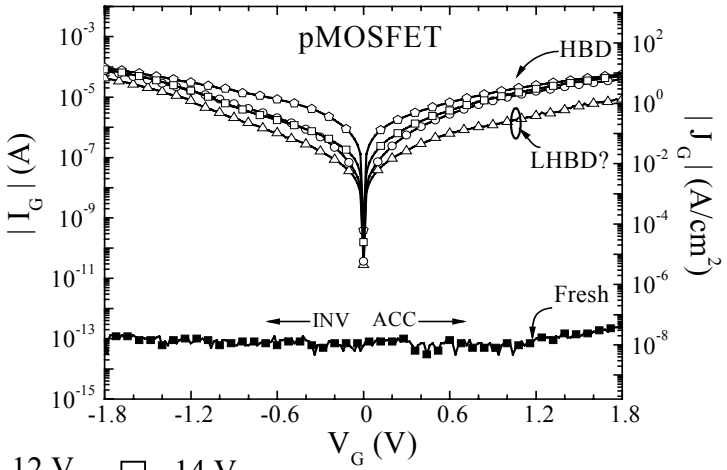
Positive Voltage Stress





Negative Voltage Stress





■ Fresh △ 8 V ⬠ 10 V ○ 12 V □ 14 V

$|I_g|$

V_g

[1]B. P. Linder et al, *VLSI Technology Digest of Technical Papers*, pp. 214-215, 2000.

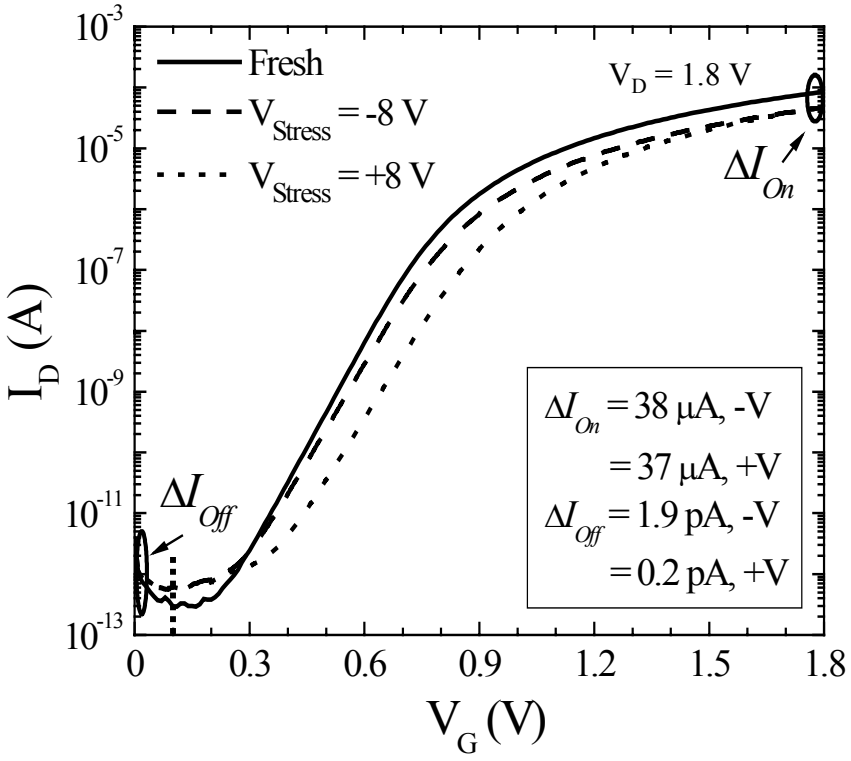
[2]W. B. Knowlton et al, Proc. of the IRW, pp. 87-88, 2001.

[3]B. Cheek et al, Workshop on Microelectronics and Electronic Devices, Boise, 2002.

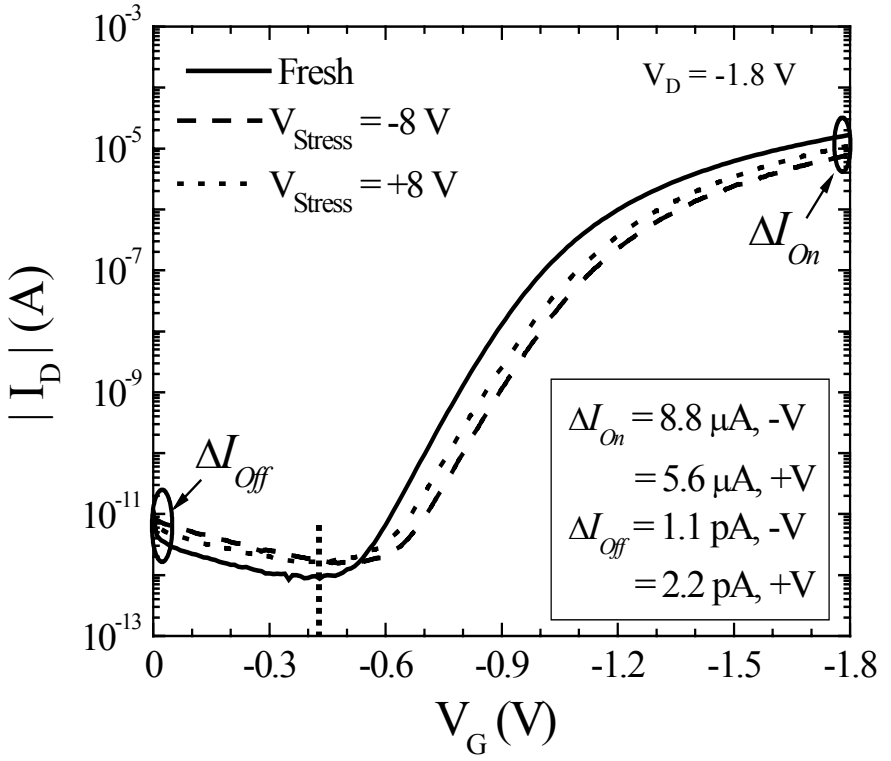
Circuit Stress Induced Breakdown - MOSFETs

- MOSFET log I_D-V_G Characteristics

nMOSFET



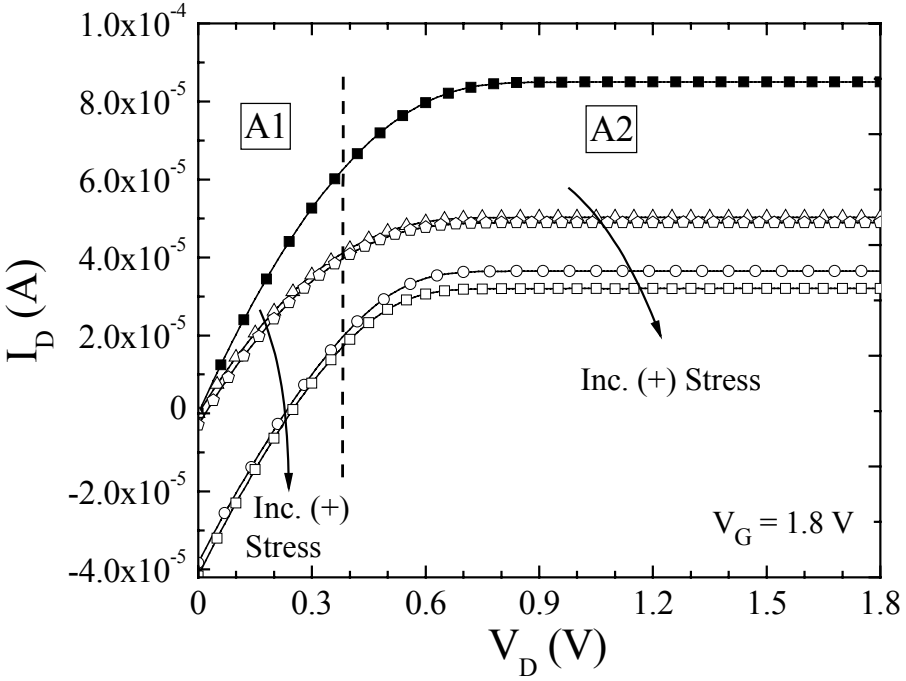
pMOSFET



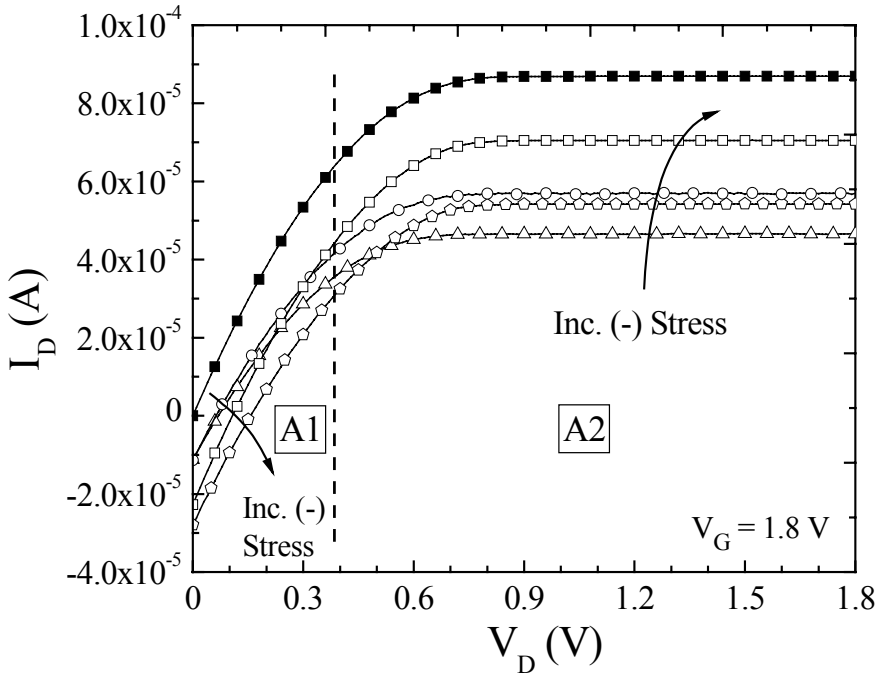
Circuit Stress Induced Breakdown - MOSFETs

- nMOSFET I_D-V_D Characteristics:

Positive stress voltage



Negative stress voltage

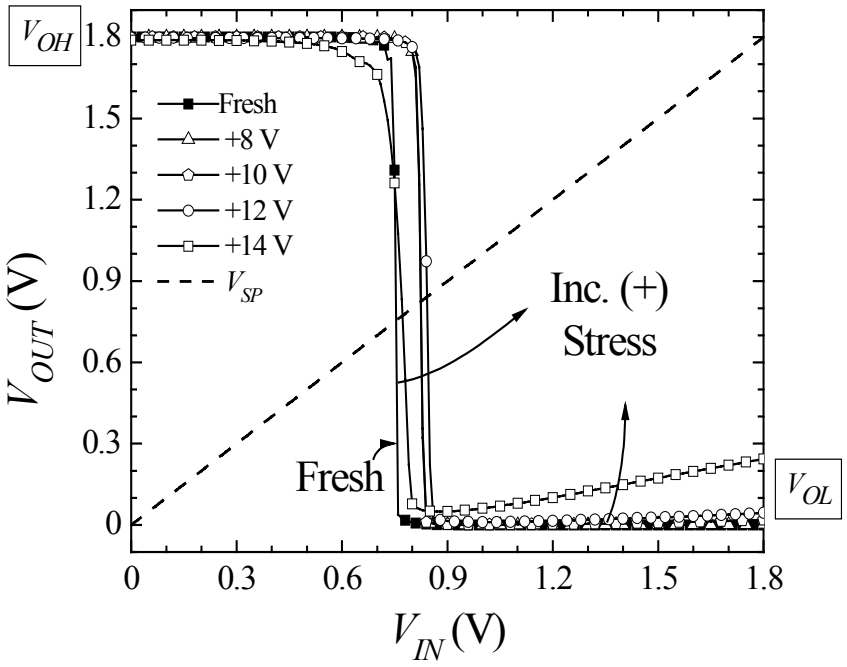


■ Fresh △ 8 V ⬠ 10 V ○ 12 V □ 14 V

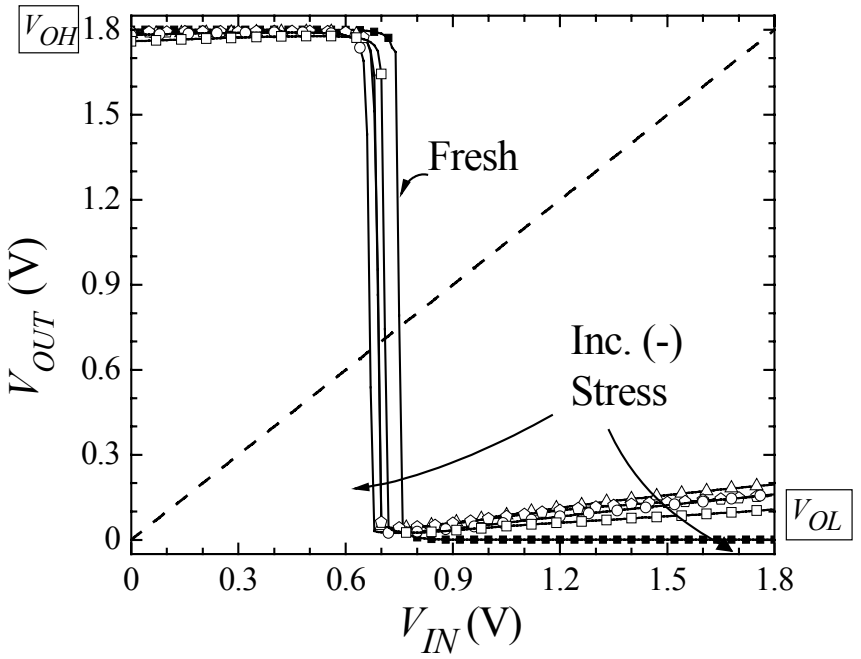
Circuit Stress Induced Breakdown - Inverter

- Inverter voltage transfer characteristics (*VTC*)

Positive Voltage Stress



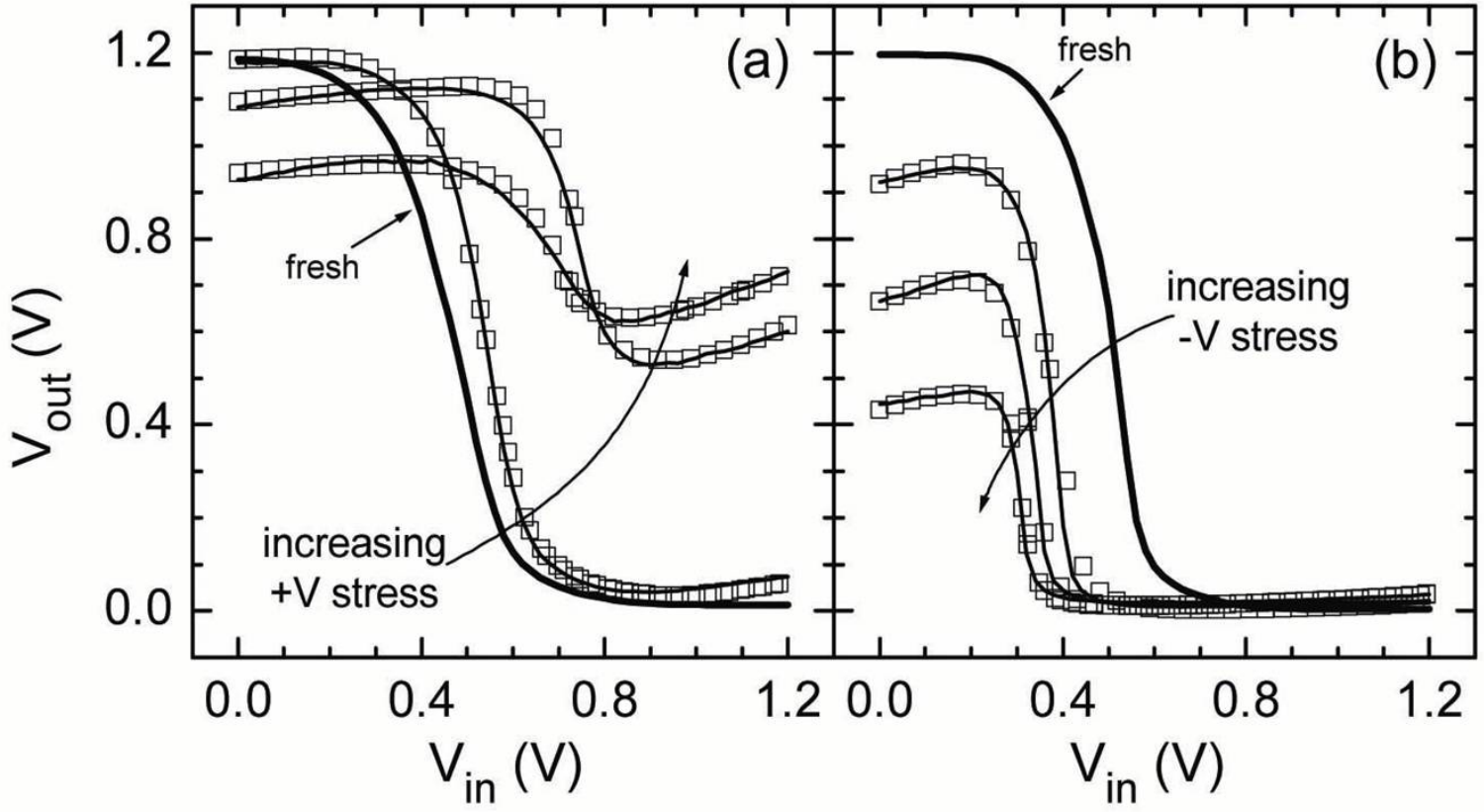
Negative Voltage Stress



■ Fresh △ 8 V ⬠ 10 V ○ 12 V □ 14 V

VTC – Comparison of Only Other Publication

- Inverter voltage transfer characteristics (*VTC*)



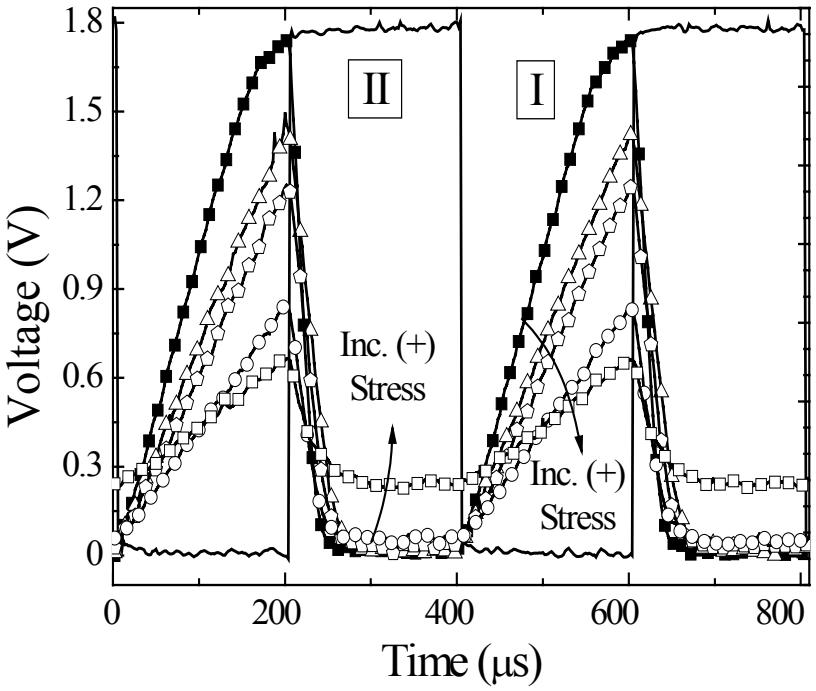
- What about time domain?
- Individual MOSFETS?

[1] J.H. Stathis, R. Rodriguez, B.P. Linder, "Circuit Implications of Gate Oxide Breakdown," *Proceedings WoDIM*, 2002.

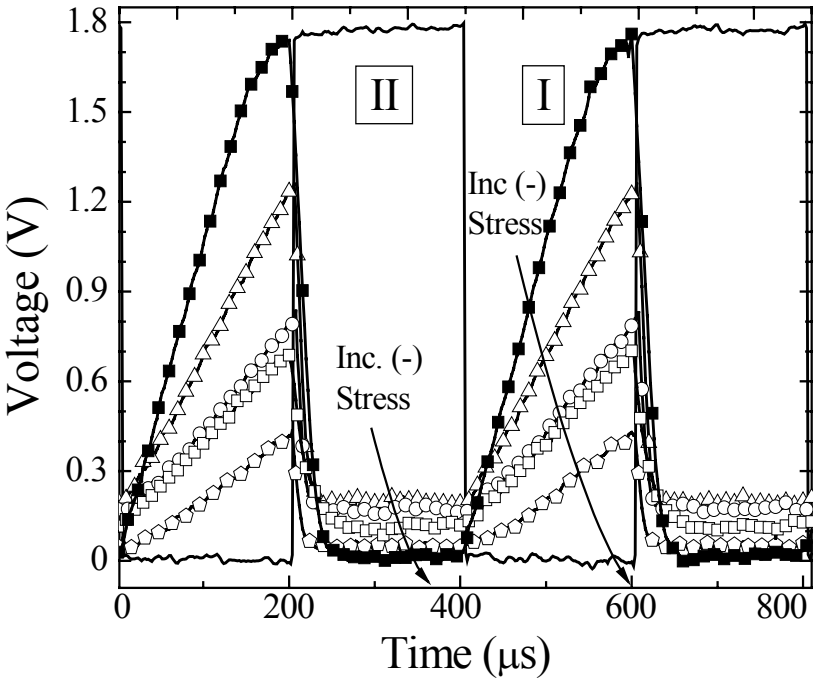
Circuit Stress Induced Breakdown - Inverter

- Inverter voltage-time domain (*V-t*) response

Positive Voltage Stress



Negative Voltage Stress



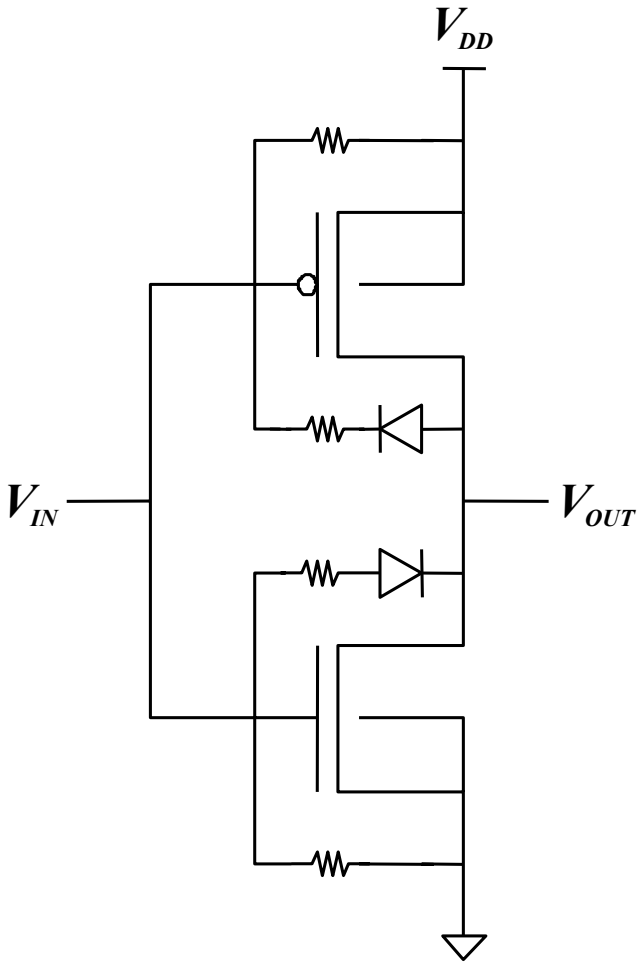
■ Fresh △ 8 V ⬠ 10 V ○ 12 V □ 14 V

Circuit Implications

Problem	Consequence
Increased off-state leakage current	✓ Increased power consumption[1] ✓Circuit failure (>1 billion transistors on a chip)
Increased gate leakage current	✓ Loading of circuit stages[1]
Increased rise/fall/delay times	✓ Timing issues in high-speed circuits[1]

[1]R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS: Circuit design, layout, and simulation," IEEE Press, 1998.

Circuit Model



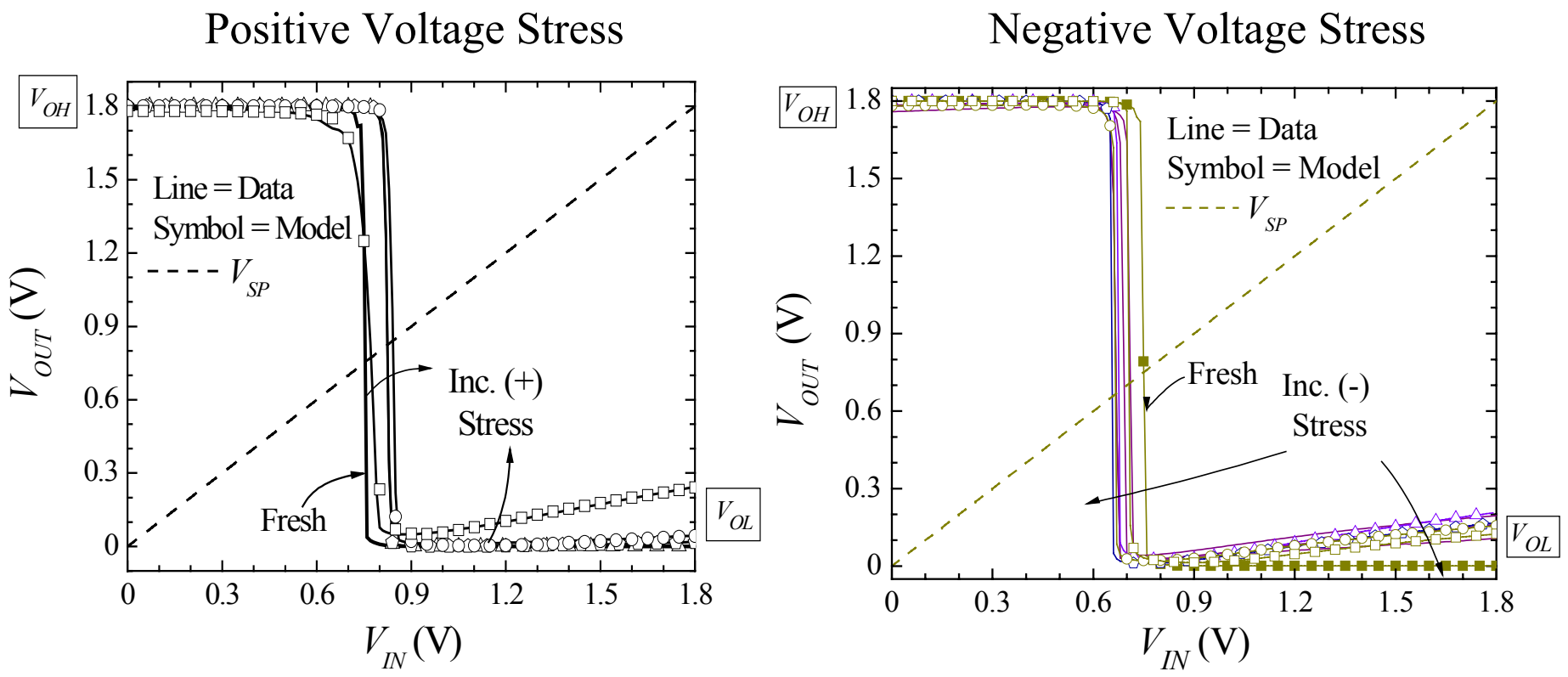
- Circuit elements
  - ✓Resistor-diode pairs
    - Connected from gate-drain
  - ✓Resistors
    - Connected from gate-source
  - ✓Diode emission equation[2]
    - $I_D = I_S \cdot [\exp(V_D / N \cdot V_t) - 1]$
    - I_S (saturation current), V_D (diode voltage), N (emission coefficient), V_T (thermal voltage)
- MOSFET threshold voltage (V_{th})

[1]T.-S. Yeoh et al, ICSE, Bangi, Malaysia, 1998.

[2] R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS: Circuit design, layout, and simulation," IEEE Press, 1998.

Data Vs Model

- Inverter voltage transfer characteristics (*VTC*)



Conclusion

- Circuit level stress
  - Determine degradation in individual devices
  - Ability to connect device degradation to circuit degradation
- VTC measurements may show negligible inverter degradation
  - Suggests Oxide degradation effects in Inverters <u>are not</u> a reliability issue
- Time-domain behavior may be severely degraded!
  - Suggests Oxide degradation effects in Inverters <u>are</u> a reliability issue
- V-t data introduces another characteristic for digital circuit reliability
  - Need for more suitable reliability criterion[1-3]

Study suggests that the time domain is the more suitable criteria

[1]J. H. Stathis et al, WoDim, 2002. [2]J. H. Stathis et al, IEDM, pp. 167-169, 1998. [3]B. Kaczer et al, *IEEE Transactions on Electron Devices*, vol. 49, pp. 500-506, 2002

Future Publications and Work

Betsy J. Cheek, Nate Stutzke, Miles Wiscombe, Terry Lowman, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton

Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics

oral presentation at the 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23, 2003.

Betsy J. Cheek, Student Member, IEEE, Nate Stutzke, Student Member, Santosh Kumar, Member, IEEE, R. Jacob Baker, Senior Member, IEEE, Amy J.Moll, William B. Knowlton, Member, IEEE

Investigation of Gate Oxide Reliability: Consequences of Dielectric Breakdown on MOSFET Characteristics and CMOS Inverter Performance

submitted September 2003 IEEE Transactions on Electron Devices – in review.

- Other SICBBs: *T-gates, current mirrors, etc.*
- Thinner gate dielectrics: *2.1 nm & thinner, high-k* (Cypress & Semitech)
- Determine Trap identity *WRT* Oxide Degradation Mechanism – Penn State
- Interconnect coupling/crosstalk effects on oxides

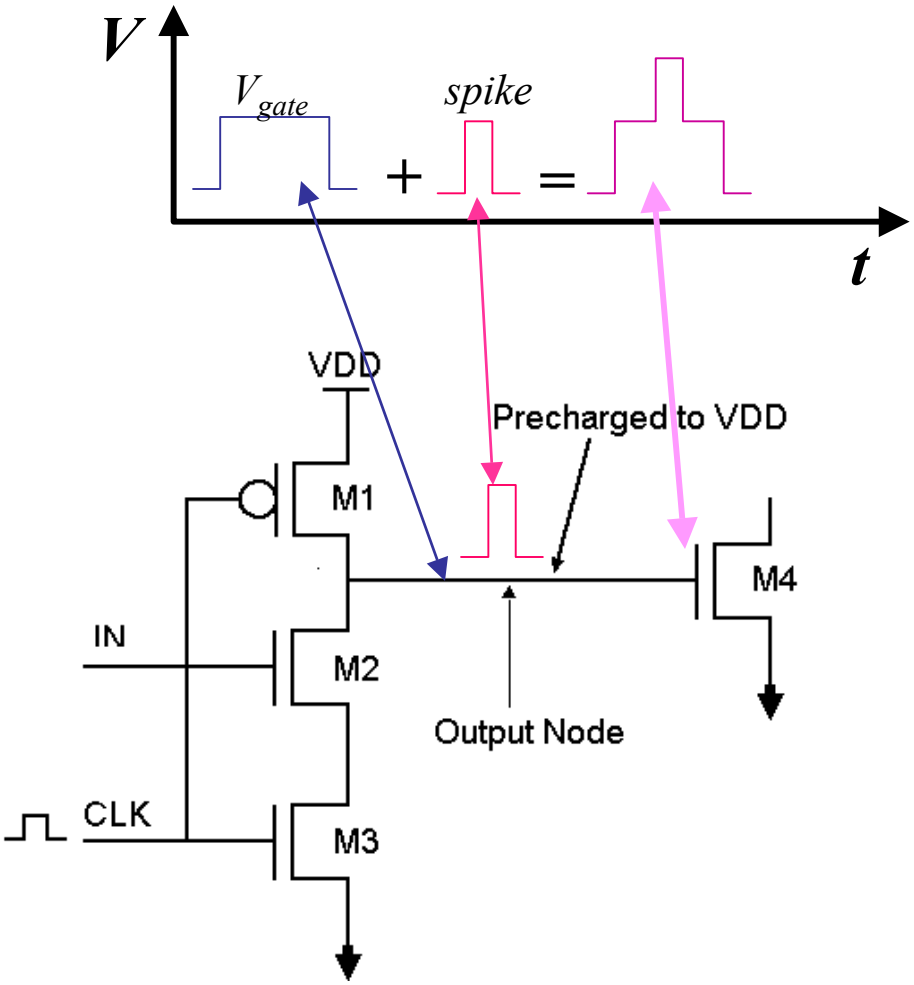
Part II:
Noise in Circuits – Effects on Ultra-Thin Gate Oxide Degradation

Bill Knowlton and Jake Baker

Department of Electrical and Computer Engineering, Boise State University, Boise, ID

Project Definition and Motivation

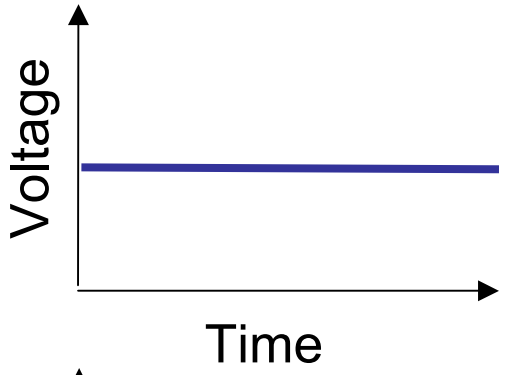
- Investigate the effects of noise in circuits using MWPVS
- Model noise as a voltage spike constructively interfering with a carrier signal due to superposition of waves
  - Noise on signal lines due to:
    - ✓ Electromagnetic radiation (space applications)
    - ✓ Very close interconnect proximity
    - ✓ Capacitive coupling



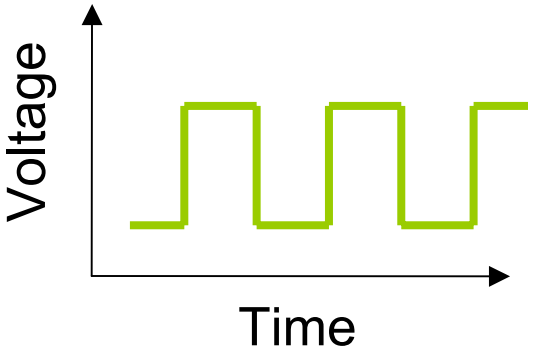
[0]Baker et. al., CMOS: Circuit Design, Layout, and Simulation (Wiley, 1998).

Reliability Test Methods

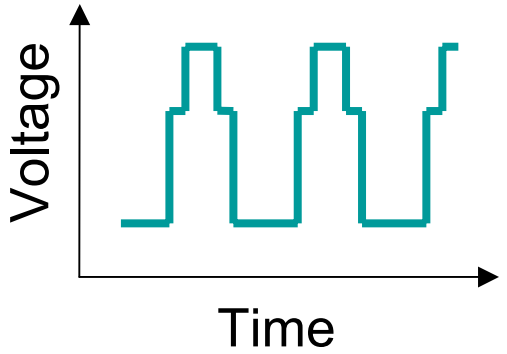
- CVS (constant voltage stress)
  - NOT typical for digital circuit operation



- PVS (pulse voltage stress)
  - Better mimics digital device behavior

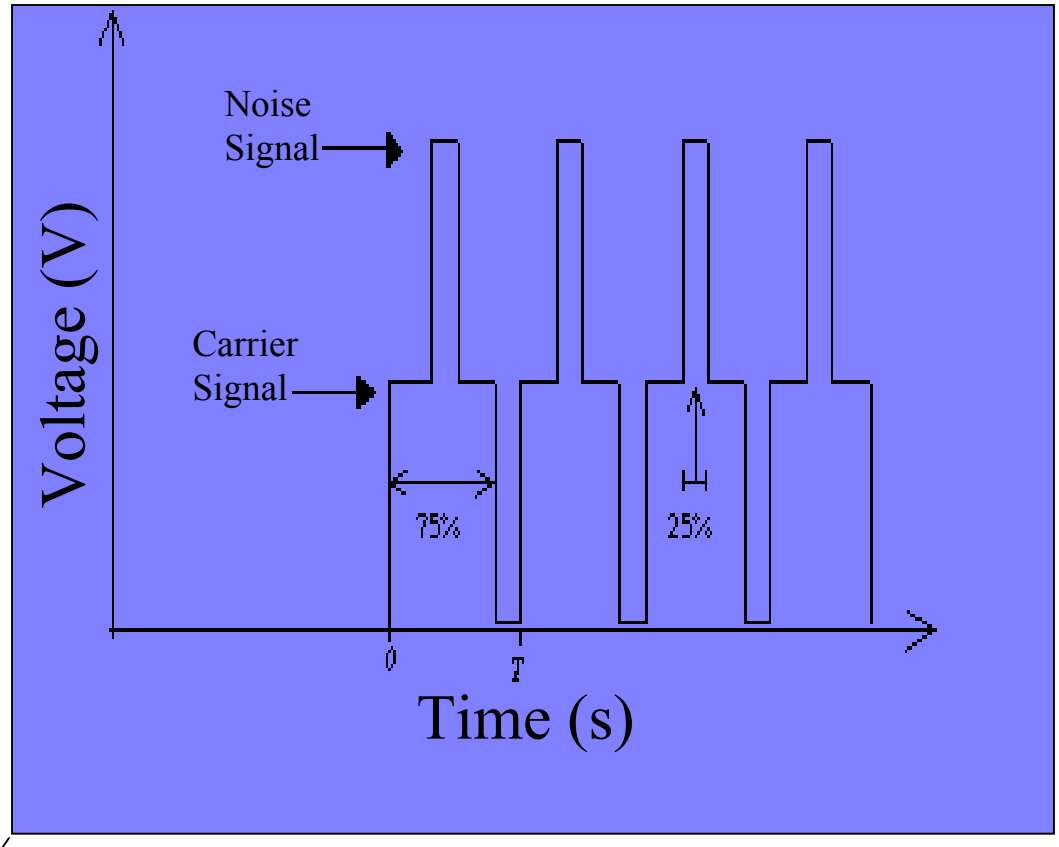


- MWPVS
  - Represents circuit operation with noise

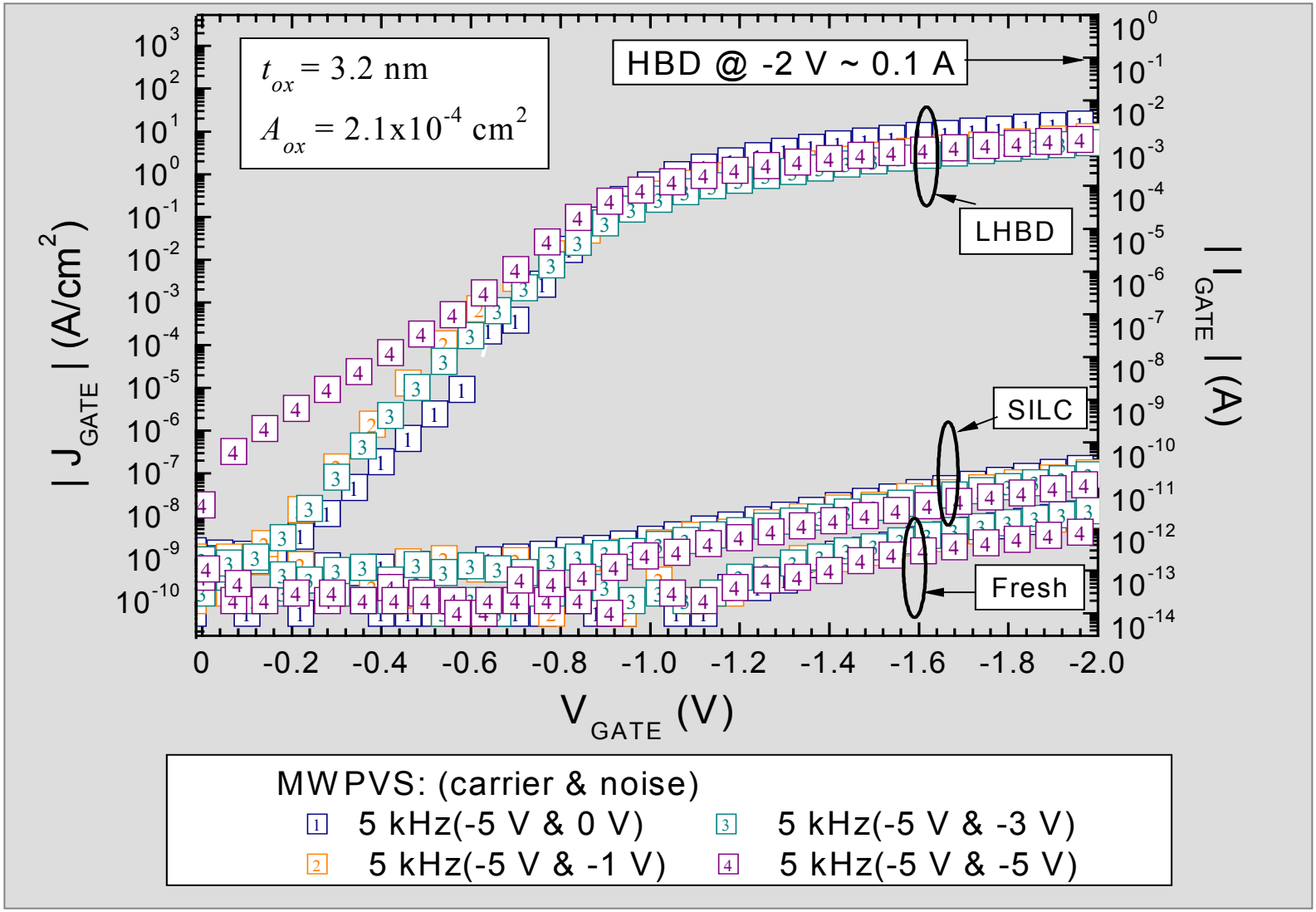


Experimental Setup Continued

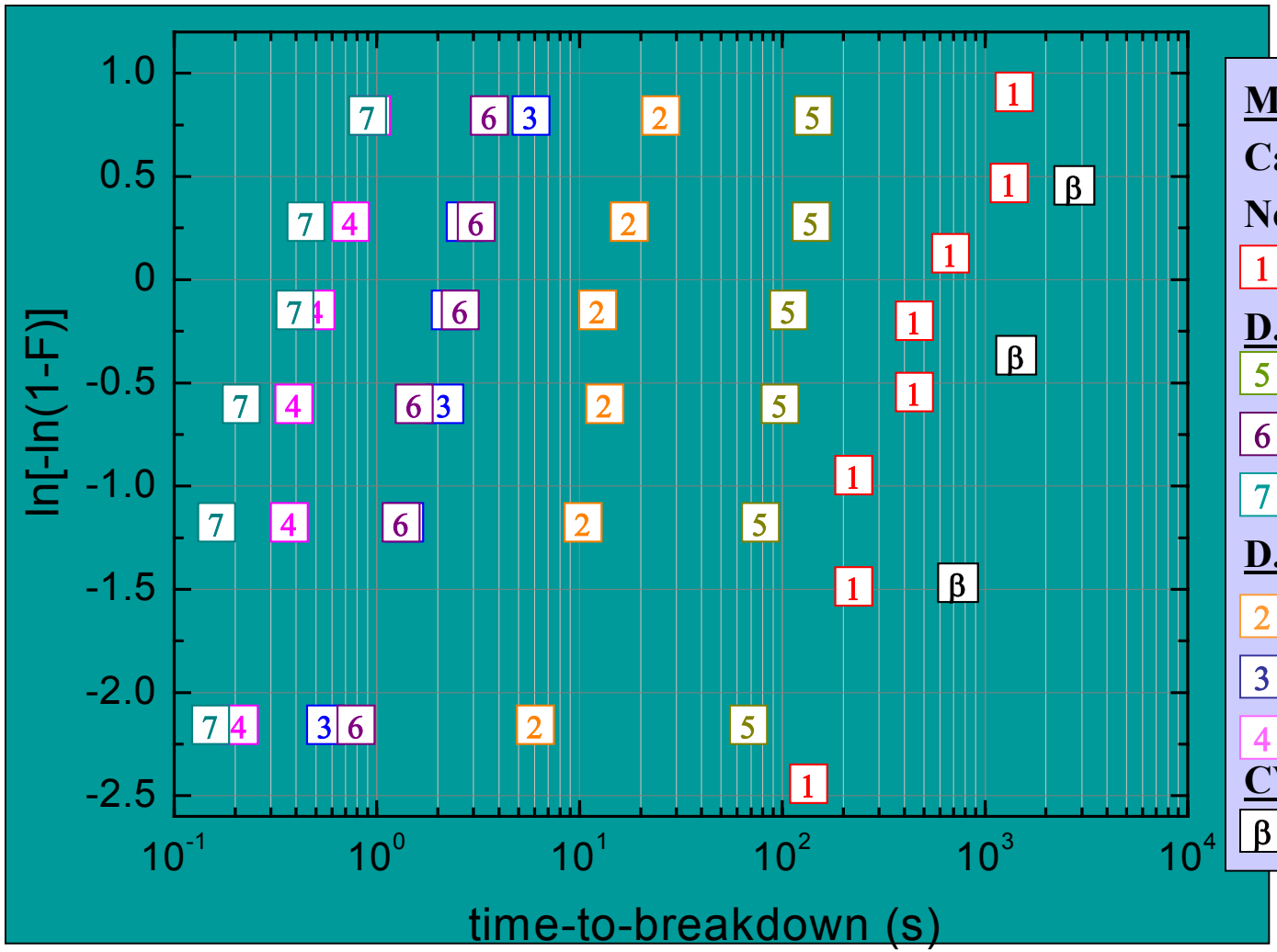
- Combined signals from two Waveform Generators (WFG) programmed with:
  - Frequency
    - ✓ 5 kHz
  - Voltage Amplitude
    - ✓ Carrier Signal: -5 V
    - ✓ Noise Signal: 0 V
      -1 V, -3 V, -5 V
  - Duty Cycle
    - ✓ Carrier Signal: 75 %
    - ✓ Noise Signal: 5 % & 25 %



I_G-V_G Sense Results



MWPVS Weibull Distribution



MWPVS: 5 kHz

Carrier signal: –5 V

Noise signal:

1 0 V (baseline)

D. C. 5 %:

5 –1 V

6 –3 V

7 –5 V

D. C. 25 %:

2 –1 V

3 –3 V

4 –5 V

CVS:

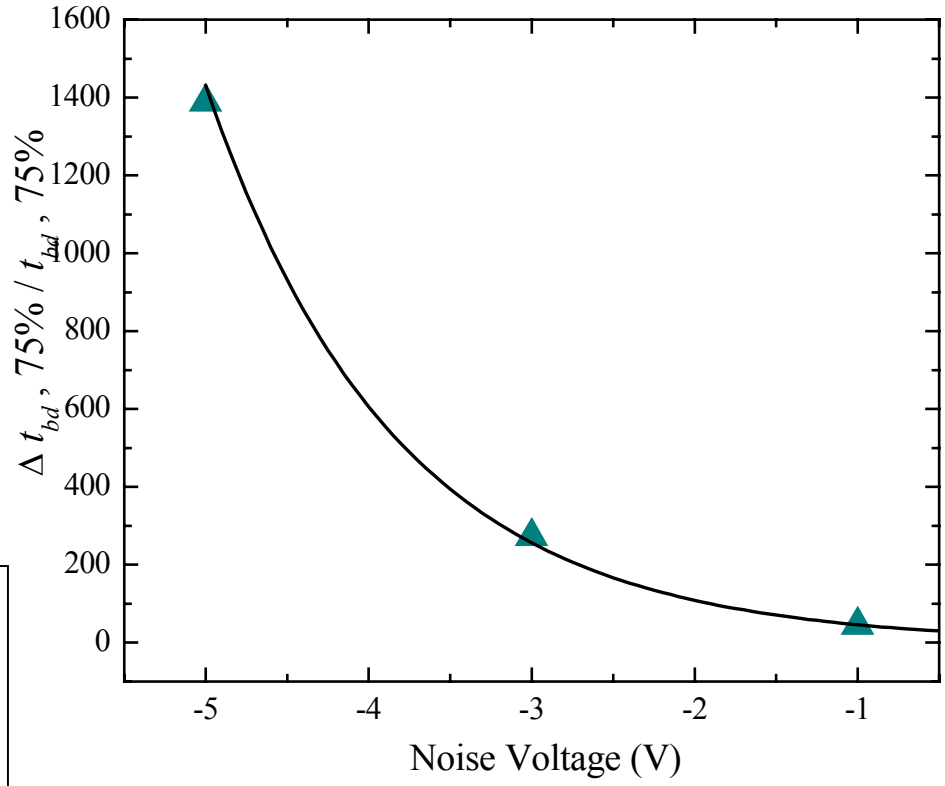
β –5 V

Preliminary Noise Model for MWPVS

- Initial data indicates that increasing the noise signal decreases device lifetime exponentially†
  - d, constant proportional to DC_{BASE} of carrier signal
  - d', constant proportional to DC_{SPIKE} of noise signal
  - c, voltage accelerator factor
  - dV, noise amplitude

$$\frac{1}{t_{bd,2}} \approx d \cdot e^{c|V|} + d' \cdot e^{c(|V|+|dV|)}$$

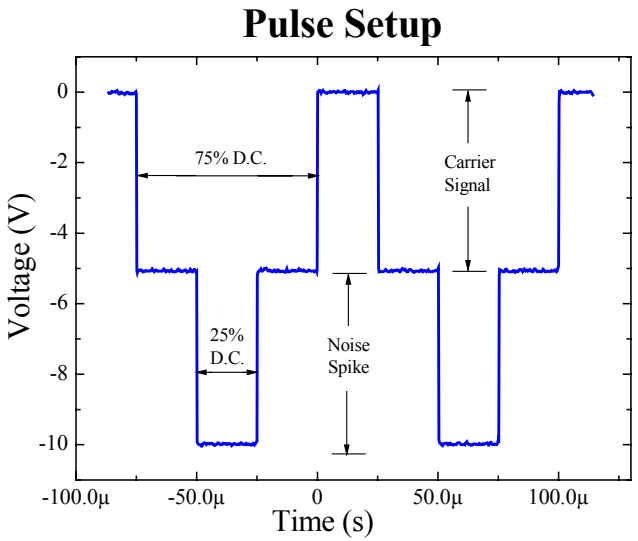
Preliminary noise model for a spike voltage with a DC_{SPIKE} of 20%



†Lawrence, C.E., et al, "Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach", in Proc. of the 15th Biennial IEEE UGIM Symposium, June 30 - July 2, 2003, pp.263-266.

Experimental Setup for MWPVS

- Carrier signal parameters:
  - 20 kHz and 100 kHz frequency (F)
  - 75% duty cycle (DC_{BASE})
  - -5 V base amplitude (V_{BASE})
- Noise signal parameters:



Duty Cycle (DC_{SPIKE})	25 %	
Frequency	20 kHz	100 kHz
Spike Voltage Amplitude (V_{SPIKE})	-1 -3 -5	-1 -3 -5

Devices:
nMOSCAPs
$t_{ox} = 3.2nm$
$A_{ox} = 2.1x10^{-4}\ cm^2$

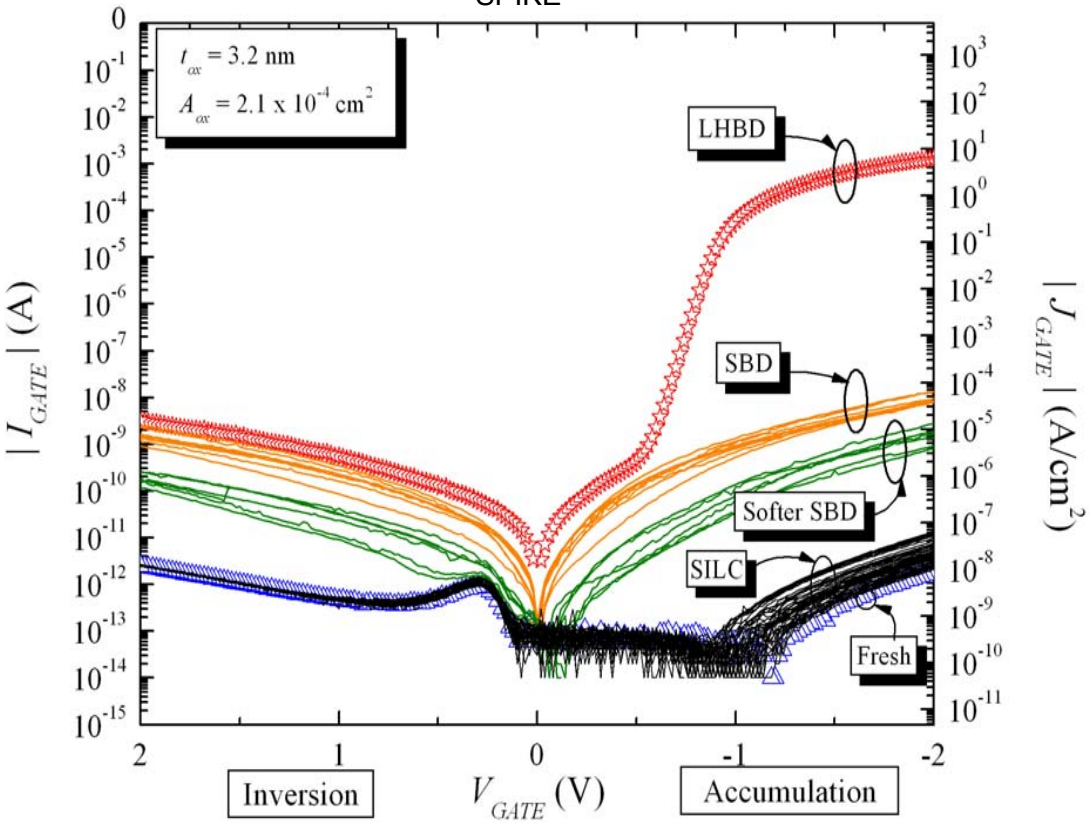
- Stress effects:
  - Monitored through gate leakage current (I_{GATE}-V_{GATE})
  - End test when leakage current reaches ≈ 1 mA (Limited Hard Breakdown)[1-2]

[1]B. P. Linder et al, *VLSI Technology Digest of Technical Papers*, pp. 214-215, 2000.
[2]W. B. Knowlton et al, Proc. of the IRW, pp. 87-88, 2001.

Experimental Results

- Pre- and post- MWPVS I_{GATE}-V_{GATE} results:
  - Degradation mechanisms observed
    - ✓ SILC (Stress Induced Leakage Current)[3-4]
    - ✓ SBD and Softer SBD (Soft Breakdown) [5]
    - ✓ LHBD (Limited Hard Breakdown)[2]

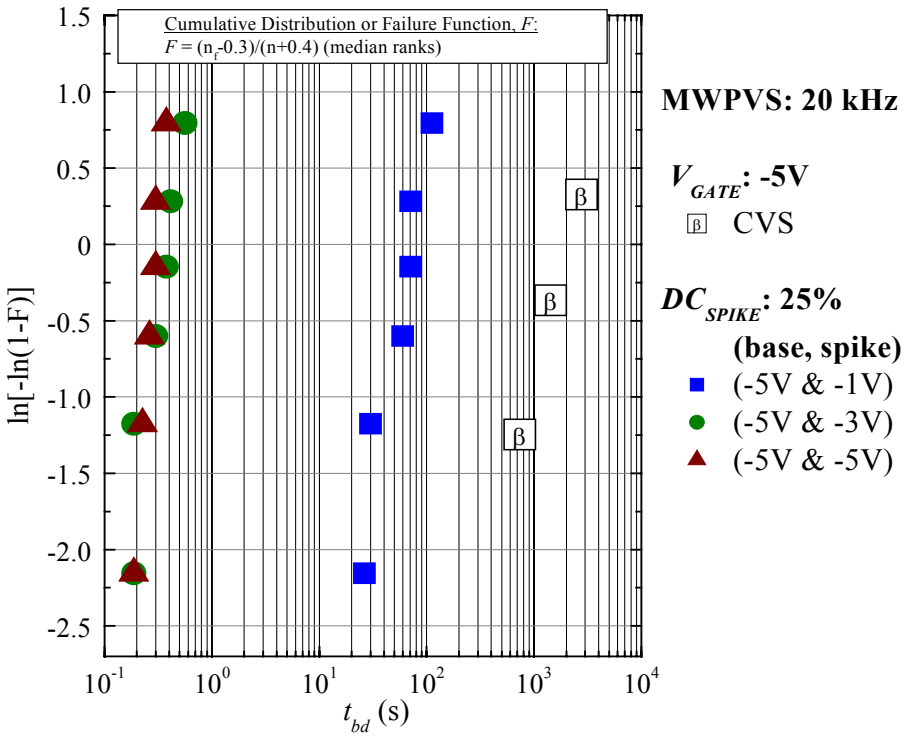
Example of nMOSCAP degradation at V_{BASE} = -5 V, V_{SPIKE} = -1 V, F = 20 kHz, DC_{BASE} = 75%, DC_{SPIKE} = 25%.

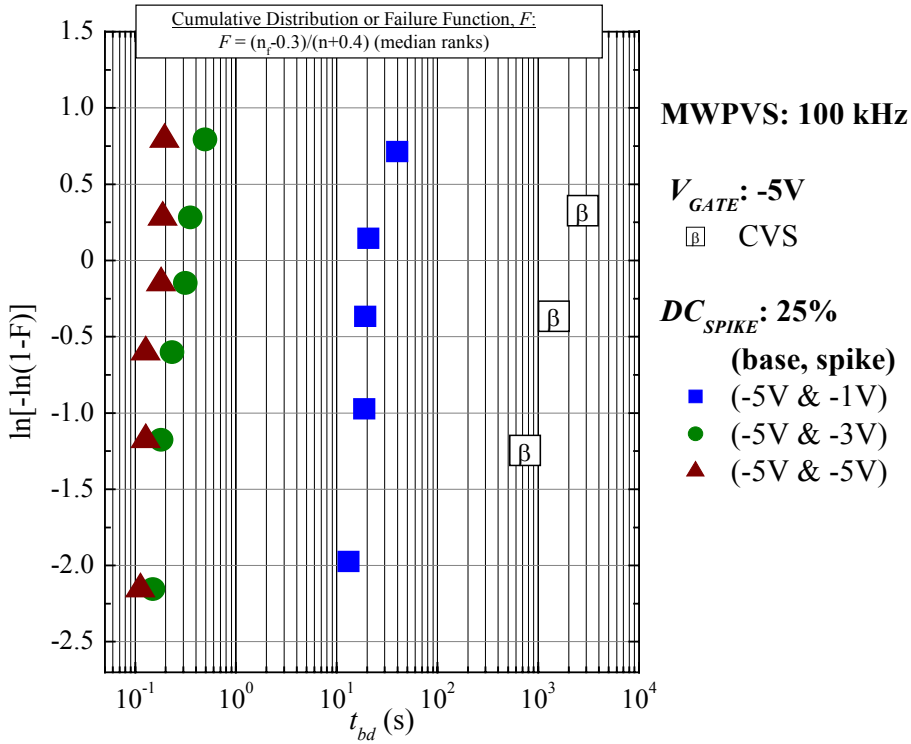


[3]T. N. Nguyen et al, "A new failure mode of very thin (<50Å) thermal SiO2 films," presented at 25th Annual International Reliability Physics Symposium, San Diego, 1987.
[4]P. Olivo, et al, "High-field-induced degradation in ultra-thin SiO2 films," *IEEE Transaction on Electron Devices*, vol. 35, pp. 2259-2267, 1988.
[5]S.-H. Lee, et al, Choi, "Quasi-breakdown of ultrathin gate oxide under high field stress," presented at IEDM Techn. Digest, 1994

MWPVS Vs. CVS

- *Weibull plots* indicate device lifetime decreases by orders of magnitudes when compared to preliminary CVS data





Conclusions

- Designed a MWPVS technique to simulate noise
- Reliability Issues
  - ✓Constructive Interference occurs due Superposition of waveforms
    - o Electromagnetic radiation
    - o Capacitive Coupling
    - o Mixed Signals
- Device lifetime shorter for MWPVS than PVS

Data corresponds to the noise model: Device lifetime exponentially decreases with increase in noise voltage

Future Work

- Further testing of 20 kHz and 100 kHz with PVS method
- Further testing of 20 kHz and 100 kHz with spike duty cycle of 5% with MWPVS method
- Lower Stress Voltage to replicate lower voltages being used in circuits
- Breakdown mechanisms as a function of higher frequency noise
- Accumulation breakdown effects on inversion

Thank You

- Questions?

Traps

The (100) Si/SiO_2 Interface:

Two closely related interface state defects P_{b0} and P_{b1}

SiO_2 Trapping Centers:

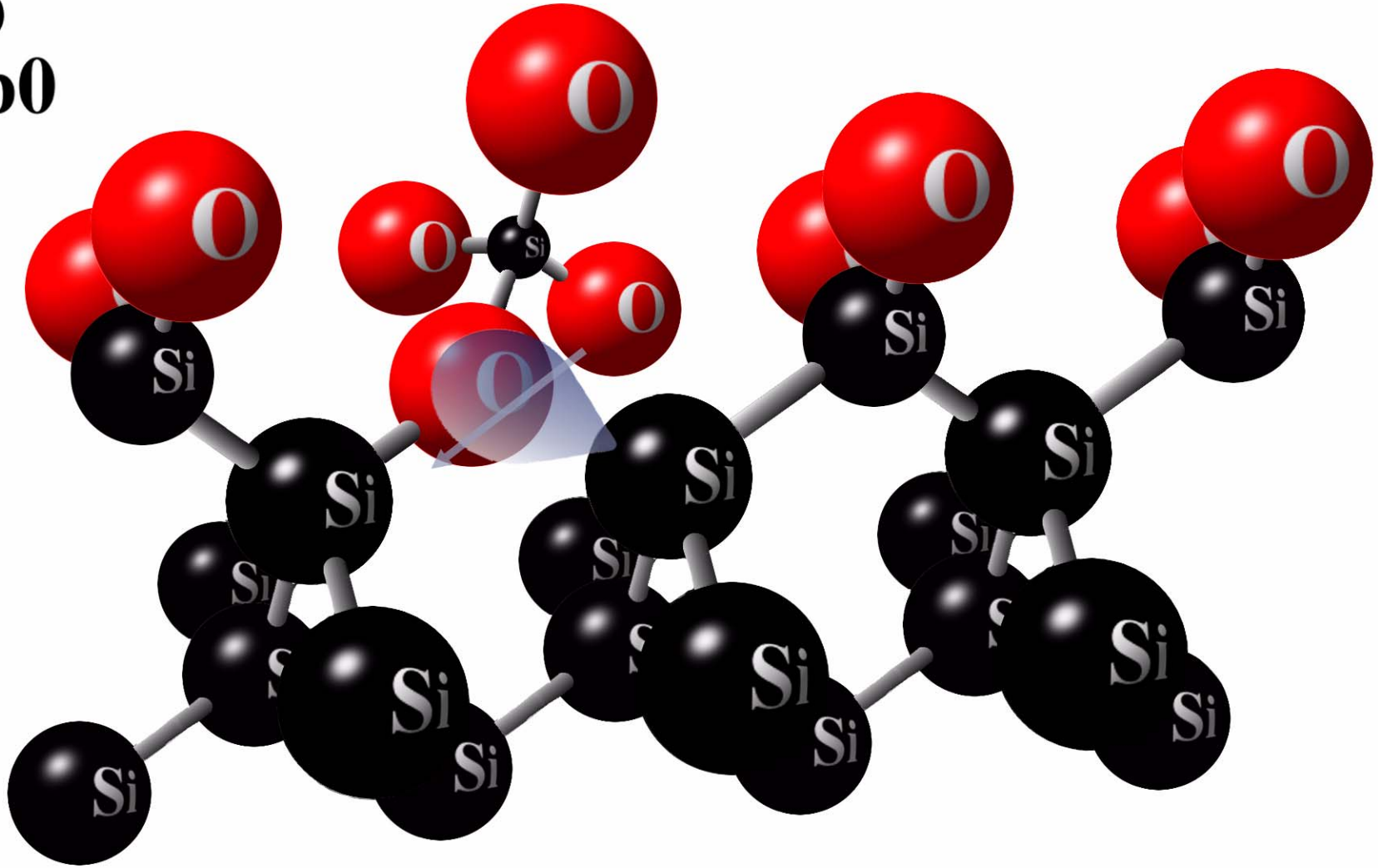
Intrinsic oxygen deficient silicon E' centers (some coupled to hydrogen)

Many extrinsic defects:

We know about these centers from electron spin resonance (ESR) studies.

Courtesy: Patrick Lenahan, Penn State

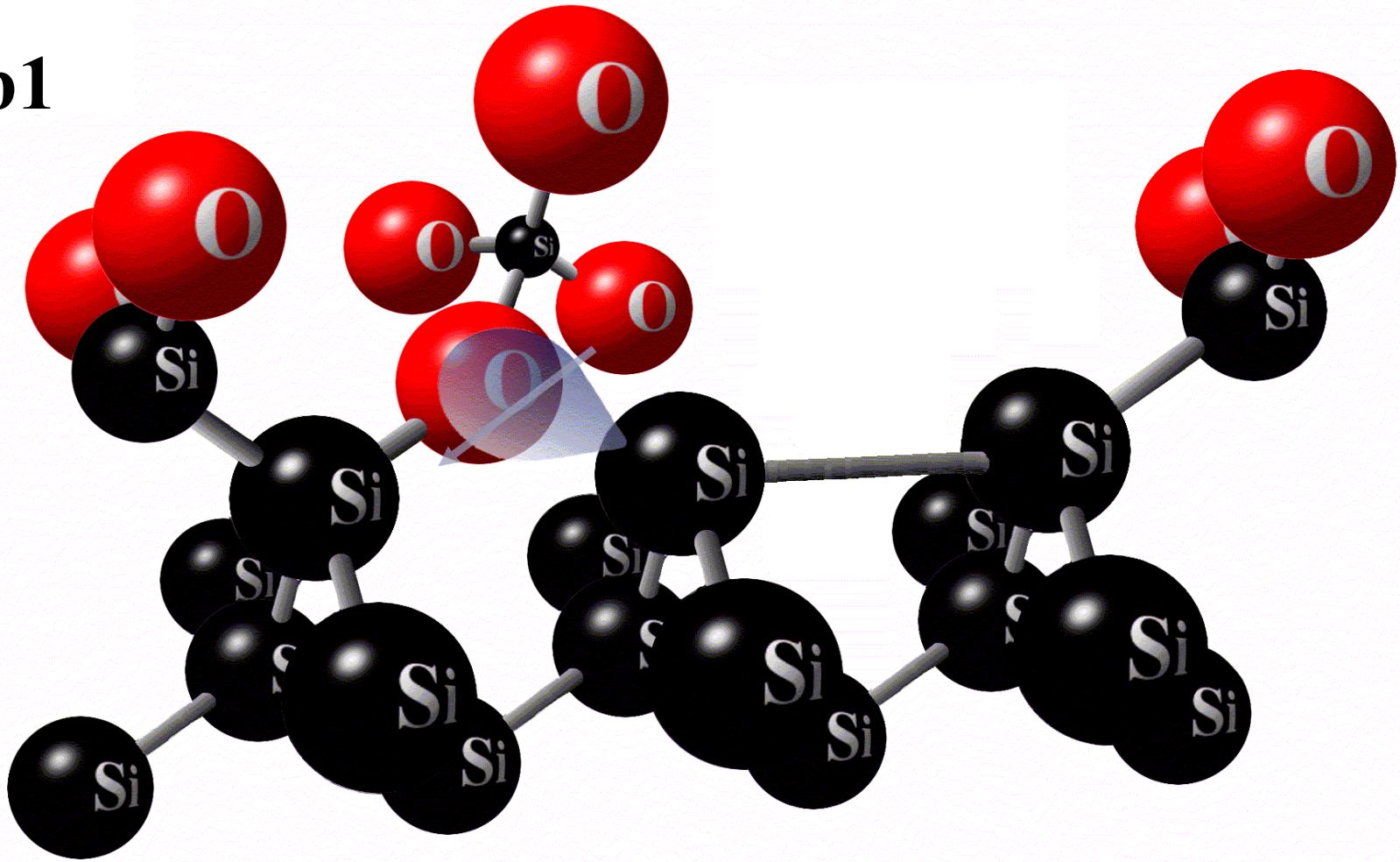
P_{b0}



Courtesy: Patrick Lenahan, Penn State

BOISE

P_{b1}



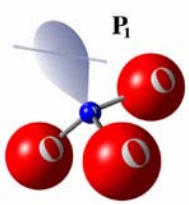
Courtesy: Patrick Lenahan, Penn State

TEOS BPSG Trapping Centers

P1

Spin density decreases with hole injection

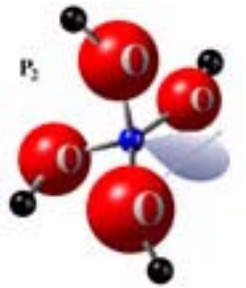
Hole Trap



P2

Spin density decreases with hole injection

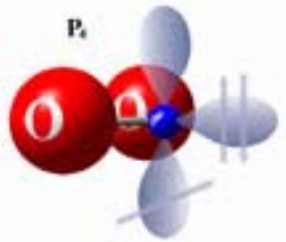
Hole Trap



P4

Spin density decreases with electron injection

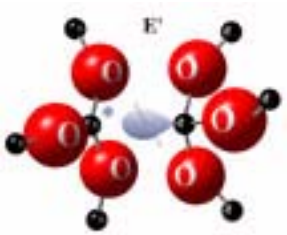
Neutral Electron Trap



E'

Spin density generally increases with hole injection; generally decreases with electron injection

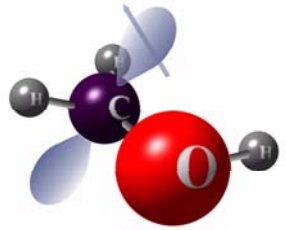
Neutral Hole Trap



Methanol Radical

One of several organic radicals present in these films. Some organic spin densities increase with hole injection other increase with electron injection

Electron and Hole Trap

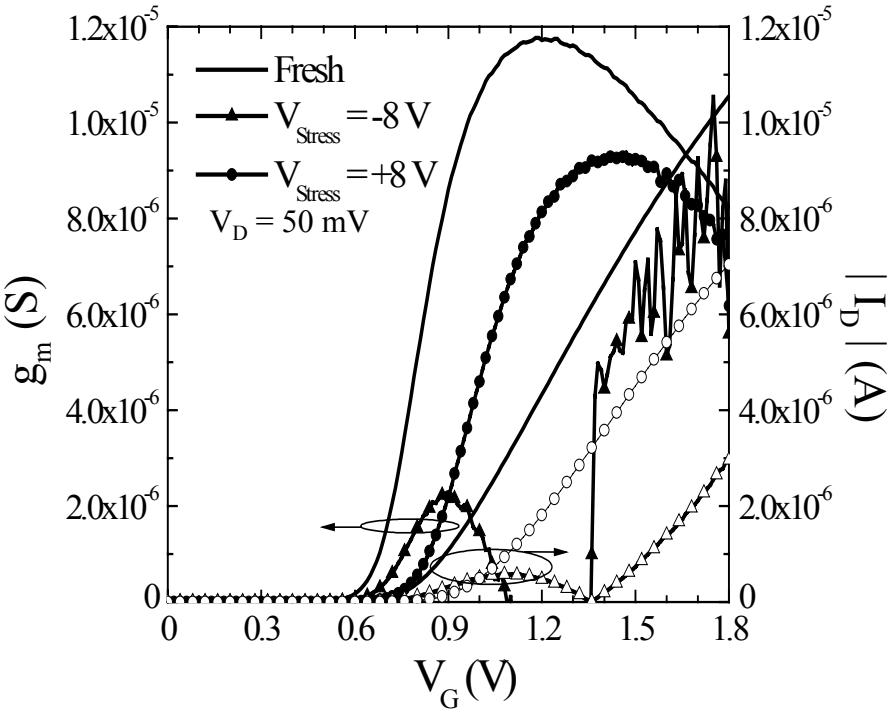


Courtesy: Patrick Lenahan, Penn State

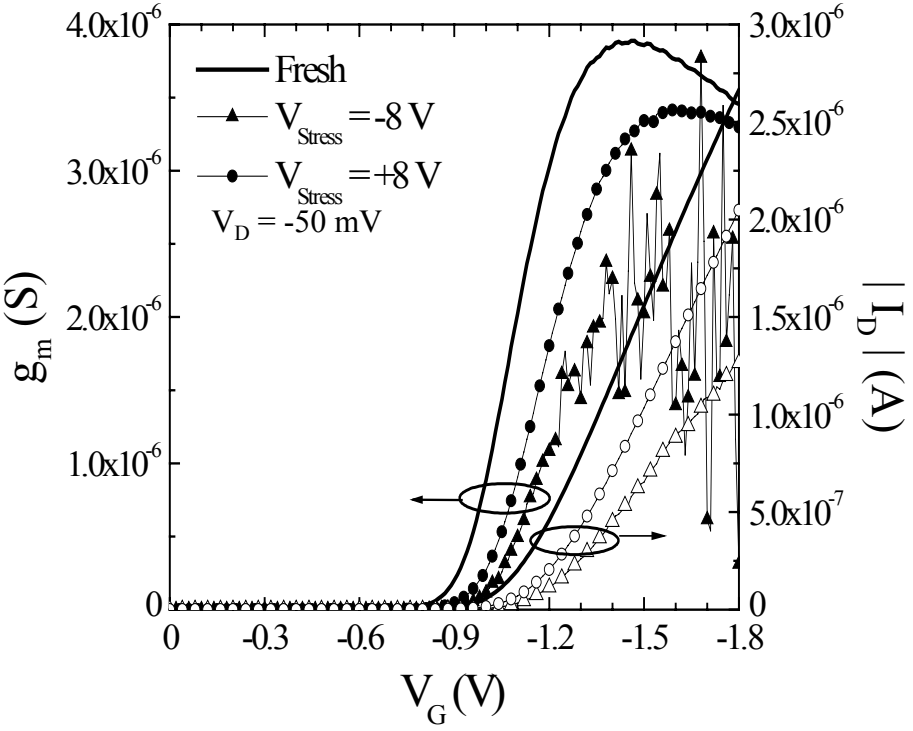
Effects of Dielectric Breakdown

- MOSFET linear I_D-V_G Characteristics

nMOSFET

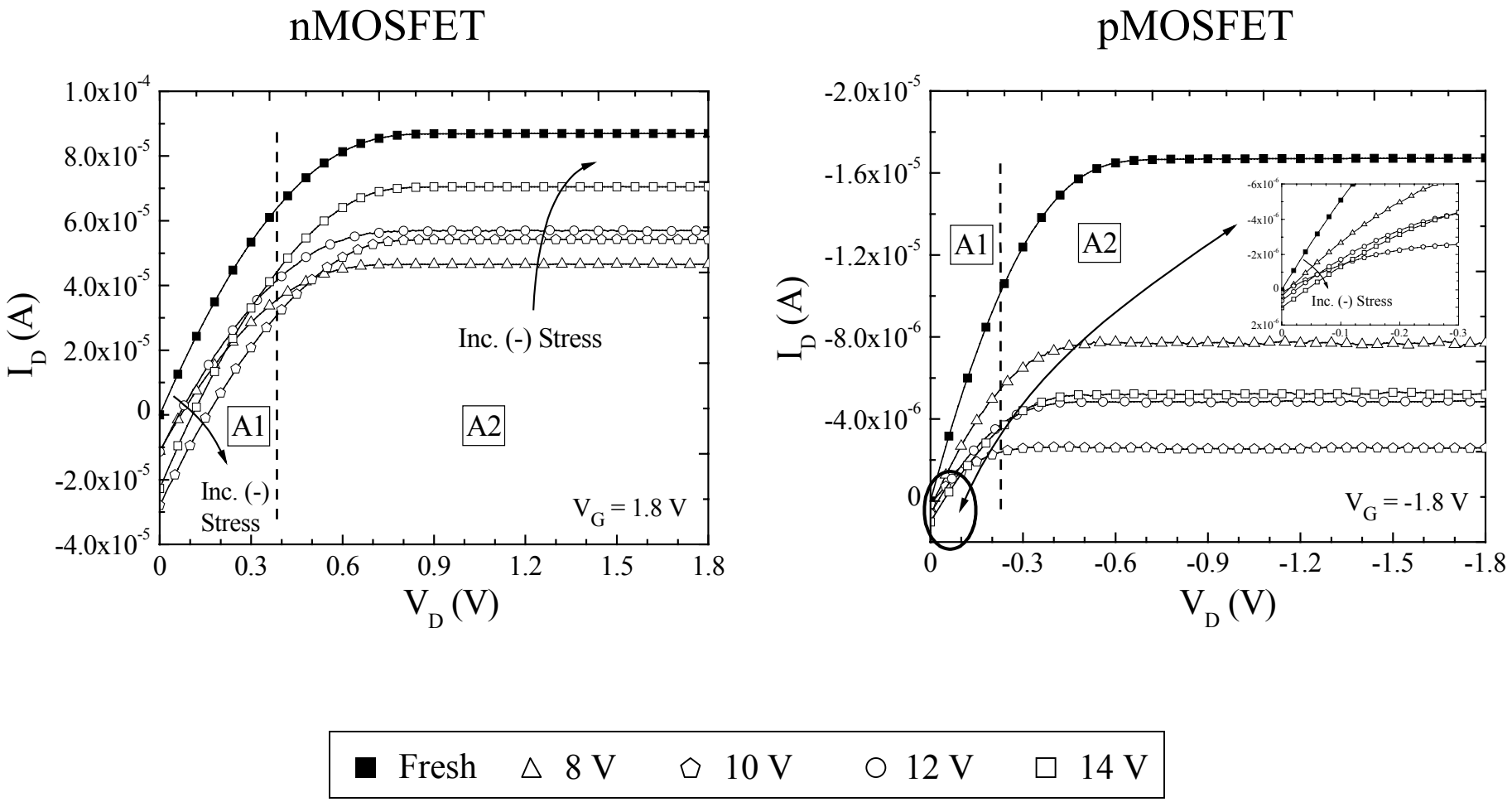


pMOSFET



Circuit Stress Induced Breakdown - MOSFETs

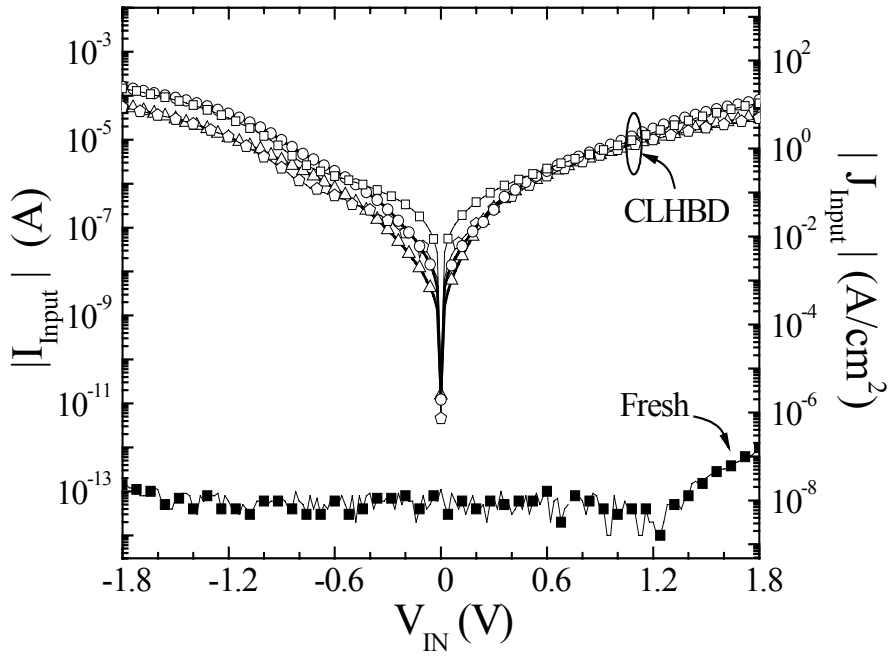
- MOSFET I_D-V_D Characteristics: *Negative voltage stress*



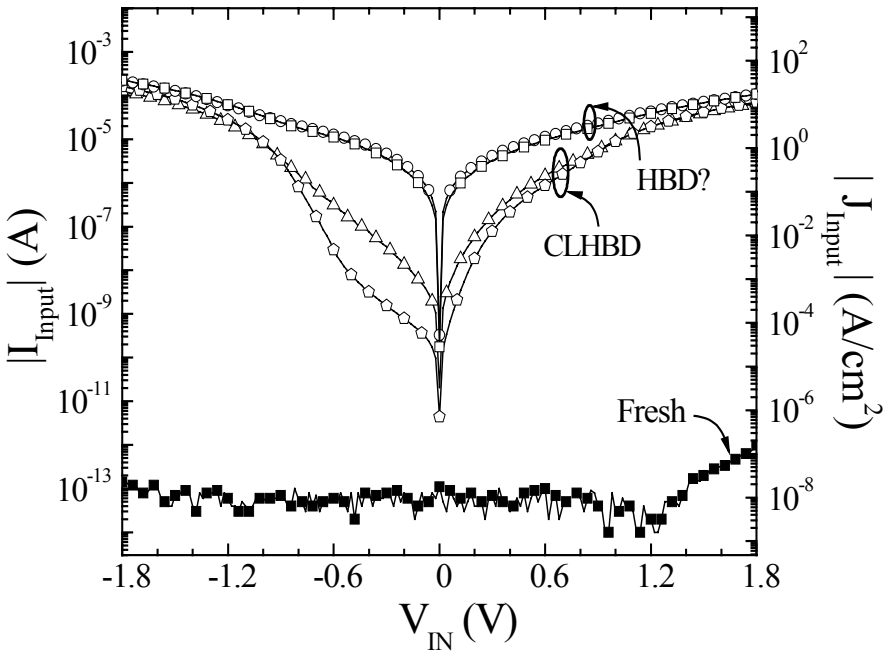
Circuit Stress Induced Breakdown - Inverter

- Inverter *input* leakage current results
  (CLHBD = circuit limited hard breakdown)

Positive Voltage Stress



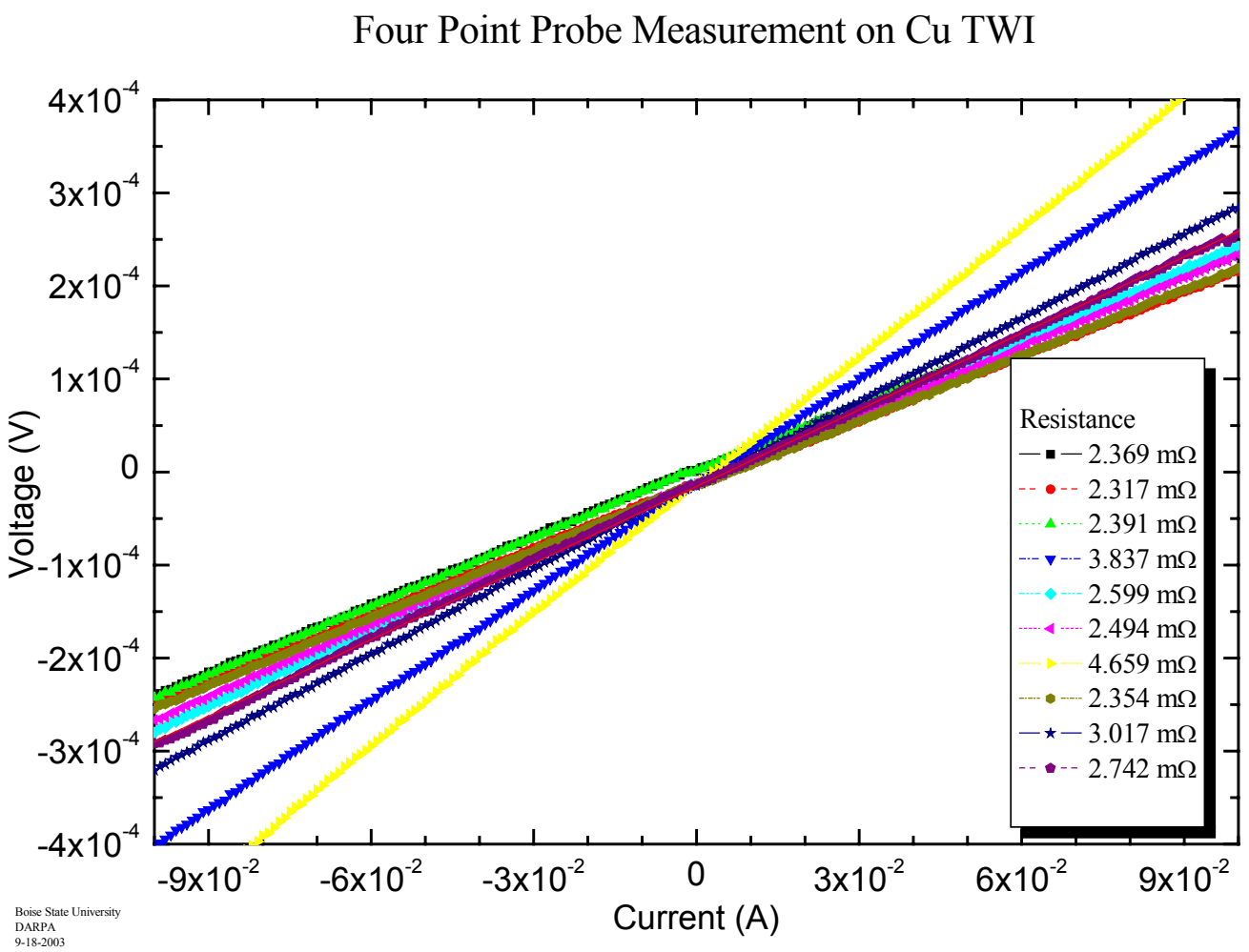
Negative Voltage Stress



■ Fresh △ 8 V ⬠ 10 V ○ 12 V □ 14 V

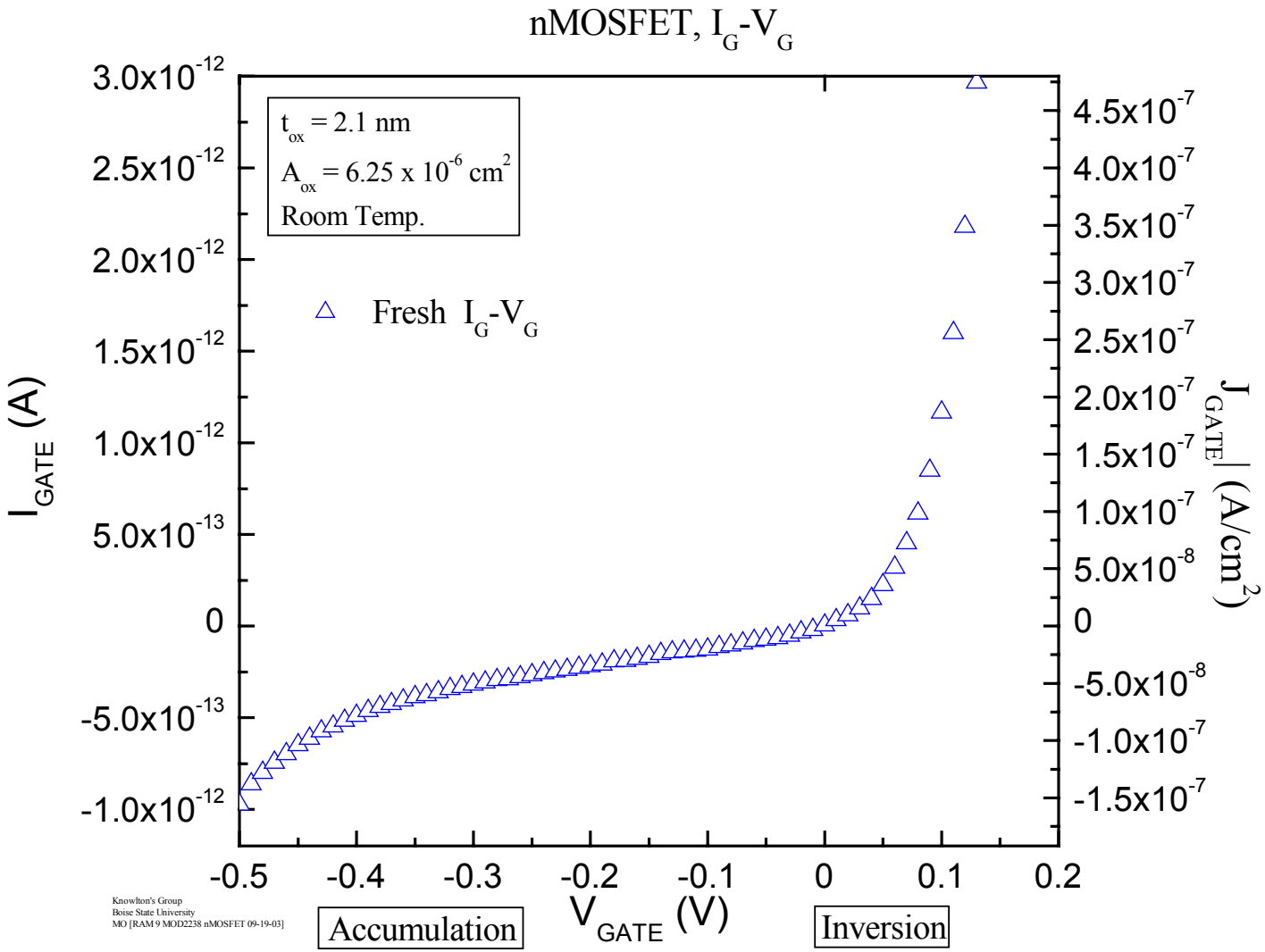
Equipment Capability

- Resistance resolution: *mΩ resolution (Cu vias)*



2.1 nm Gate Oxides

- Tunneling current is Direct



Summary

- What type of oxide degradation has been introduced into the gate oxide to cause these types of VTCs?
  - MOSFET LHBD
  - Inverter CLHBD
    - ✓ Similar to the MOSFET degradation mechanism LHBD
    - ✓ Suggests oxide degradation mechanisms in simple circuits are similar to MOSFETs

- How do the individual devices respond to this type of degradation?
  - Increased off-state leakage current
  - Increased gate leakage currents
  - Decreased g_m, increased V_{th}

Summary

- Importantly, how does this affect the time domain?
  - Reduced output swing
    - ✓ V_{OH} decreases
      - Positive or negative stress
    - ✓ V_{OL}
      - Positive, *increases* with increasing stress
      - Negative, *decreases* with increasing stress
  - Increased rise- and fall-times

- Circuit model
  - Observed both Ohmic and non-Ohmic (exponential) behavior in data
  - Physical Explanation
    - ✓ Resistor = Ohmic
    - ✓ Diode = non-Ohmic
  - Result: Both Positive and negative data fit well