# EM Noise Mitigation in Circuit Boards and Cavities


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# Previous Work and Recent Work

- Developing 3-dimensional full-wave predictive tools for cavity Resonance and S Parameters [Completed]
- Developing fast predictive modeling tools for PCB analysis [Completed]
- Using lossy material coating to reduce aperture radiation [Completed]
- Reduction of coupling between cavities using high-impedance surfaces [Completed]

# Previous Work and Recent Work

- Reducing noise in printed circuit boards using high impedance surface

Previous:

1. Concept development
2. Experimental verification
3. Wideband extension

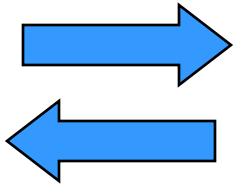
New:

1. Accurate wideband prediction
2. Wideband extension using advanced materials
3. Band gap design
4. Miniaturization

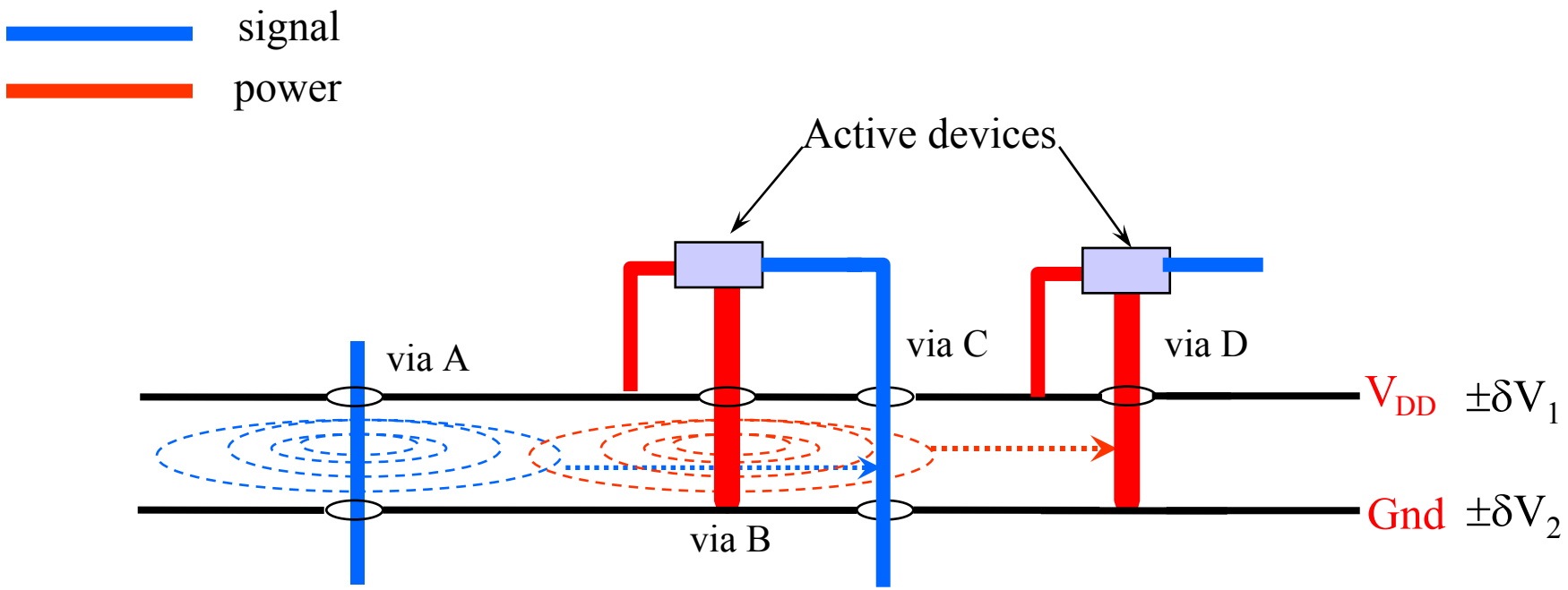
# Reduce switching and other noise in Printed Circuit Boards

# Importance of PCBs

- Everything will be printable!
- Cost
- Compactness
- …

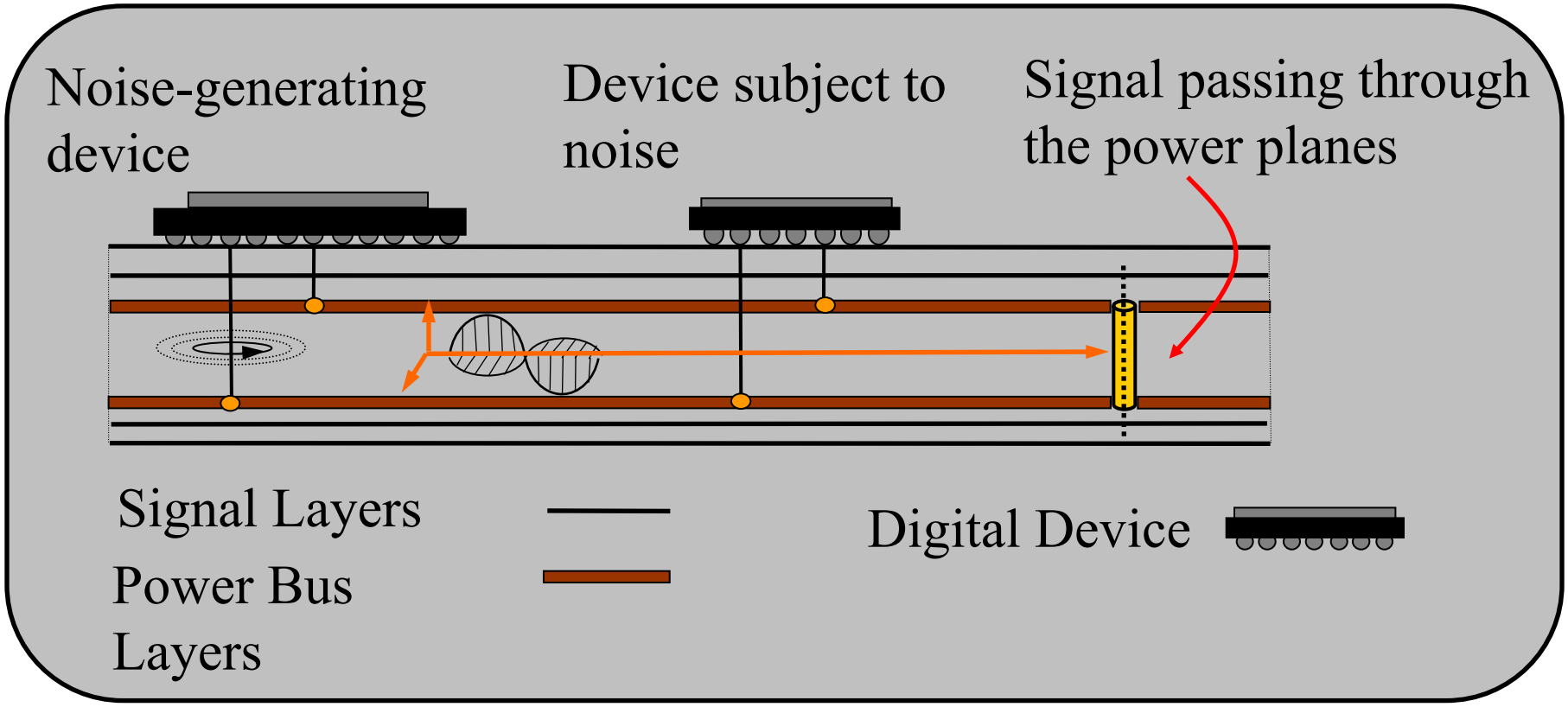
PCB not radiating  immune from external radiation

# EM Noise in PCB



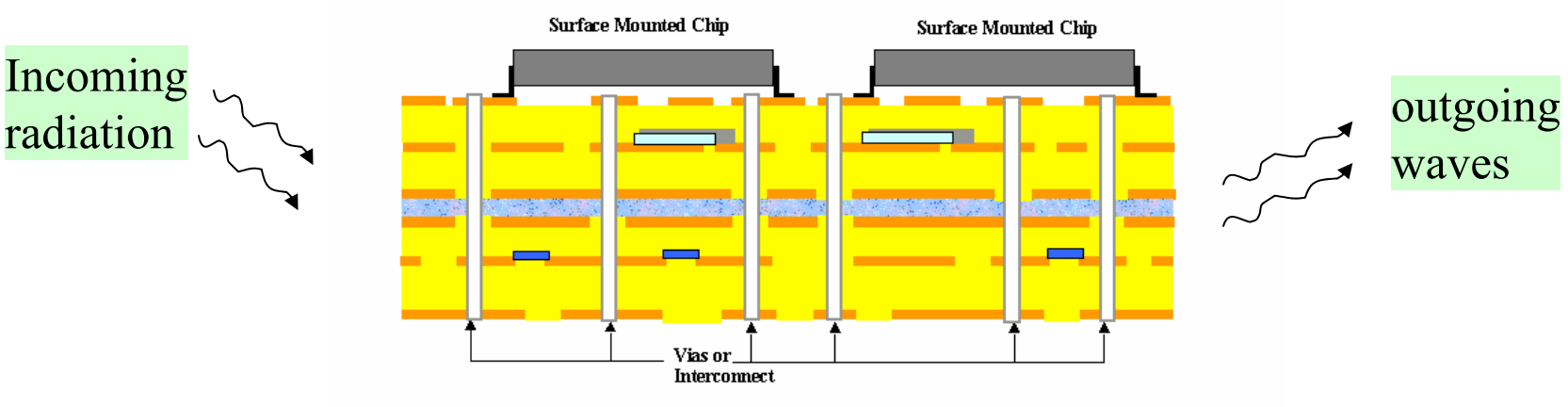
# Motivation

**Problem:** Switching noise ….




- Need to do something for mitigation of noise beyond ~ 500MHz

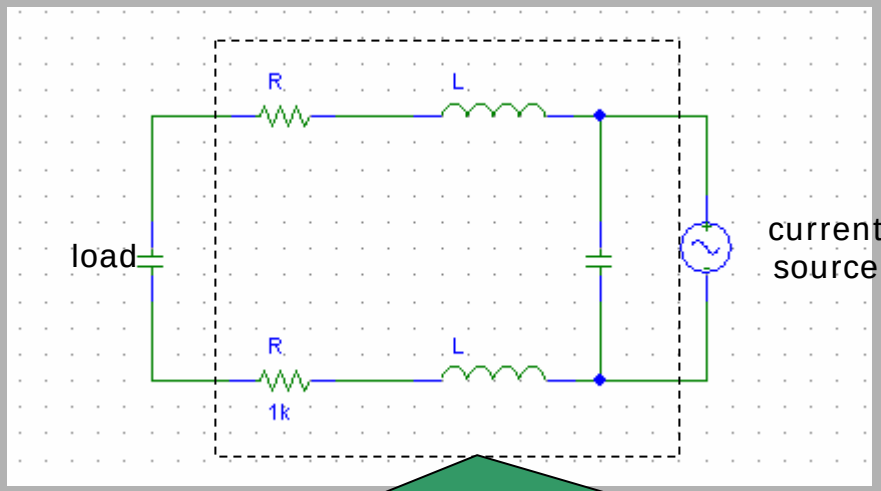
# Coupling to Sensitive Devices in a Multi-Layer Stack up

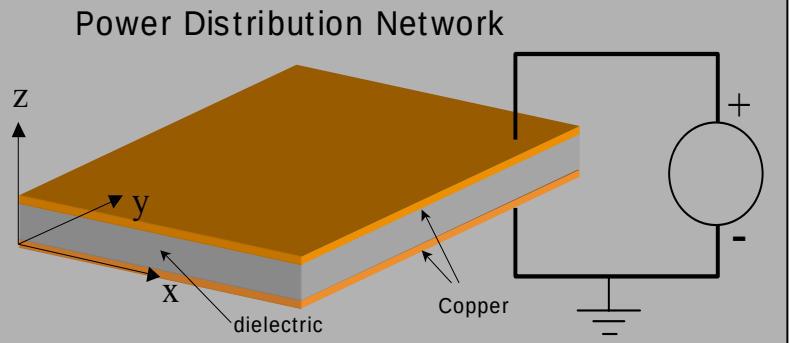


# Problem and Classical Solutions

- Interconnect and Board Inductance

**R-L circuit model for the power plane**

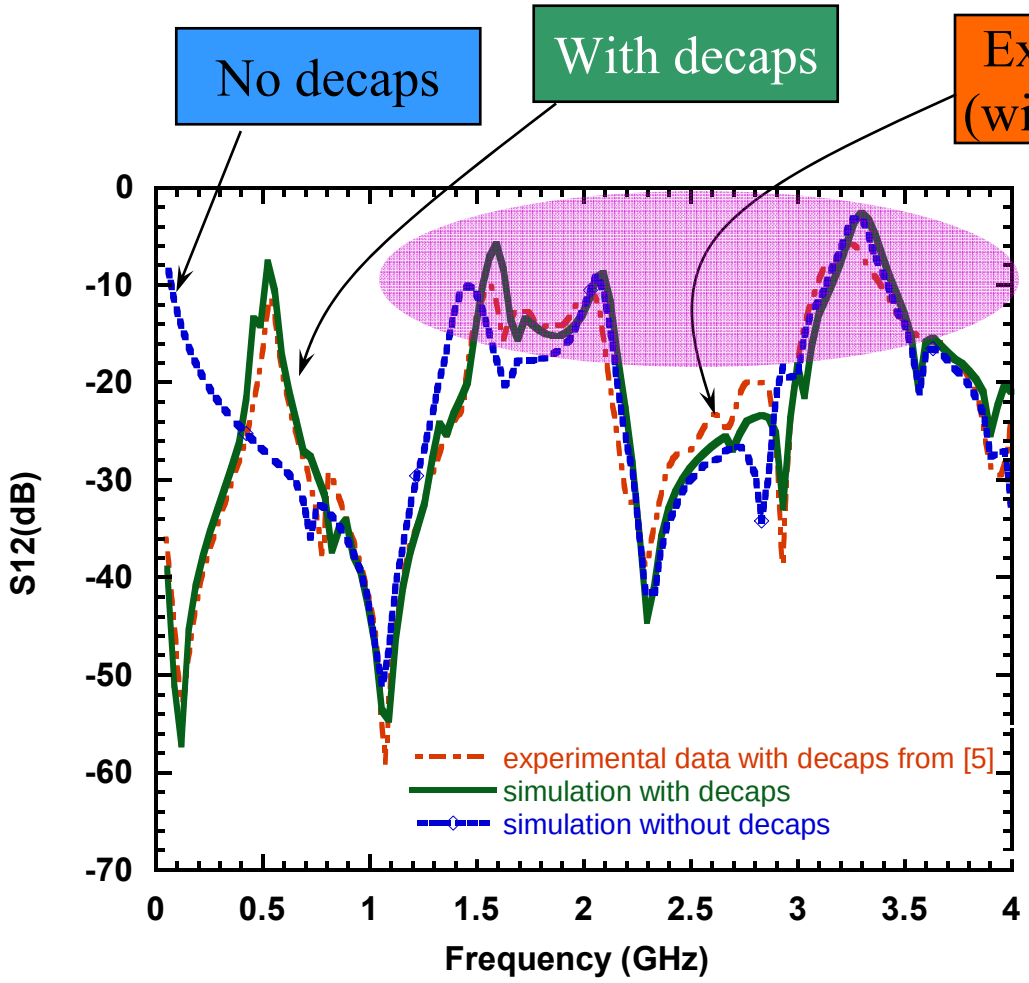


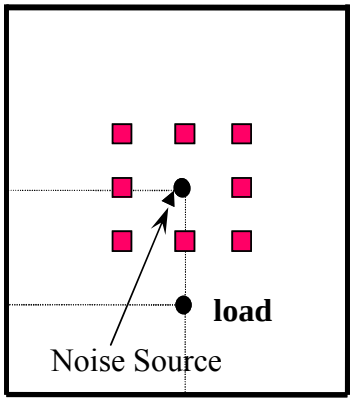




Voltage drop between two points on the board depends on the inductance, L, and resistance R.

$$V_L = L_{eff} \frac{\partial i}{\partial t}$$

# Decoupling Capacitors around Noise Source

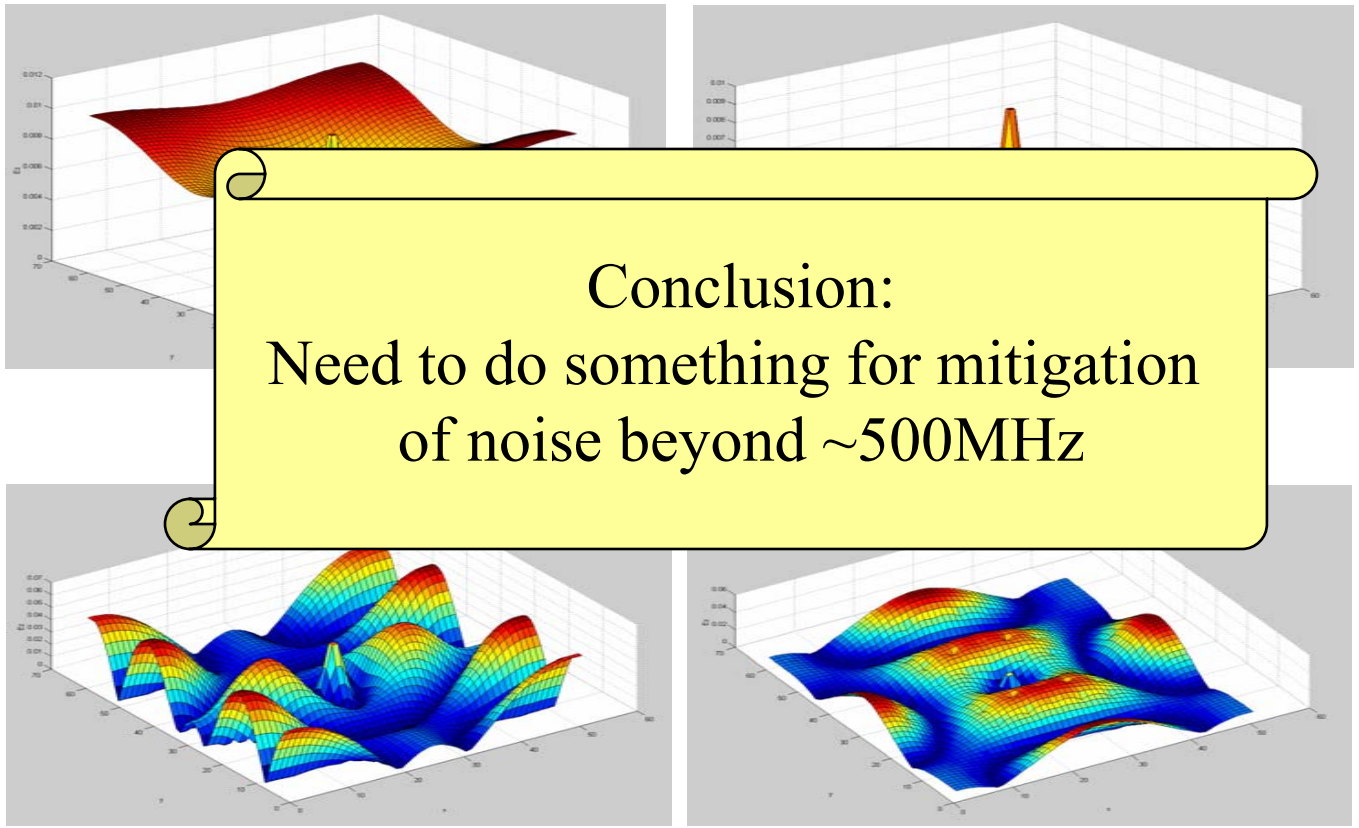



8 decoupling capacitors around noise source:
C=10nF, L=2nH, R=50mΩ

# Classical Methods: Ineffective at Microwave Frequencies

•Effect of Capacitors Placement at **200**MHz and 1GHz



Conclusion:
Need to do something for mitigation of noise beyond ~500MHz

Effective

NOT Effective

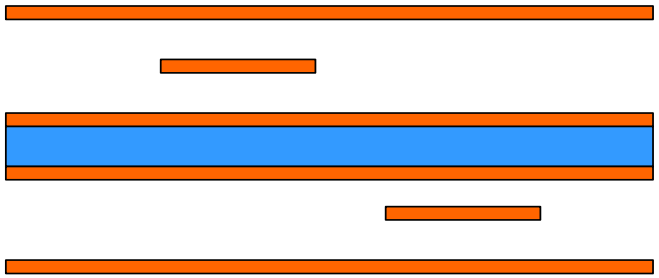
**no caps 1 GHz**

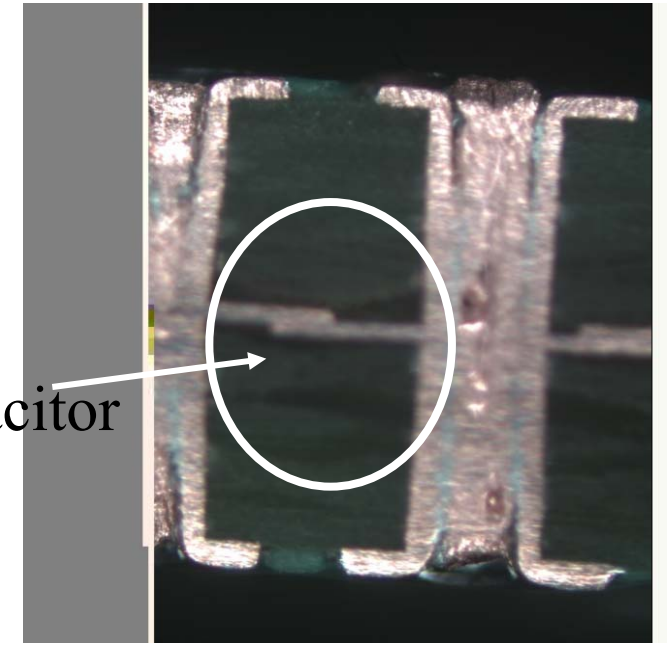
**99 caps 1 GHz**

# Possible Solutions

Embedded ***Capacitors***

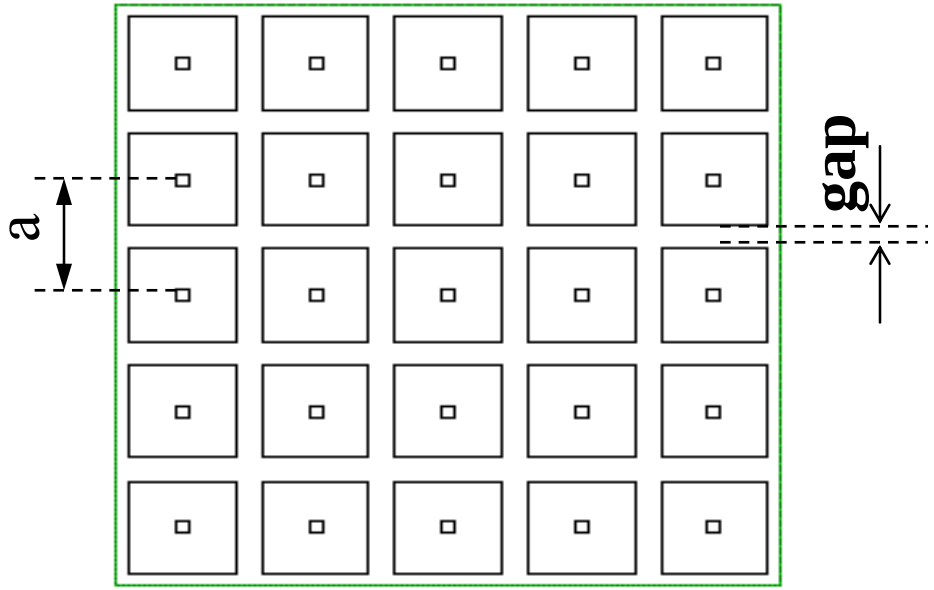
Embedded ***Capacitance***



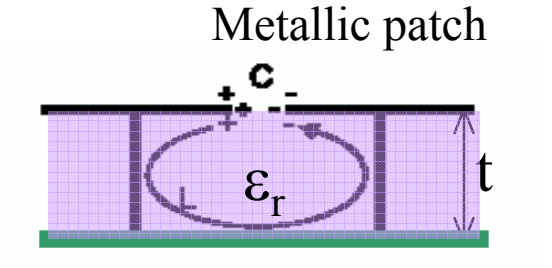


# Electromagnetic Band Gap Structures
## for switching noise mitigation

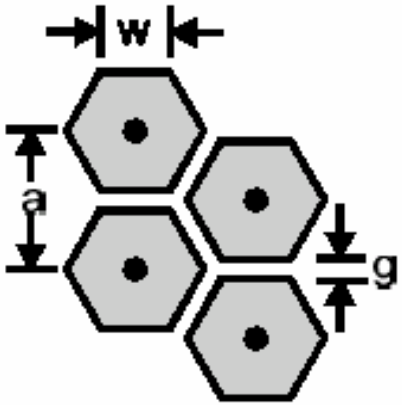
# Electromagnetic Band Gap Structures (EBG) for "Surface" Wave Suppression

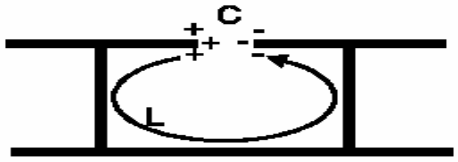


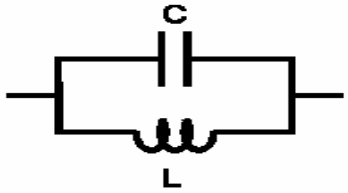

Top view of HIS with square patches

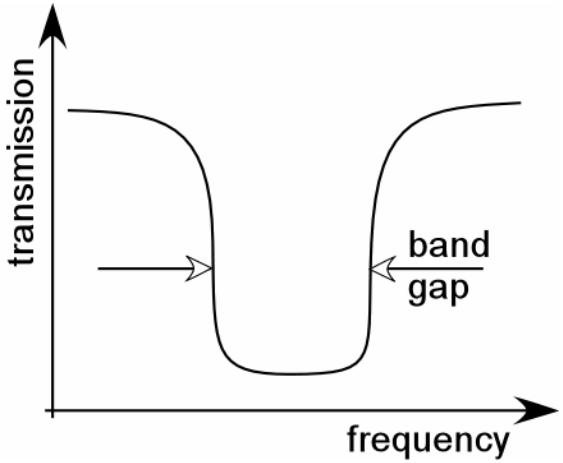


# Interpretation: EBG as a Series of Parallel LC Resonators



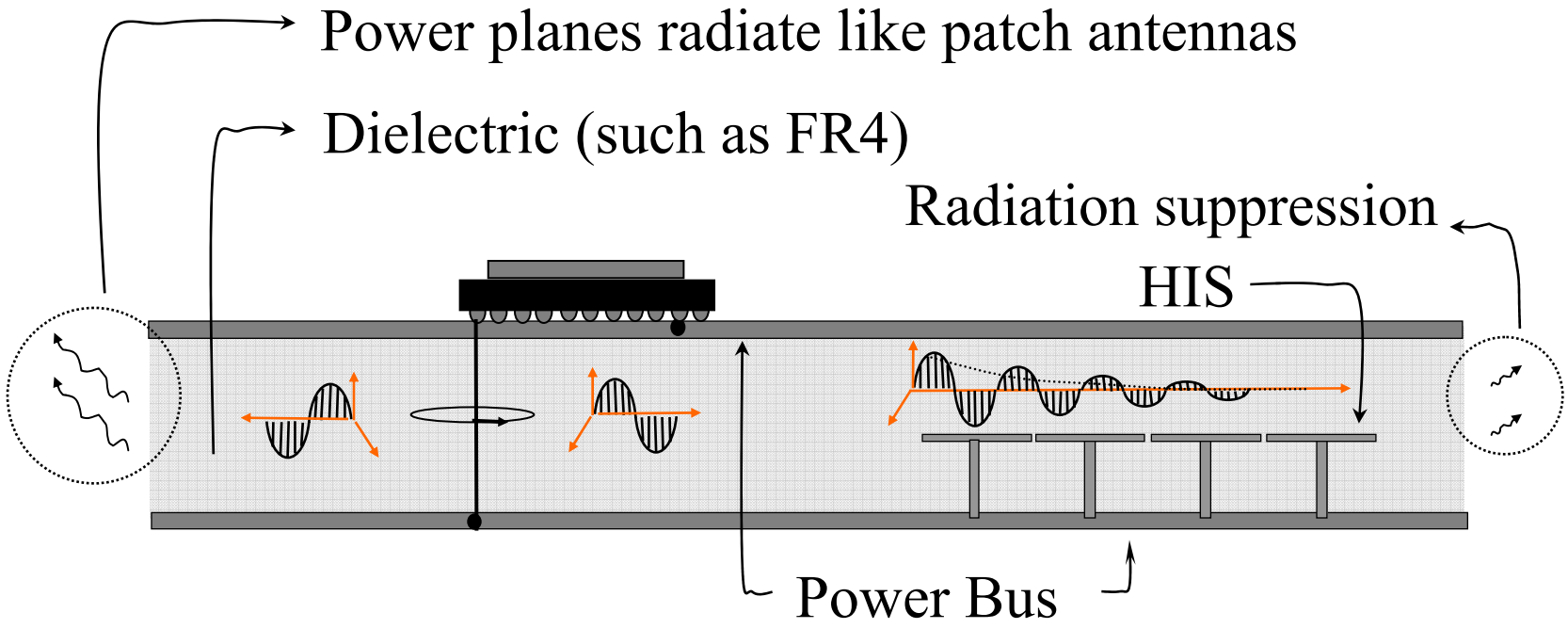



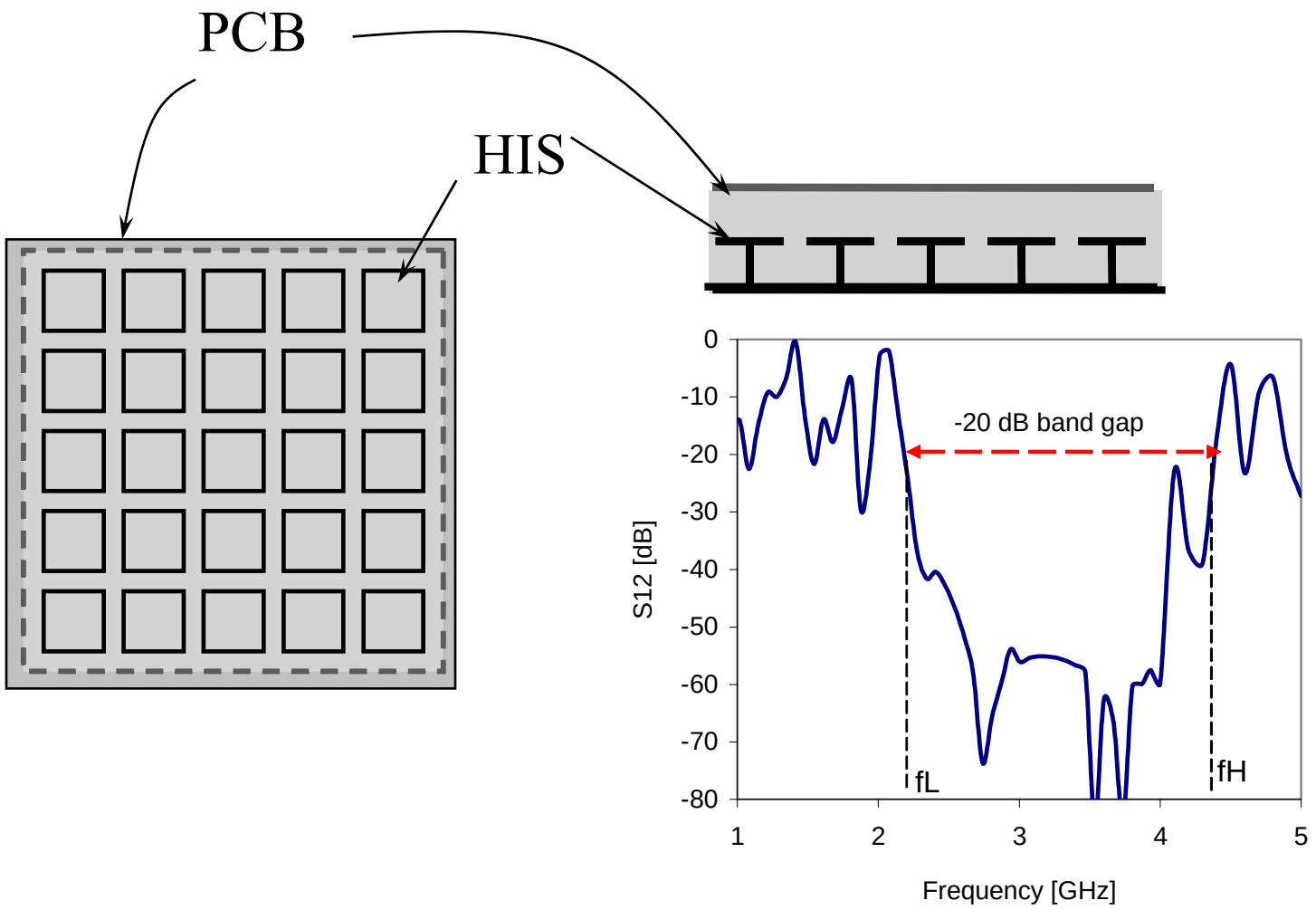

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

# Suppression Mechanism



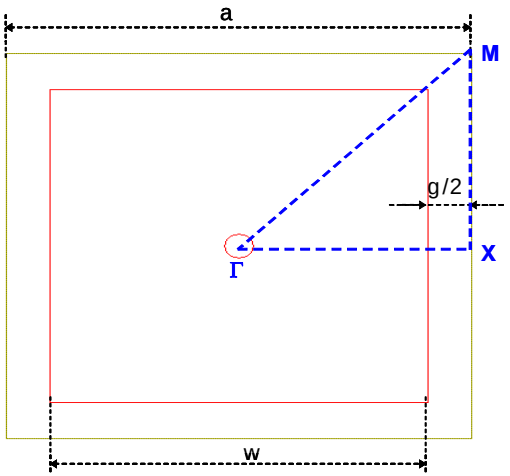

• Both propagation and emission from the board are suppressed with the employment of EEBG/EHIS structures.

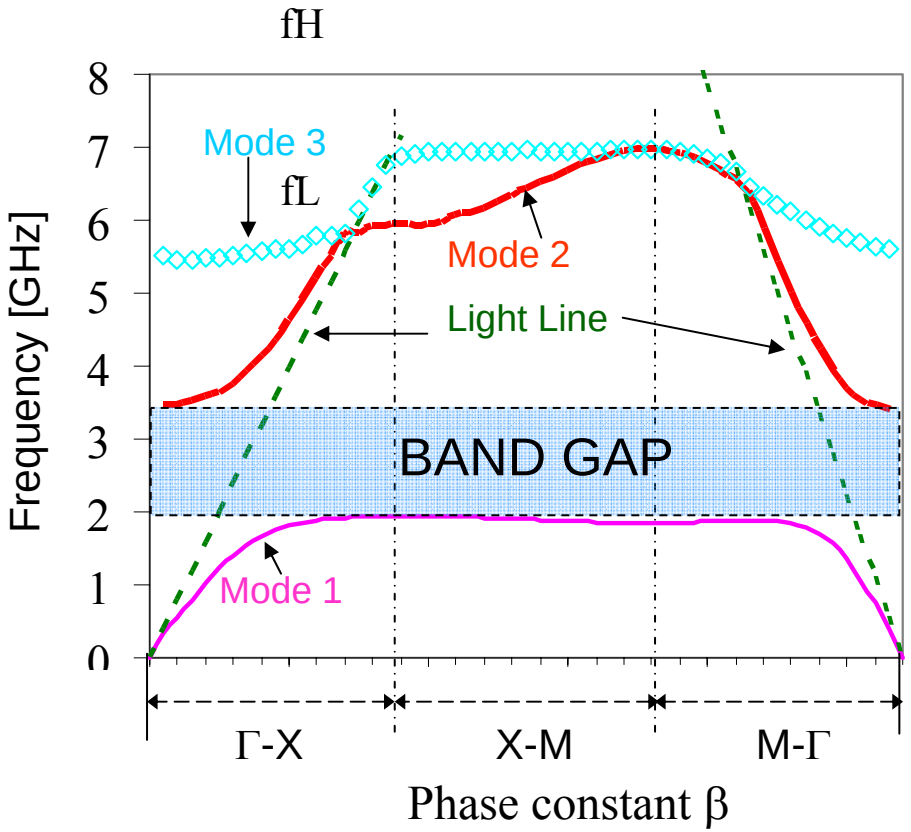
# Power Plane with Embedded HIS



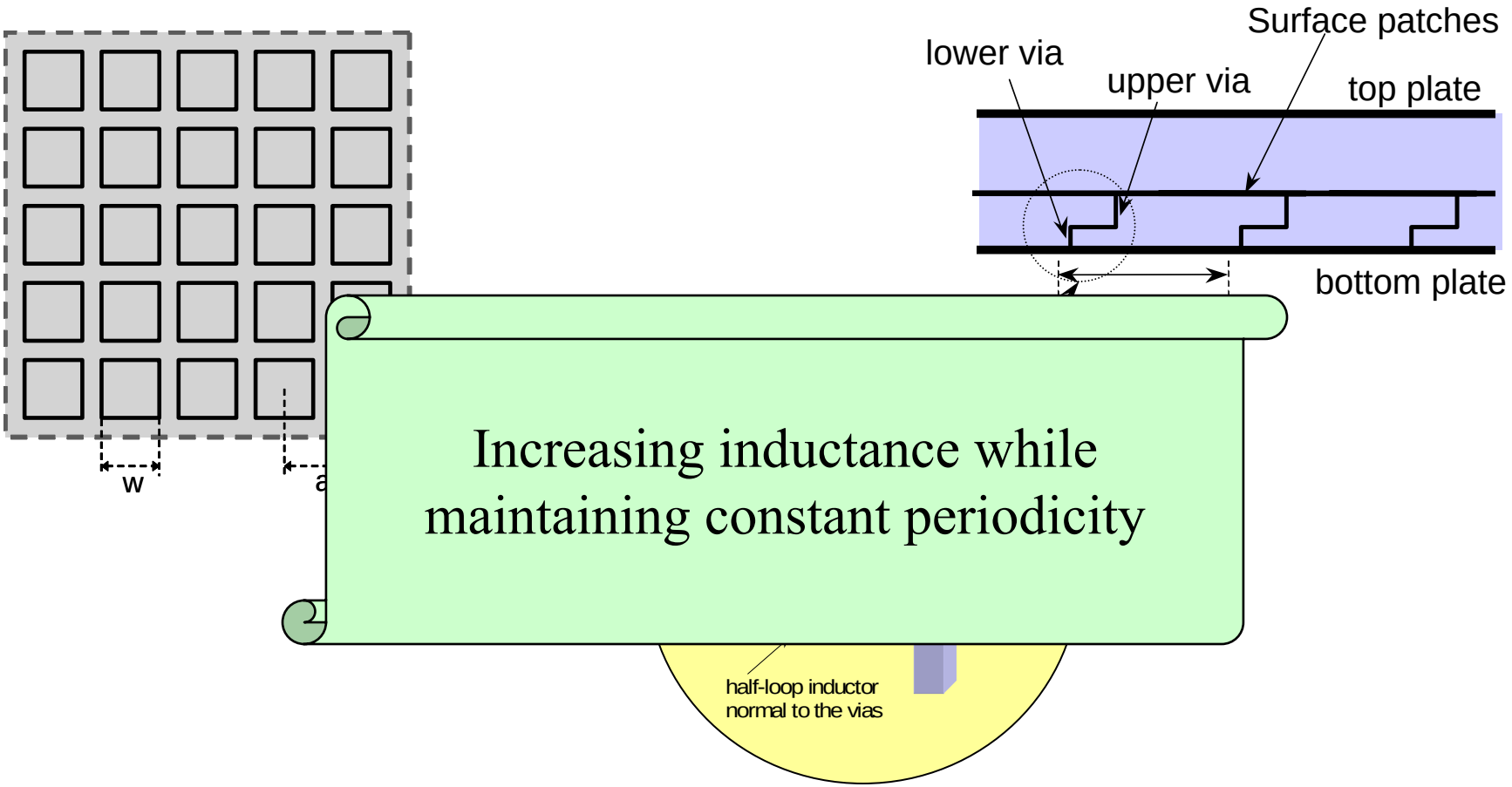
# Stop Band Prediction

Analysis of a unit cell provides eigenmode solutions for Maxwell's equations



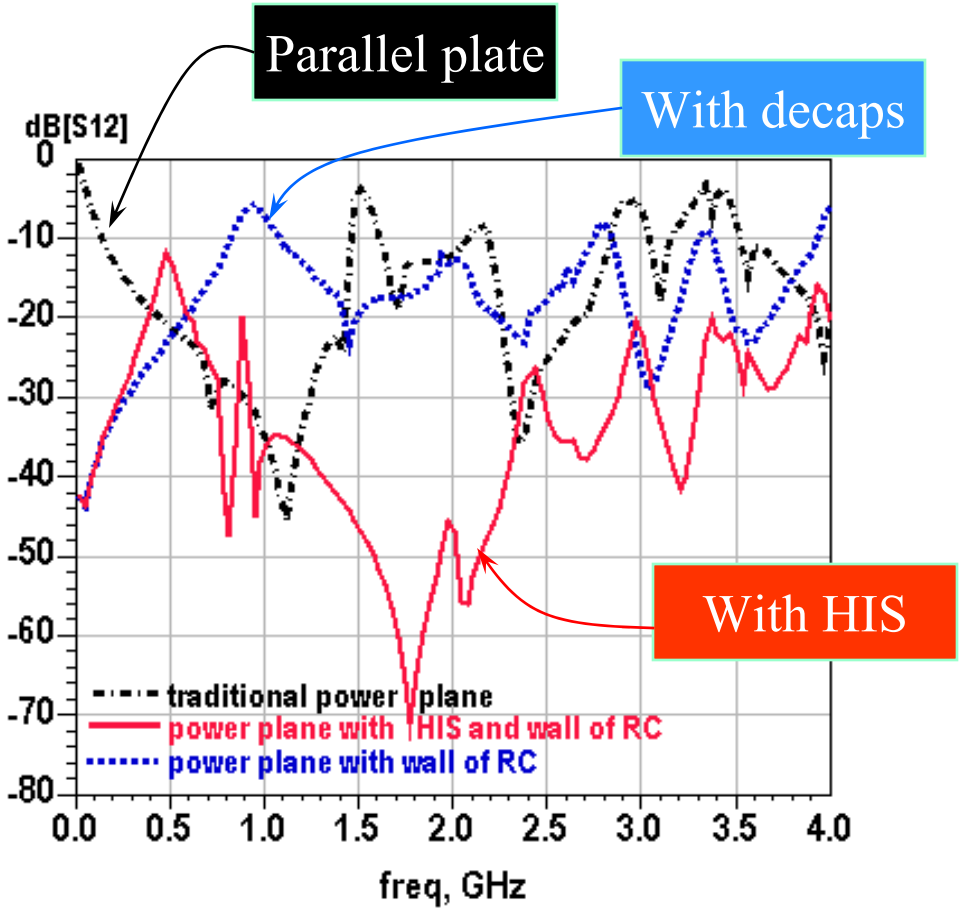



# Widening the Gap: Concept: Vertical Integration

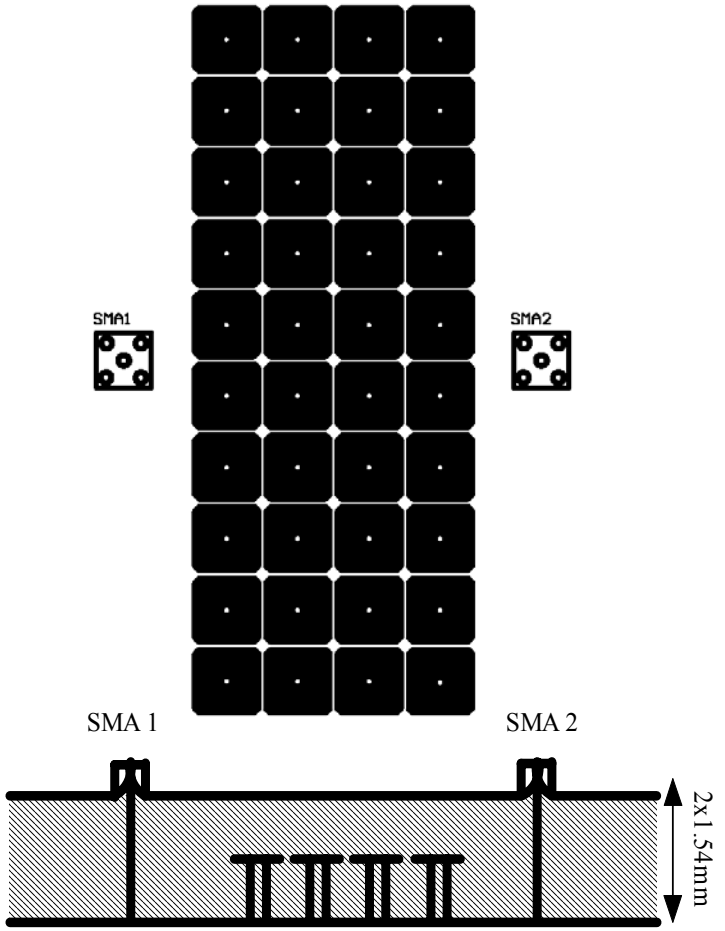


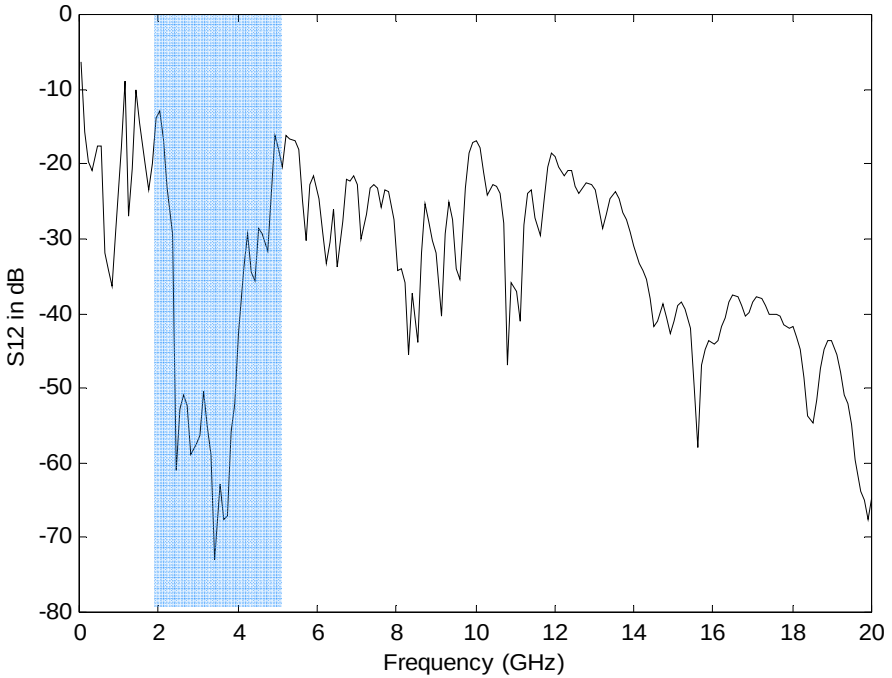
# EBG Inductance-Enhanced Power Planes

Achieved a 3.2 GHz –20 dB bandwidth!



# Experimental Validation

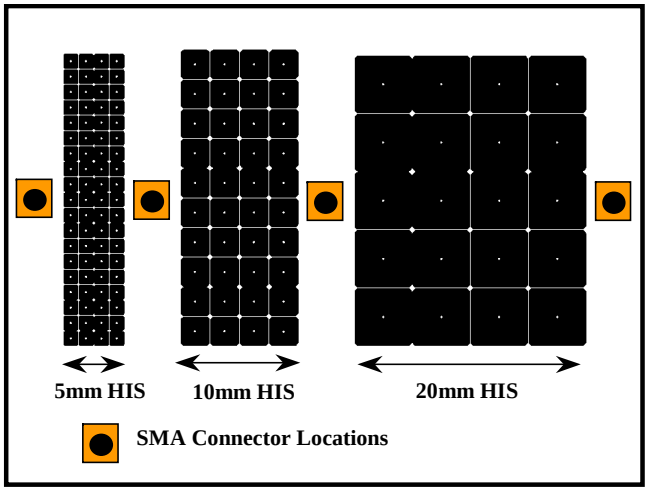


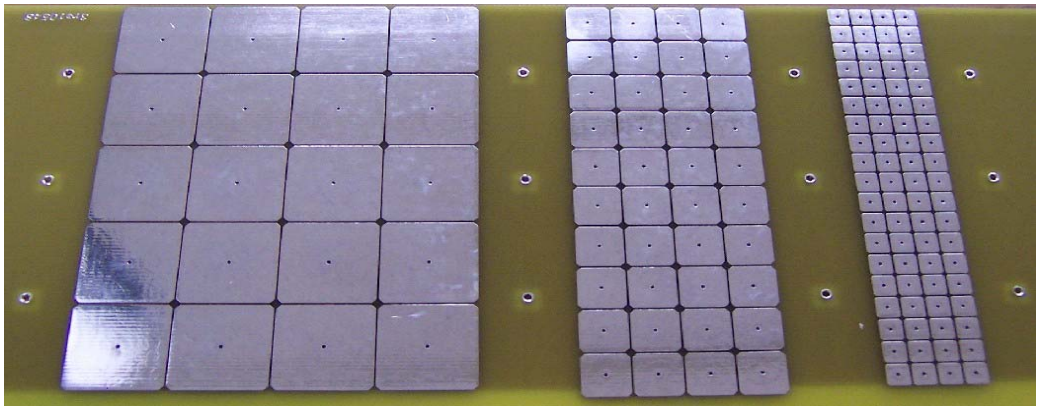




HIS:
period a = 10mm and gap g = 0.4 mm

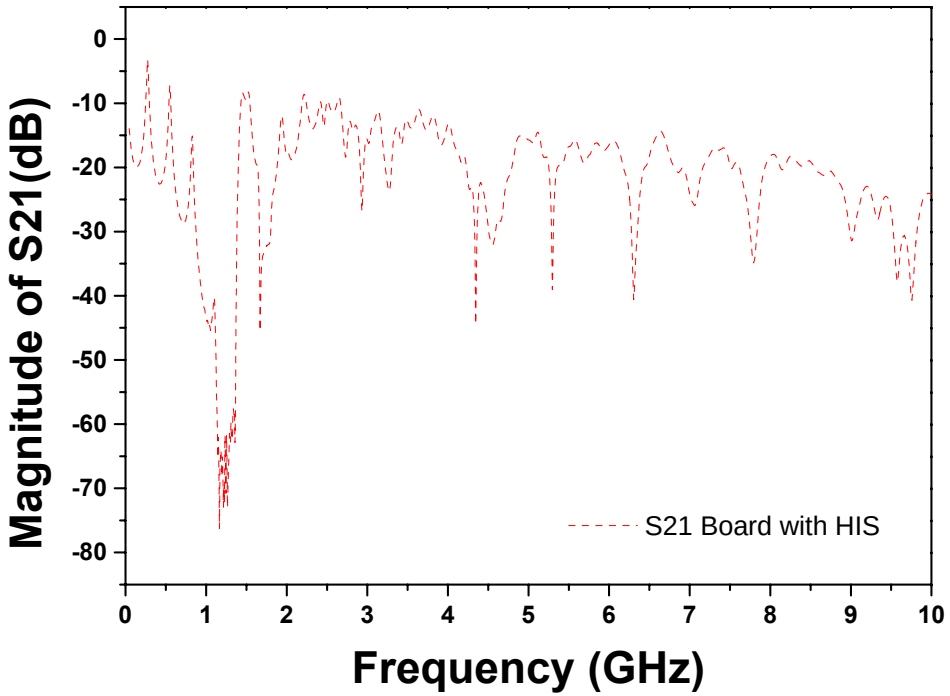
# Widening the Gap
# Concept: Cascading

*Concept: cascaded filter design*

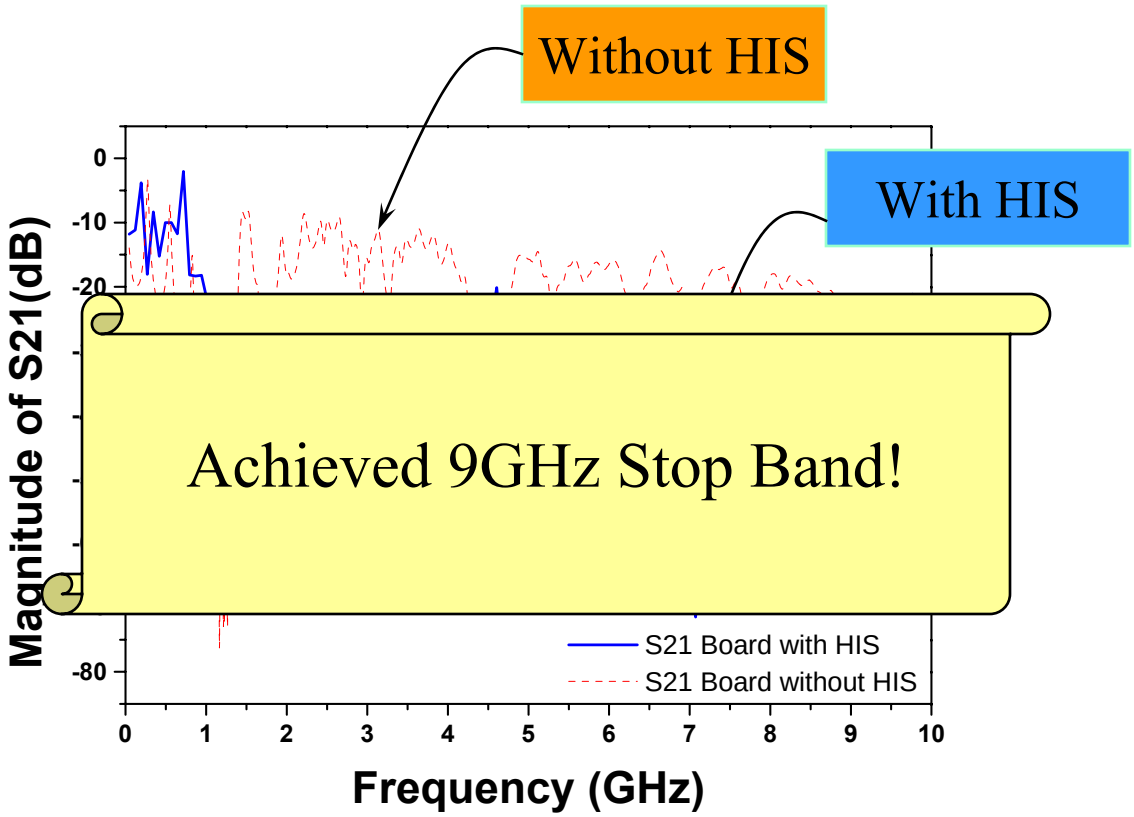


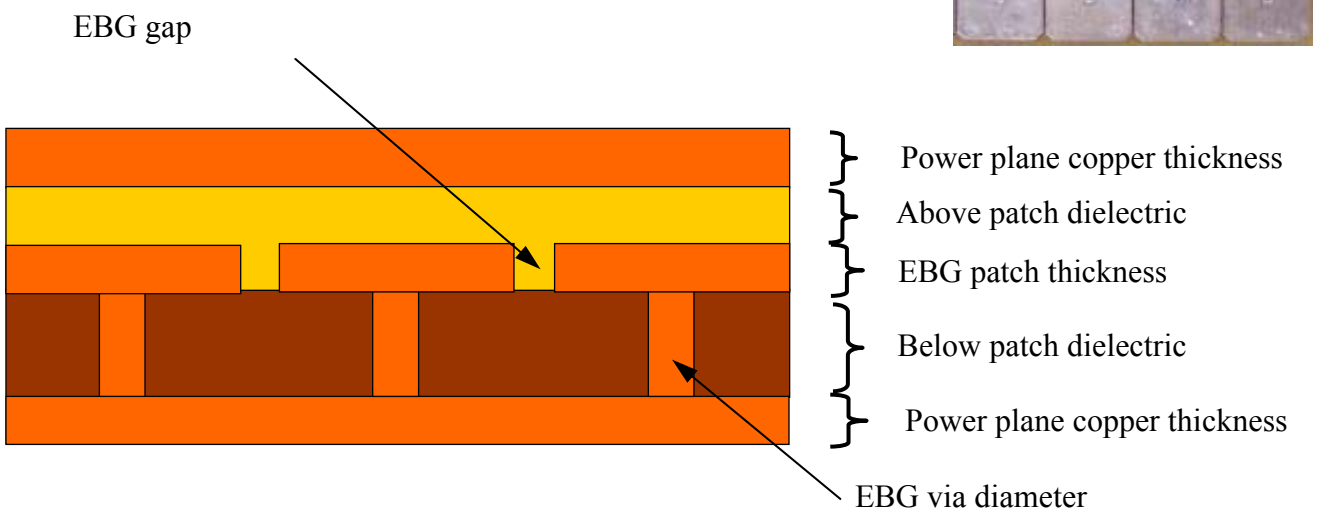
# Experimental Validation



# Experimental Validation

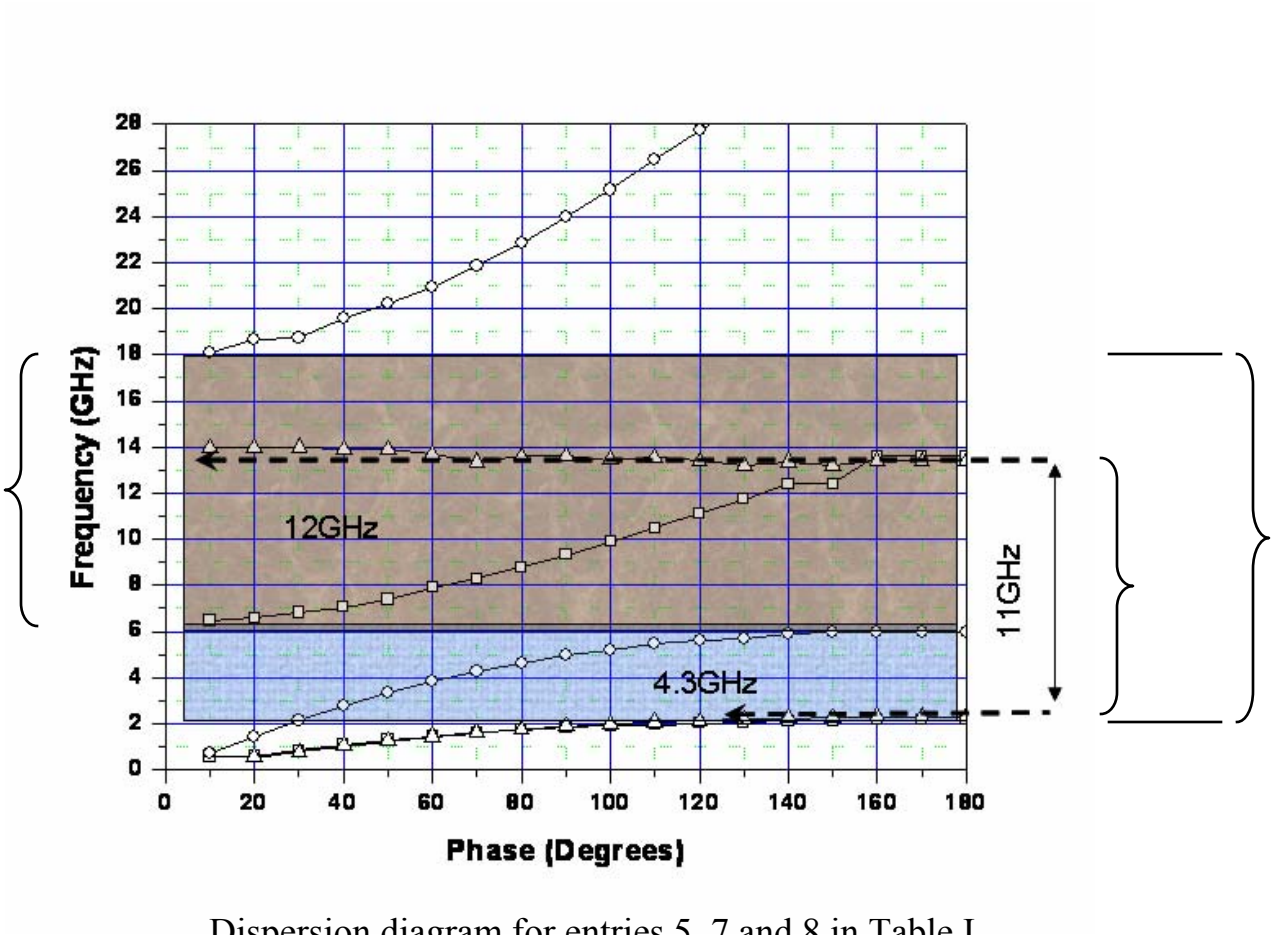


# Widening the Gap
# Concept: High Permittivity Material




(a)

# Numerical Validation




Dispersion diagram for entries 5, 7 and 8 in Table I.
Entry 5 can achieve and ultra-wide band gap (11 GHz) using high-dielectric material.
Cascading entries 7 and 8 can also achieve a wide-band region (16 GHz) but at a far lower cost.

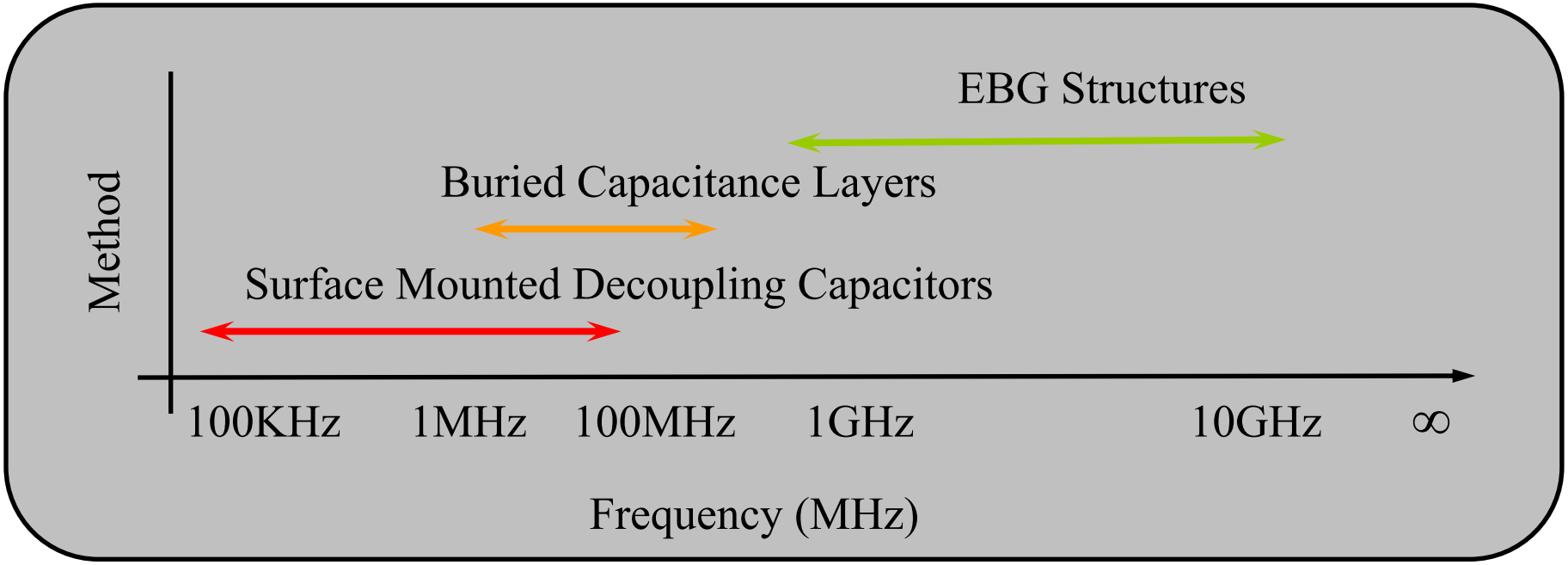
# Numerical Validation

| Entry Number | Patch size (mm) | Above patch $\varepsilon_r$ | Below patch $\varepsilon_r$ | Above patch th. (um) | Below patch th. (um) | Patch th. (um) | Gap size (um) | Via diameter (um) | $f_l$ | $f_h$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 10x10 | 4.1 | 4.1 | 1540 | 1540 | 0 | 400 | 800 | 2.13 | 4.03 |
| 2 | 10x10 | 8.2 | 4.1 | 1540 | 1540 | 0 | 400 | 800 | 1.6 | 3.71 |
| 3 | 10x10 | 12.3 | 4.1 | 1540 | 1540 | 0 | 400 | 800 | 1.35 | 3.12 |
| 4 | 10x10 | 16.4 | 4.1 | 1540 | 1540 | 0 | 400 | 800 | 1.22 | 2.87 |
| **5** | **2x2** | **30** | **4.1** | **16** | **100** | **0** | **200** | **125** | **2.3** | **13.1** |
| 6 | 2x2 | 30 | 4.1 | 16 | 100 | 35 | 200 | 125 | 2.28 | 13.2 |
| **7** | **2x2** | **4.1** | **4.1** | **16** | **100** | **0** | **200** | **125** | **5.96** | **18.1** |
| **8** | **5x5** | **4.1** | **4.1** | **16** | **100** | **0** | **200** | **125** | **2.17** | **6.46** |
| 9 | 5x5 | 16.4 | 4.1 | 16 | 100 | 0 | 200 | 125 | 1.11 | 6.44 |

# Experimental Validation

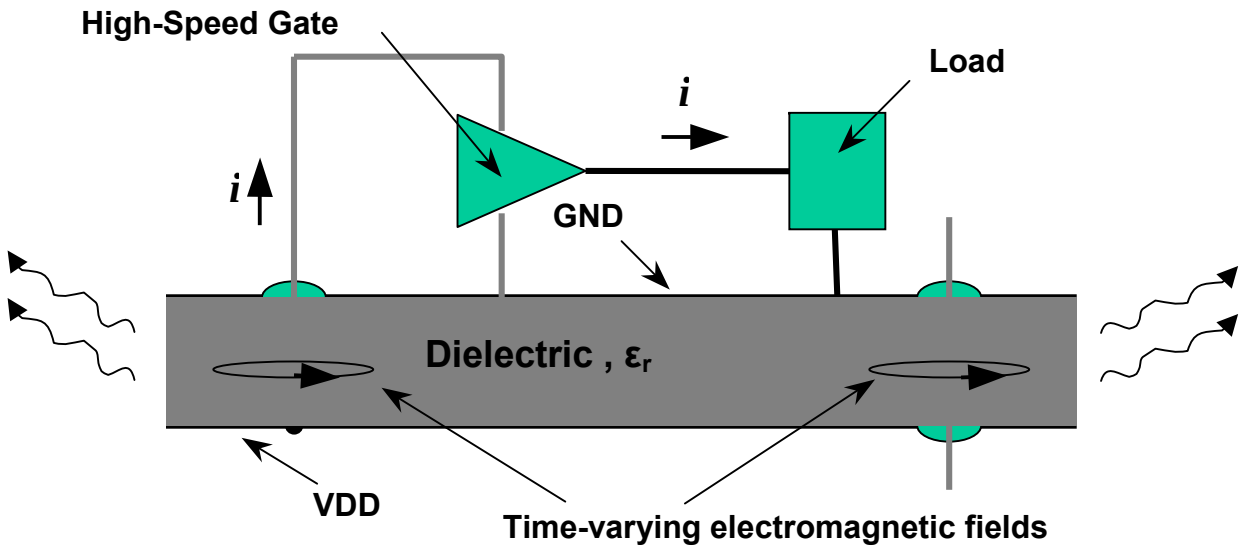
$$$

# Achievements



# Part II:
# EMI Reduction from PCBs (Interference and Immunity)

# External Radiation from PCBs

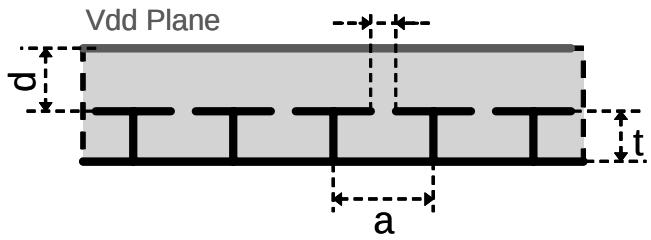


# EMI Reduction through EBGs

*Concept:*

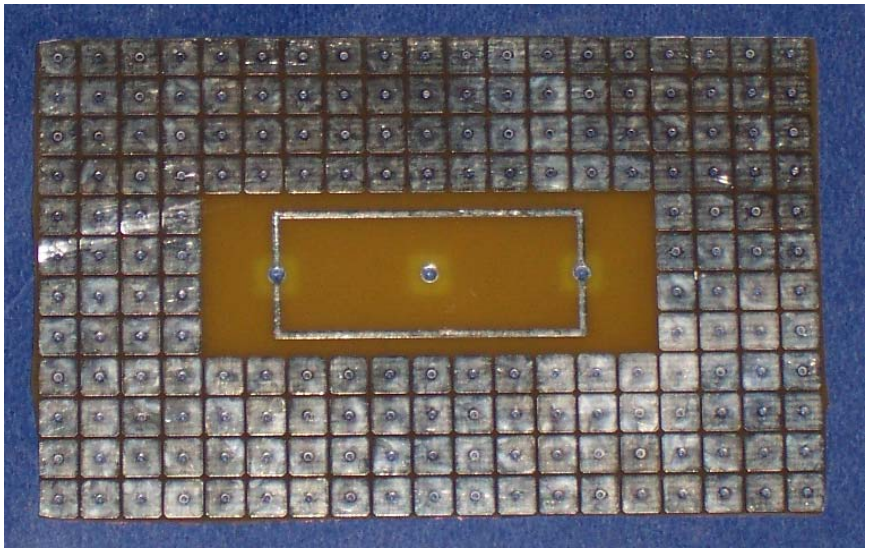
*Same as switching noise mitigation…*

*If waves don't travel within the PCB, they will not radiate!*

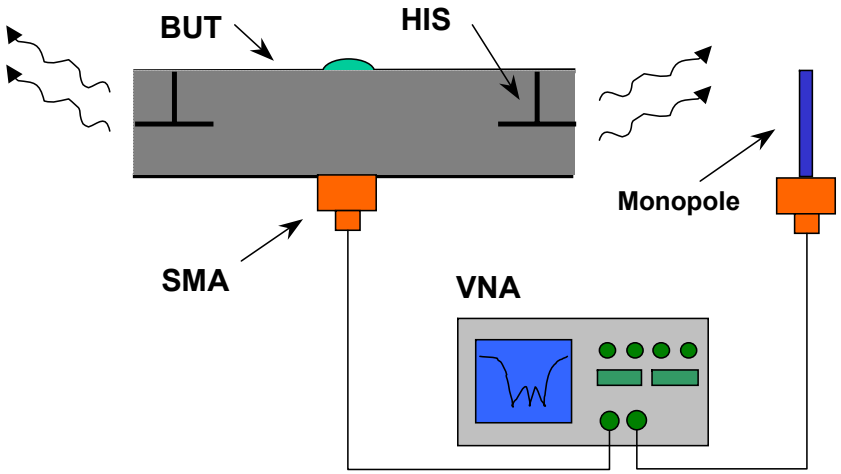


# EMI Measurement Setup

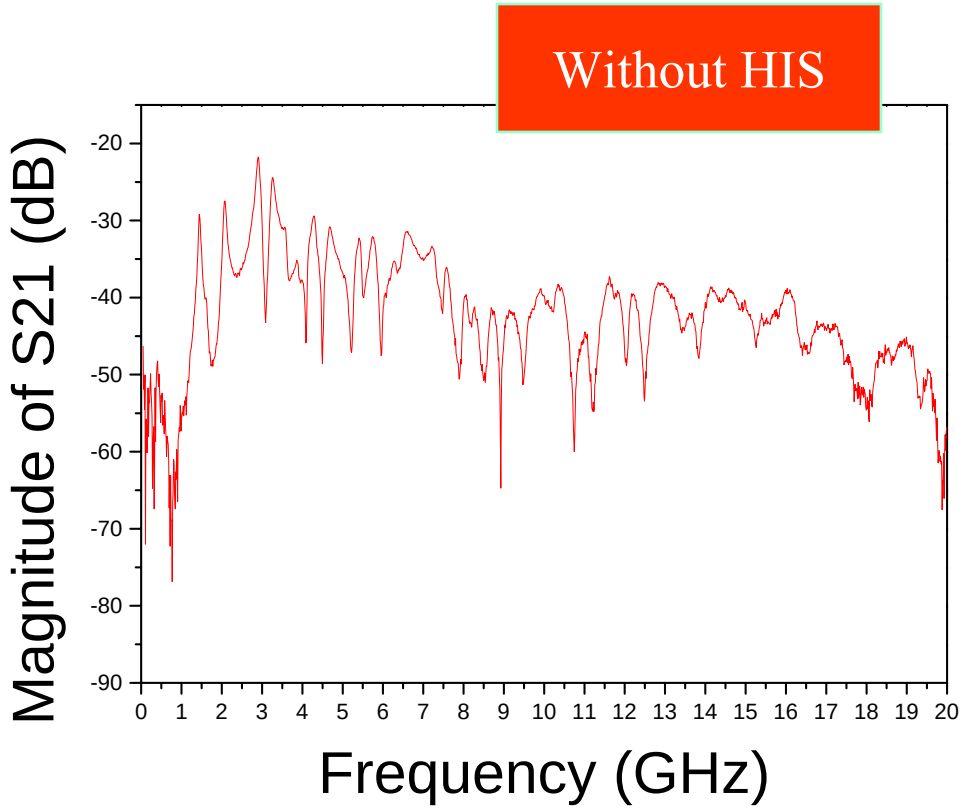
5mm x 5mm patches



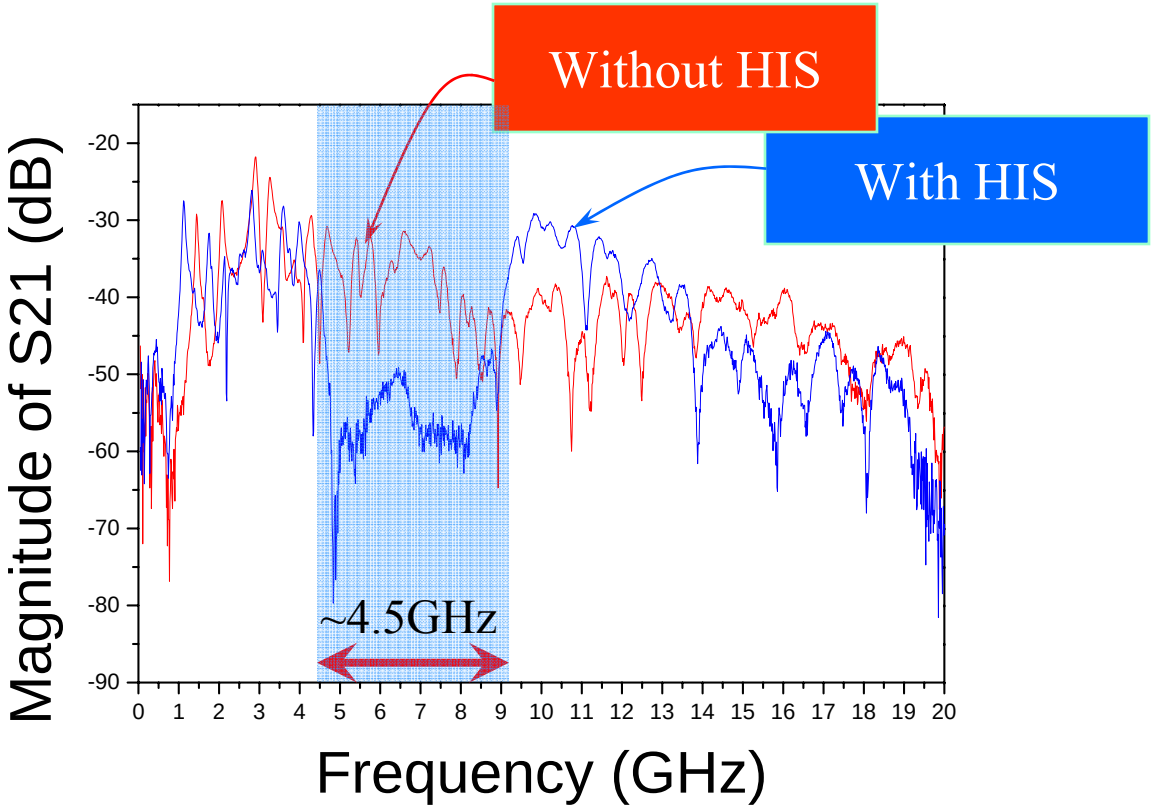
10cm x 6.5cm board



# Effect of HIS on EMI

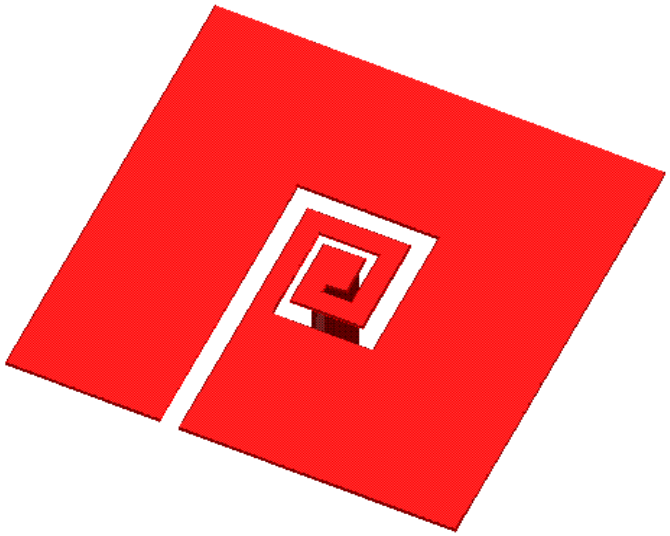


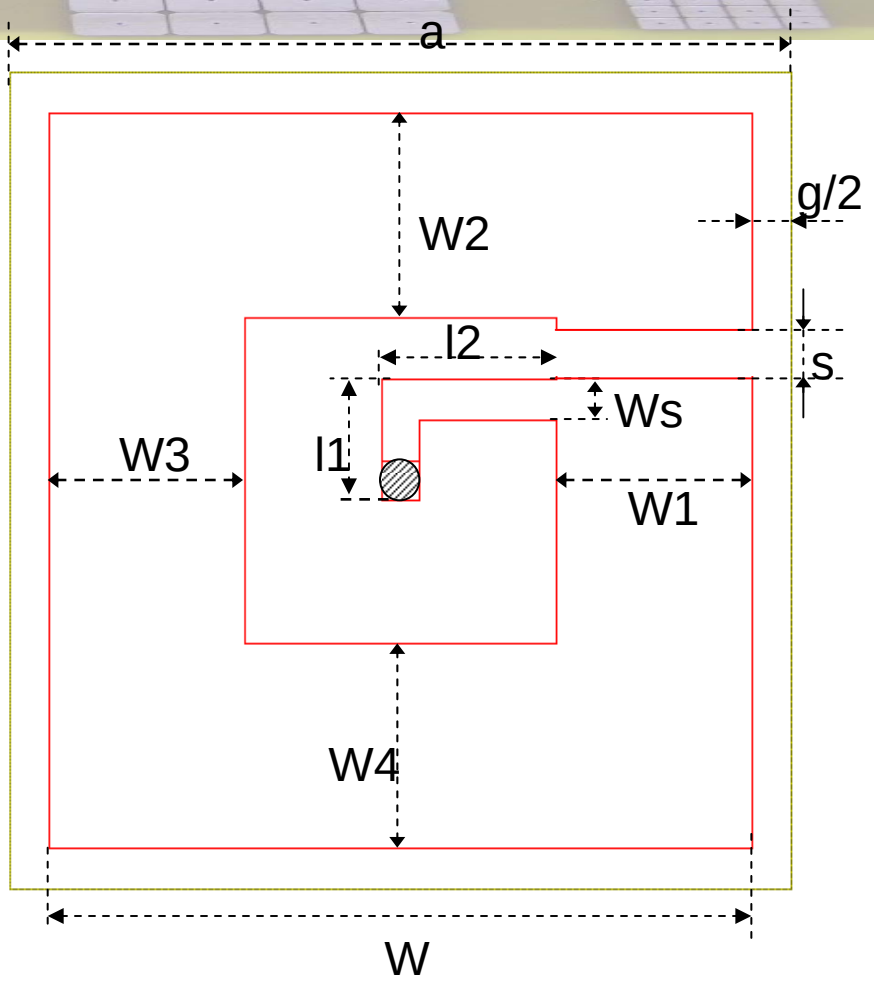
# Effect of HIS on EMI



# Part III:
# **Multiband** EBG Design

# Novel single-layer inductance-enhanced EBG

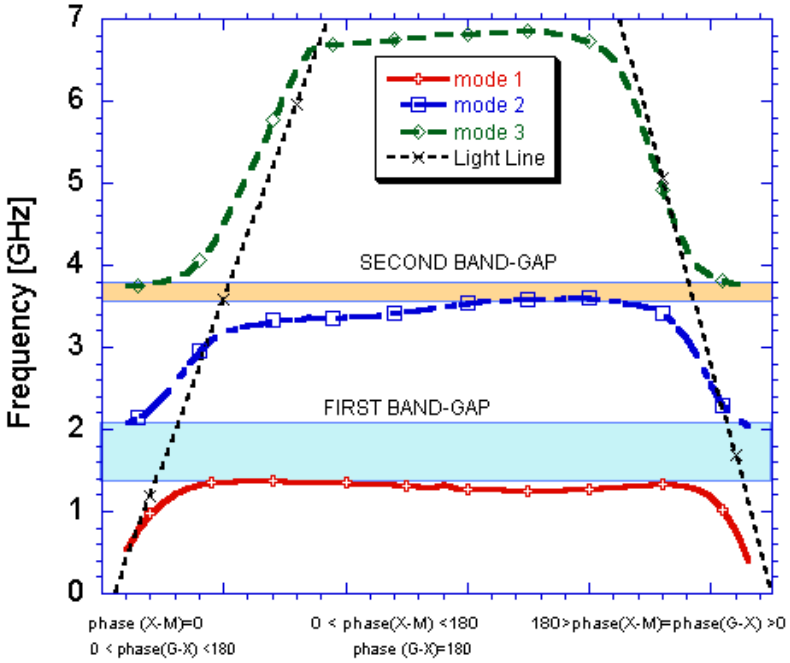




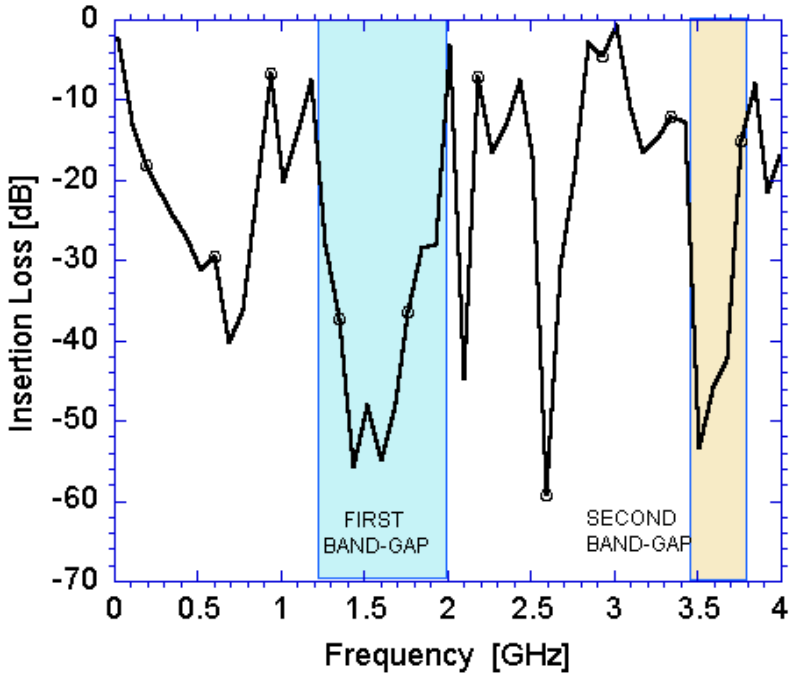

- Variable line width inductor used to replace patch of standard HIS
- Inductance of spiral adds in series to that of via
- High fringing capacitance through fat outer lines
- Additional design variables: number of turns, starting inner diameter, trace width

implementation for a period of 10 mm

# Electrical performance of novel EBG in parallel-plate environment




Dispersion diagram



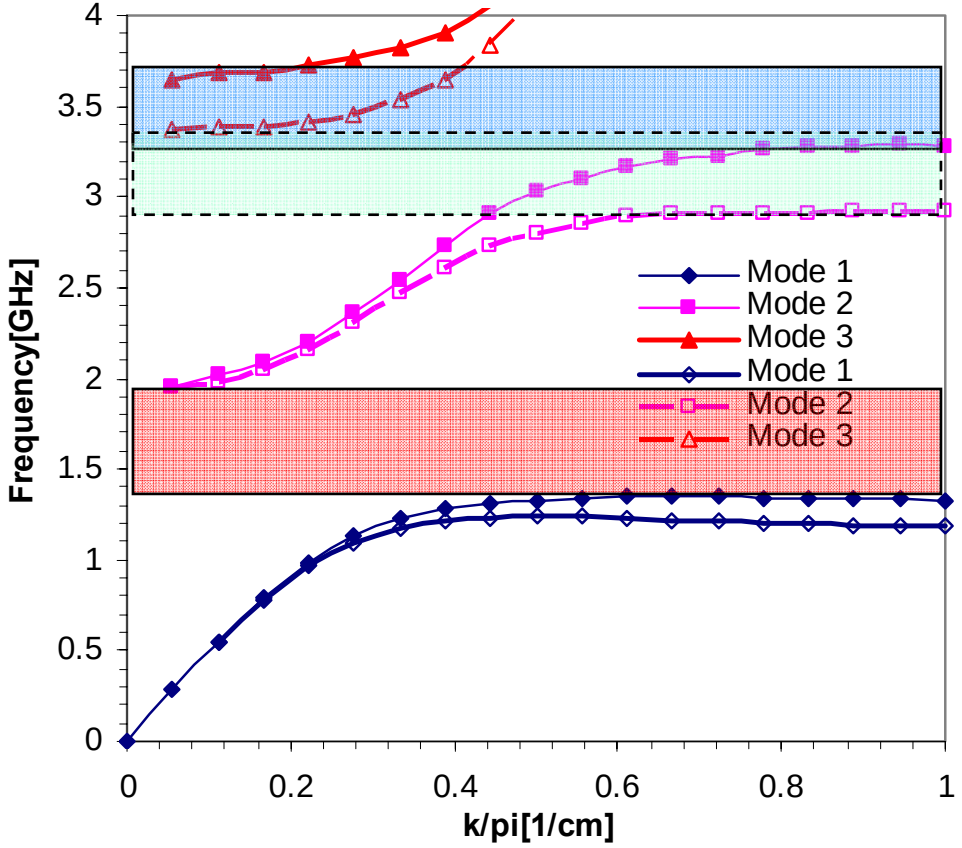

S-parameters

***s=0.4 mm, W=9 mm, g=1 mm, a=10 mm, W1=3.5, W2=W3=W4=2.5 mm, l1=1.5 mm, l2= 2 mm, Ws = 0.5 mm***

- Existence of two band-gaps
- Multiband noise mitigation possible

- Type of modes also analyzed by looking at field plots at different phase constant

# Upper bandgap tuning using spacing




Spacing (gap) is reduced from 1mm (filled symbols) to 0.4 mm (empty symbols)

**Upper band:**

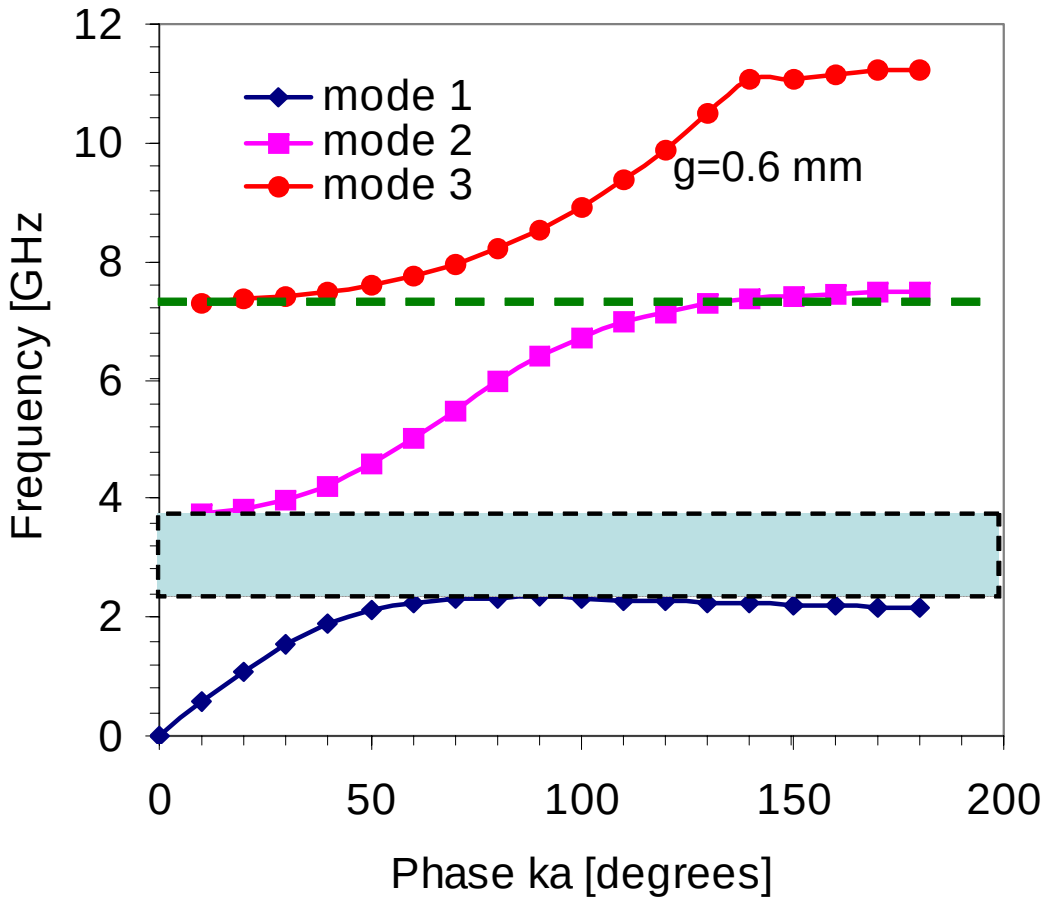
Moves towards lower frequencies with slight variation in the bandwidth

**Lower band:**

- Lower edge slightly affected
- Change can be compensated through variation in the spiral inductor geometry or period

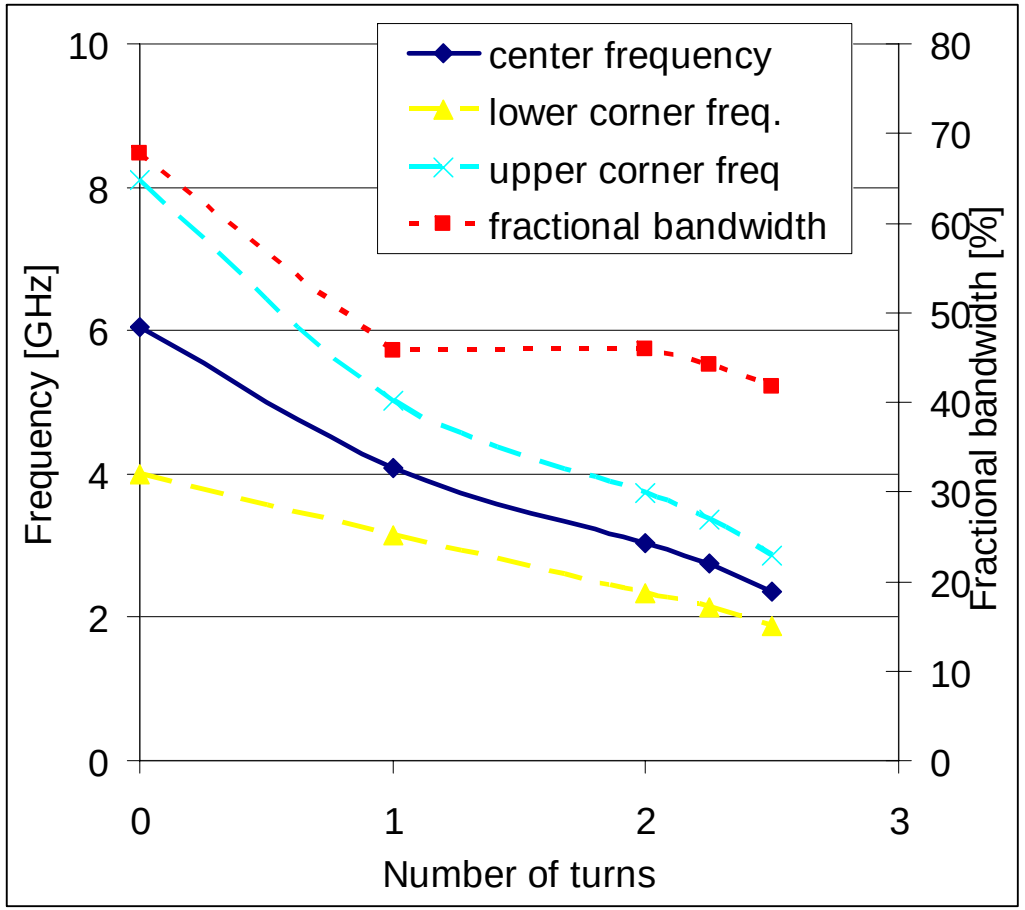
This indicates that the two bands can be tuned independently

# Second band-gap disappearance in a structure with smaller periods



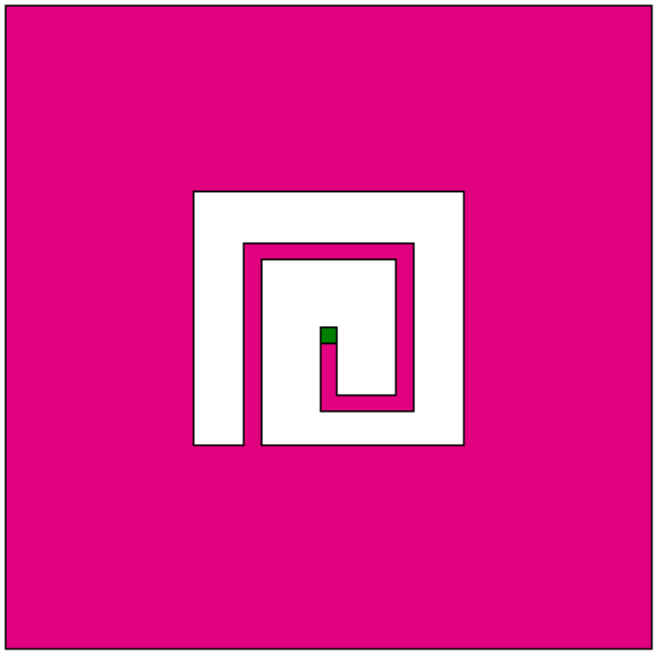
# Effect of number of turns on first band-gap

- Physical dimensions: a=5mm, g=0.6mm, t=d=1.54mm
- Band-gap shift to lower frequency, when traditional HIS replaced with novel EBG
- Band-gap lowering with increase in number of turns
- Fractional bandwidth > 40% at 2GHz

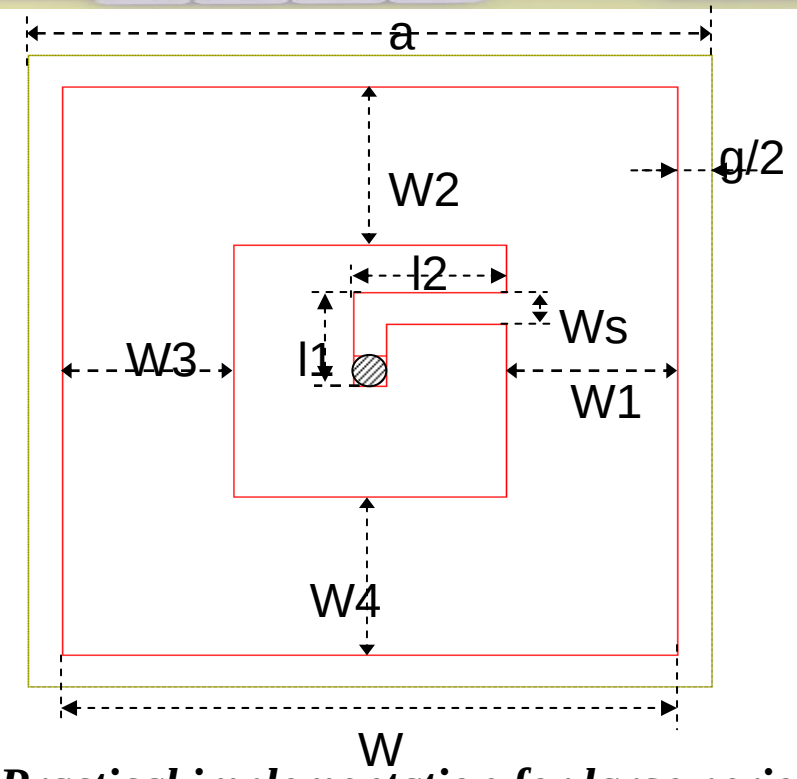



Note: N=0 corresponds to standard HIS

# “Complementary” Structure

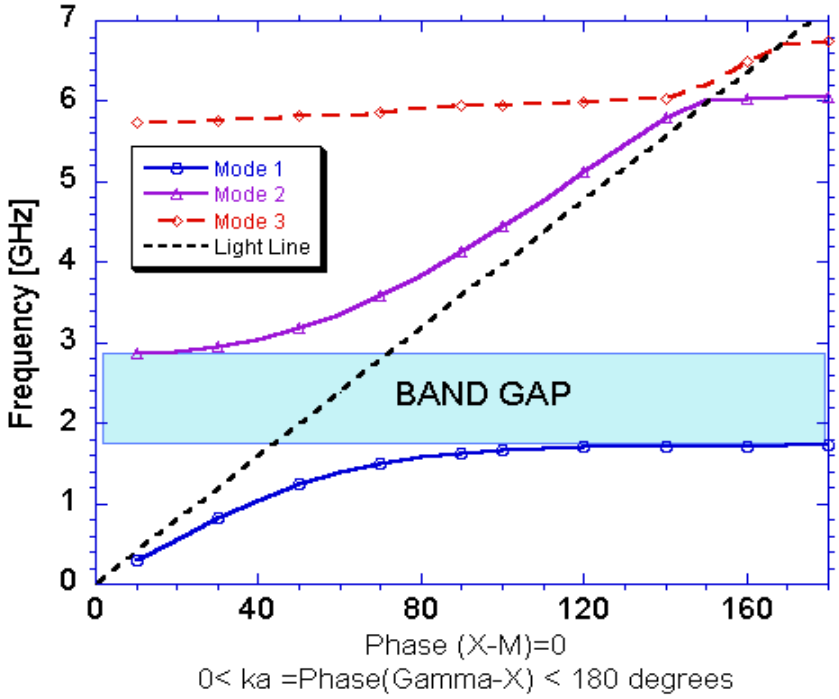


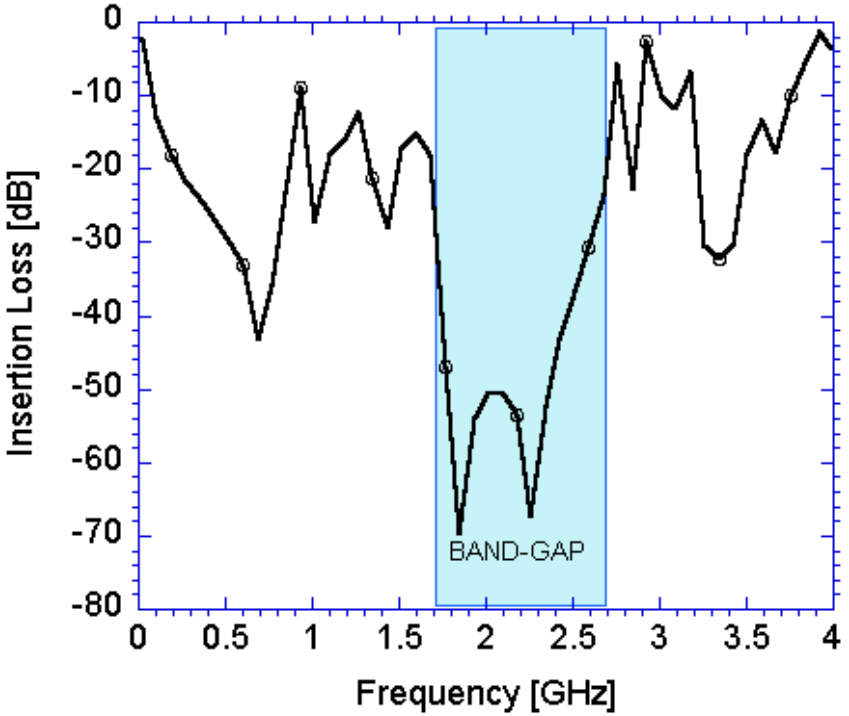
*concept*




***Practical implementation for large period (a=10mm)***

# EBG using spiral with outer loop closed as patch: simulation results




***W=9 mm, g=1 mm, a=10 mm, W1=3.5, W2=W3=W4=2.5 mm, l1=1.5 mm, l2= 2 mm, Ws = 0.5 mm.***

- Band-gap region at lower frequencies compared to power plane with standard HIS

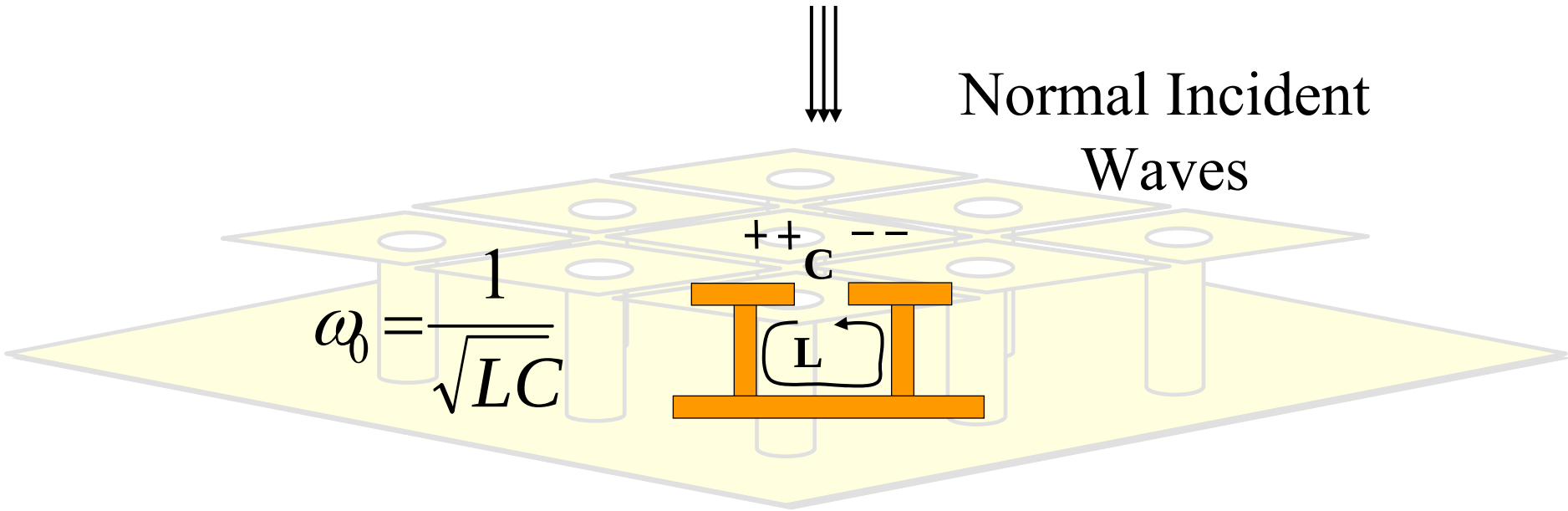
# EBG Structures embedded in PCB's

• The whole structure, acts as a band-stop filter by suppressing surface waves within a predictable range of frequencies. *It also suppresses waves supporting surface currents*

• This frequency range is a function of the geometrical features of the structure (such as periodicity, patch size, gap size, via diameter, via length and also board thickness) as well as the dielectric material used in the printed circuit board as substrate.

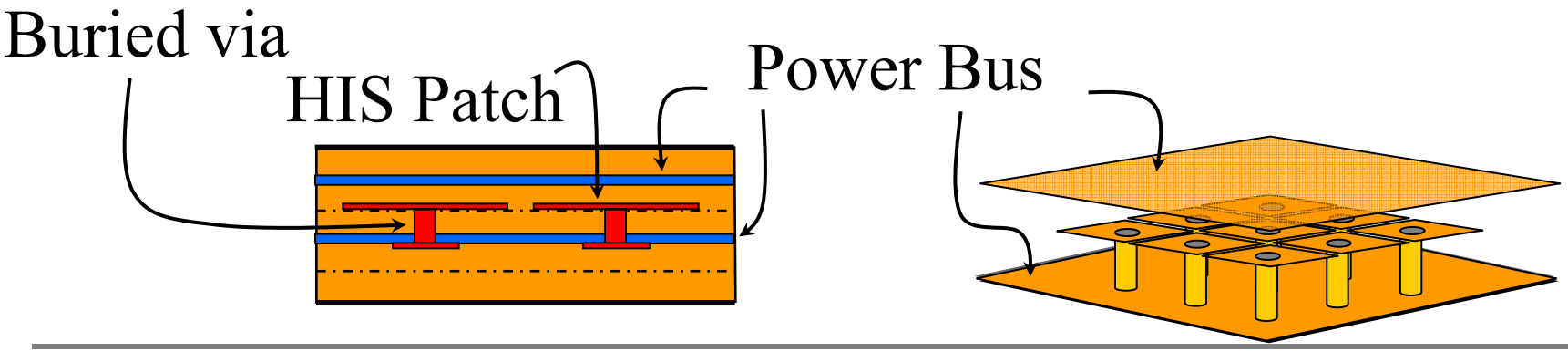
# Part III:
# Accurate Band Gap Prediction

# Electromagnetic Bandgap Structures: Lumped Element Perspective



# Design and Fabrication

• Design and simulation of EEBG structures is followed by fabrication using a commercial PCB process with FR-4 as dielectric.



# Need for Simple and Accurate Models

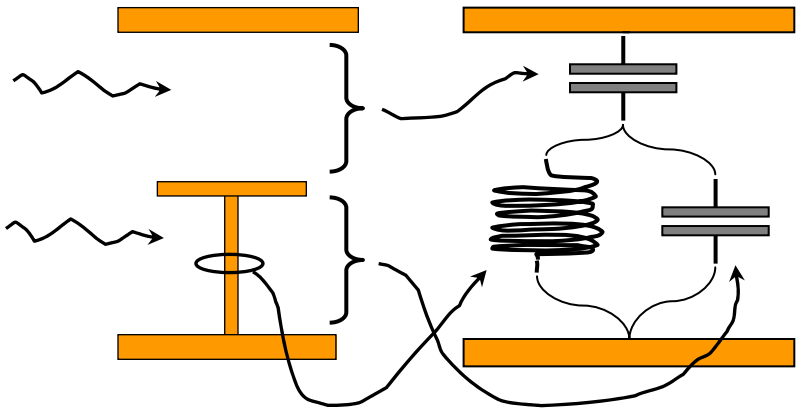
- Full wave simulations are slow and costly

- It is costly and not feasible to do trial and error experiments

- Engineers like to have initial but accurate estimations of the resulting bandgap by doing a couple of calculations

# Fast and Simple Design Technique

## Lateral view of a single cell



- Physics-based circuit modeling

$$f_{res} = \frac{1}{2\pi\sqrt{L\ (C_1 + C_2)}}$$

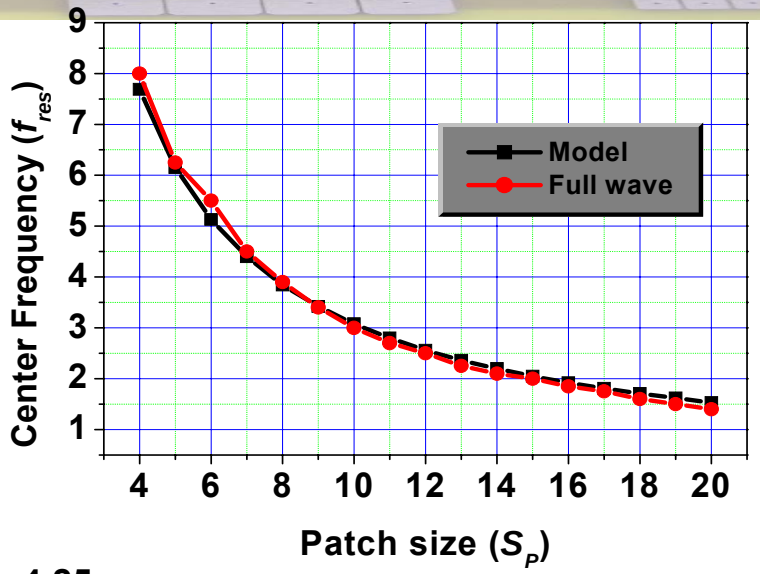
HIS via (L value: approximate methods)

Plate-to-Patch Capacitance ($C_1 = \varepsilon_r\varepsilon_0 \boldsymbol{S_p^2 / H_v}$)

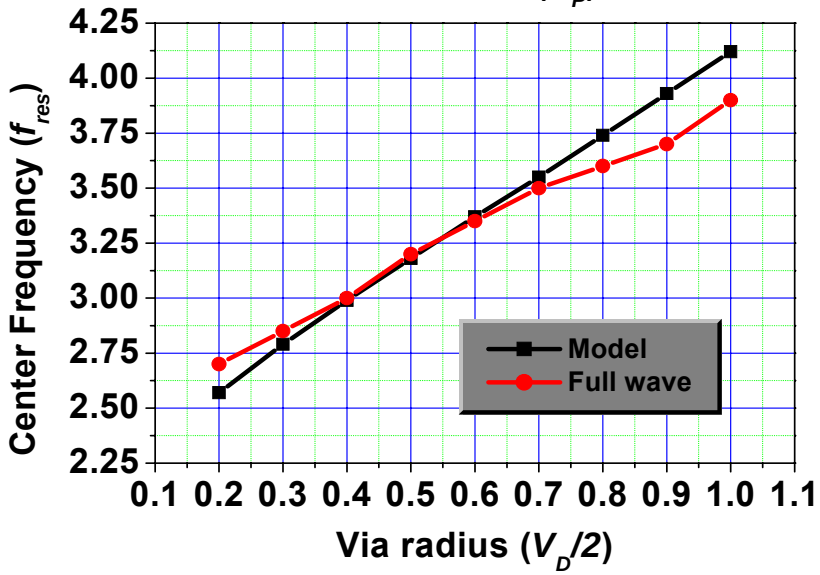
Patch-to-Plate Capacitance ($C_2 = \varepsilon_r\varepsilon_0 \boldsymbol{S_p^2 / H_v}$)

# Accuracy of the Model

- Accuracy of the model while the patch sizes changes ($C_1$ and $C_2$ change)

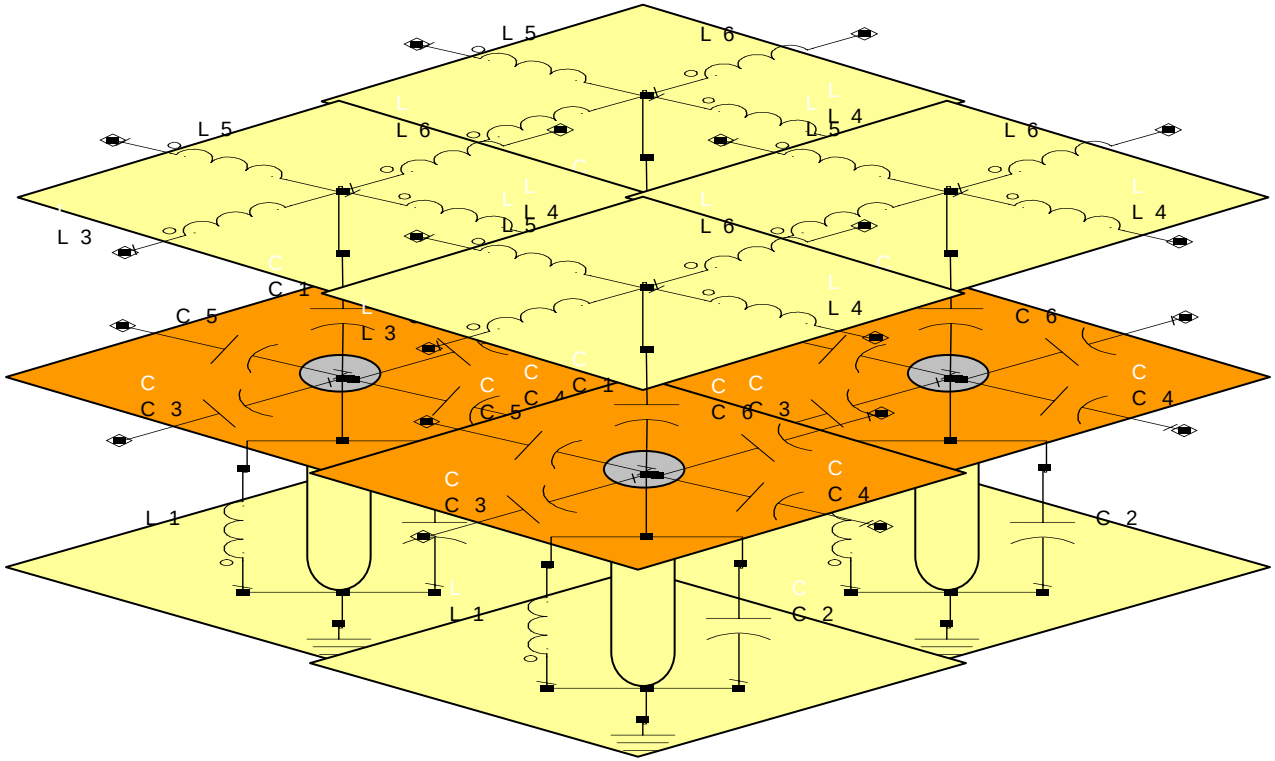



- Accuracy of the model while the via radius changes (L changes)



# 3D Model

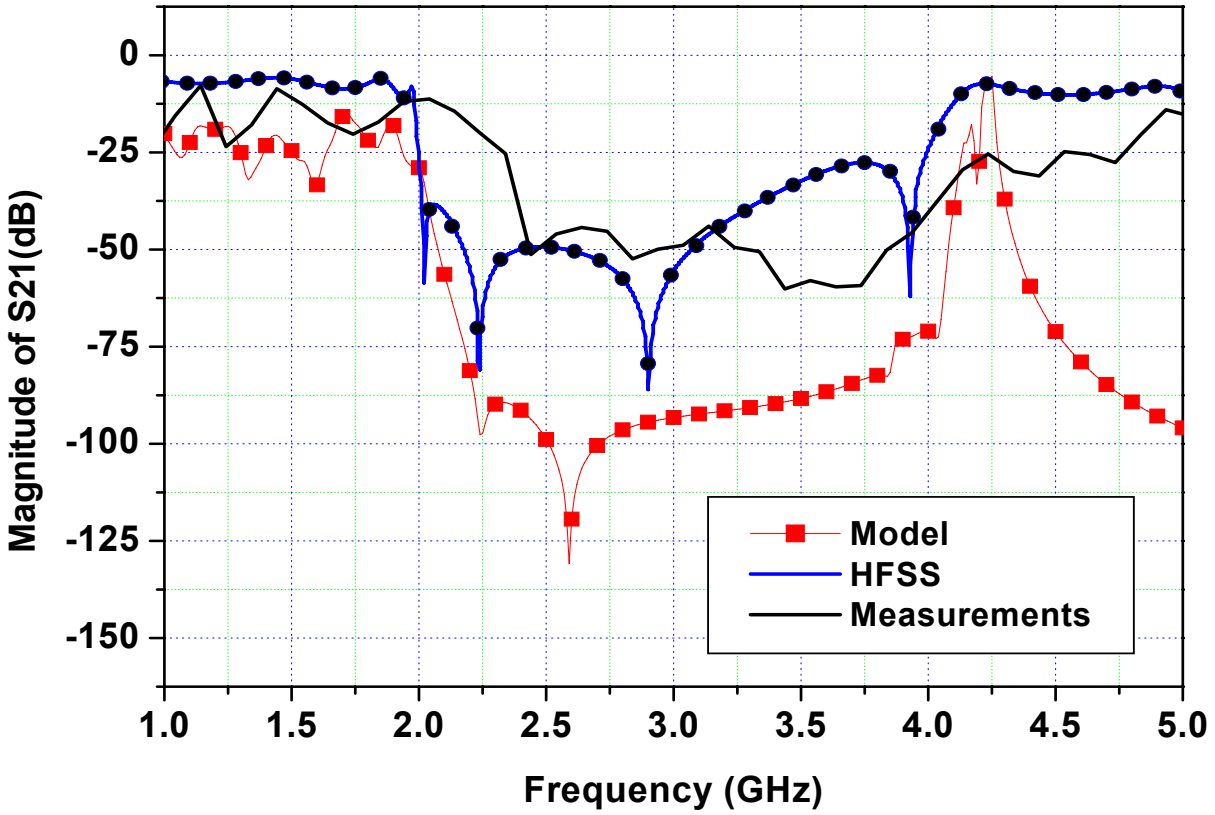
• EEBG cell model integrated in a macro-model of power/ground planes.



# Why the circuit model?

**Reduce printed circuit board simulation time from HOURS to seconds!**

# Numerical and Experimental Results



# Conclusions

- Provided accurate EBG-embedded PCB models
- Introduced multi-band EBG design concepts
- Introduced three different concepts for wideband applications

# Future Work

Miniaturization!