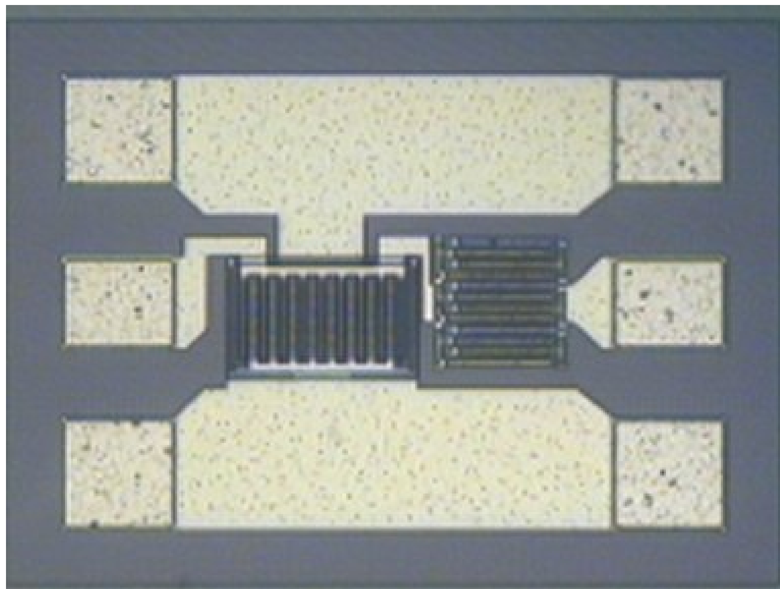
Gate Oxide Degradation

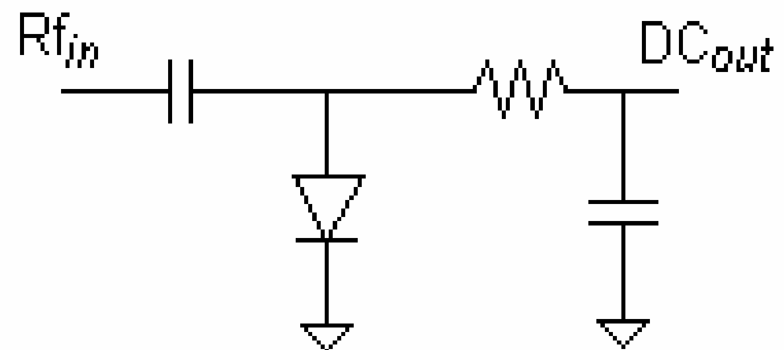
R. Jacob Baker and Bill Knowlton

- Microwave test structures
  - What's been done
  - What we're doing
- The weakest link (gate oxide stress)
  - Motivation
  - Why oxide is the weakest link
- Experimental results
  - Device stress
  - Circuit stress
- Summary and publications

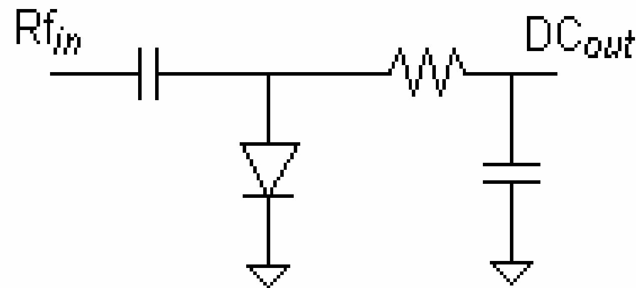
What has been done

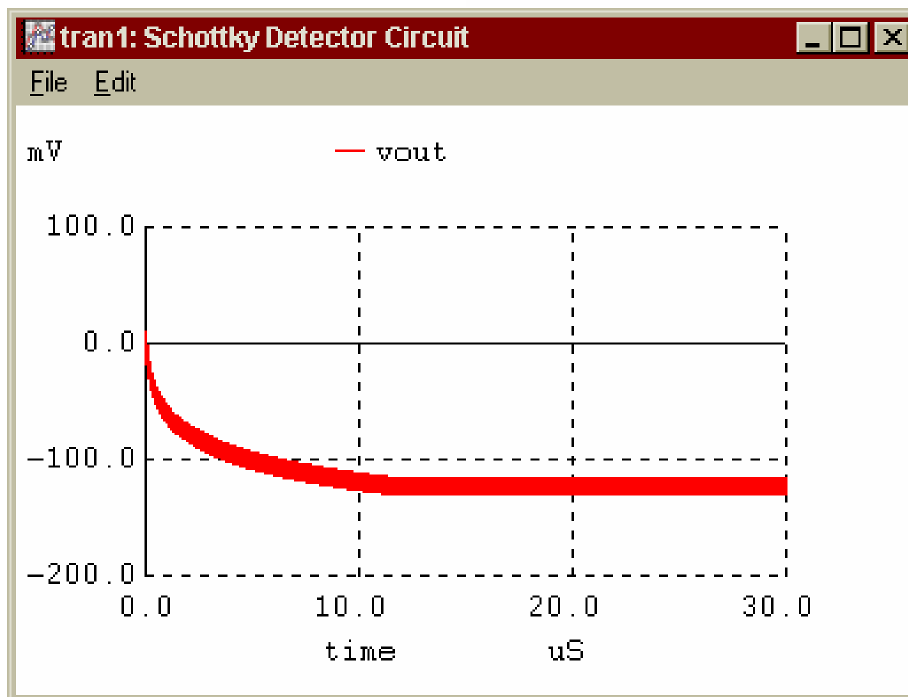
- Design of Schottky diodes, first-chip
- Re-design due to spacing problems
- Characterized Schottky detector circuit below





Circuit Characteristics



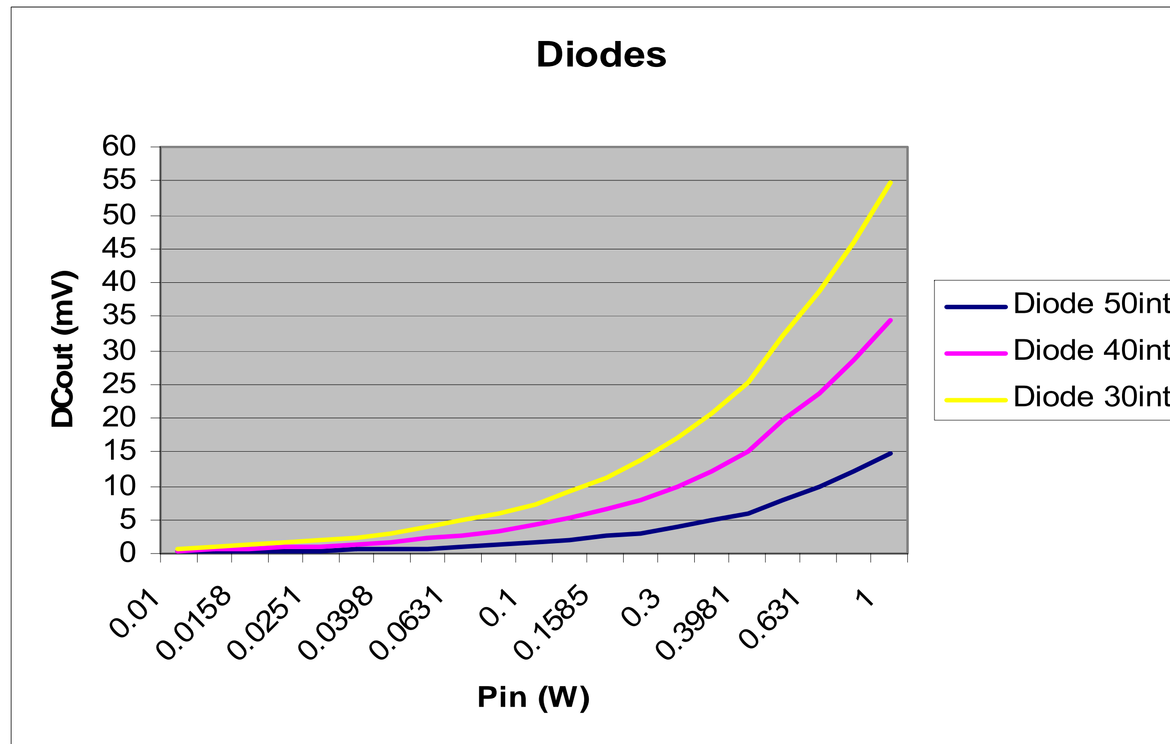


Schottky Detector Circuit

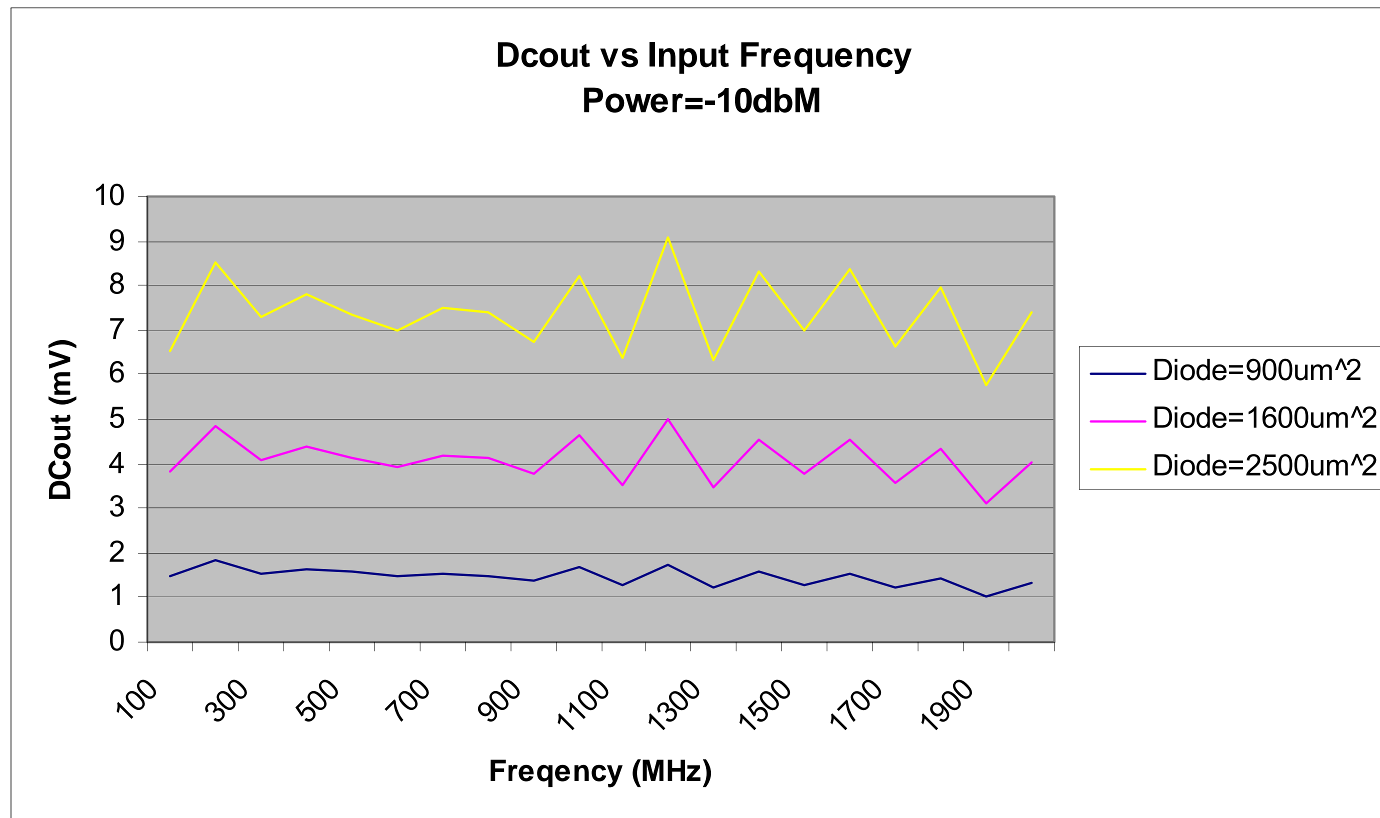
.control
destroy all
run
plot vin
plot vout
.endc
D1 VD 0 dmod 30
C1 Vin VD **.5p**
R1 VD Vout **1k**
C2 Vout 0 **10p** IC=0
Vin Vin 0 sin 0 **500m 1G**
.TRAN .1n 30u
.MODEL dmod D vj=0.3 cjo=0 tt=0
rs=10
.end

Measured Results

- Several different types of test structures
- Measured the DC voltage out as a function of microwave power applied to the test structure.



- We also looked at the frequency behavior of the circuit.



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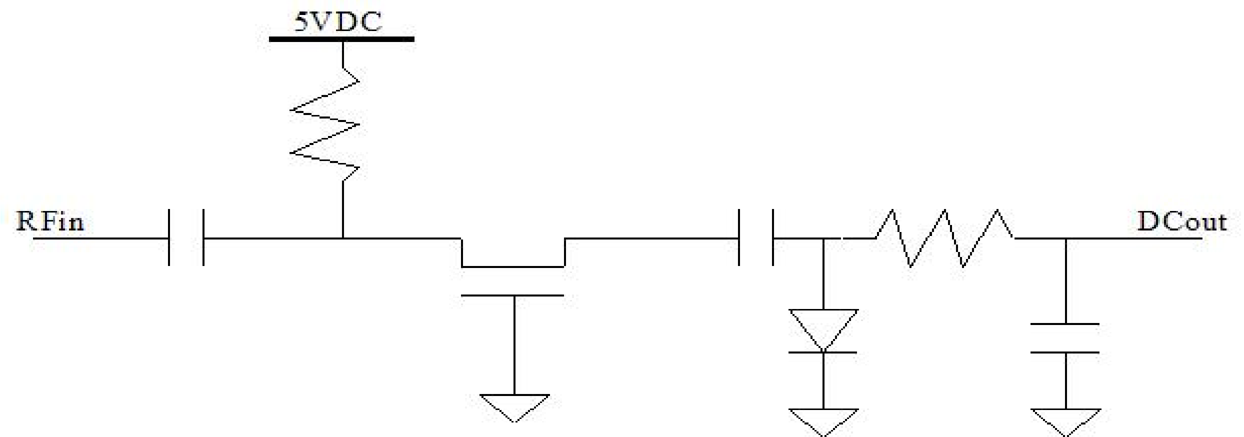
Current Activities

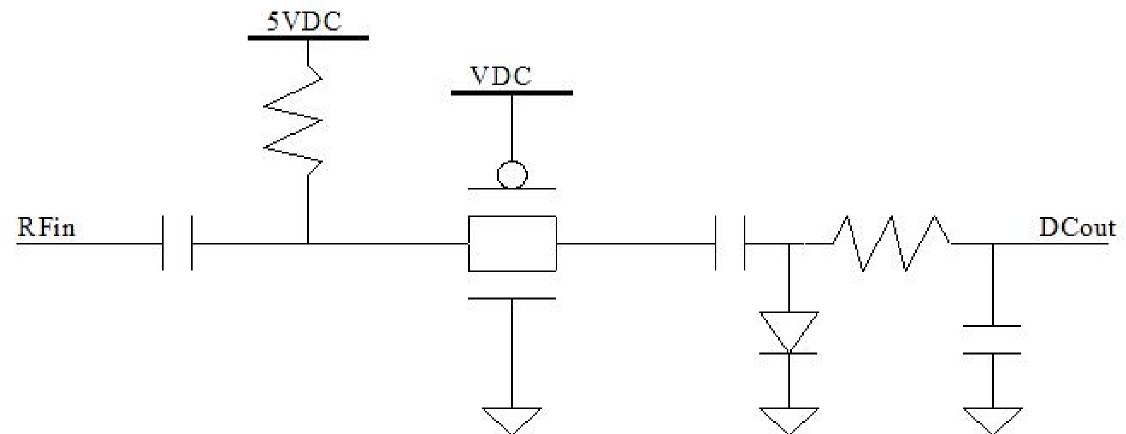
- We are now integrating the Schottky detector with various circuits to characterize change with DC bias
  - Pass Gate
  - Transmission Gate
  - Inverter
  - Self-Biasing Differential Amplifier
- Waiting for fabrication through MOSIS

❑ Layout Schematics

Pass Gate Schematic



Transmission Gate Schematic



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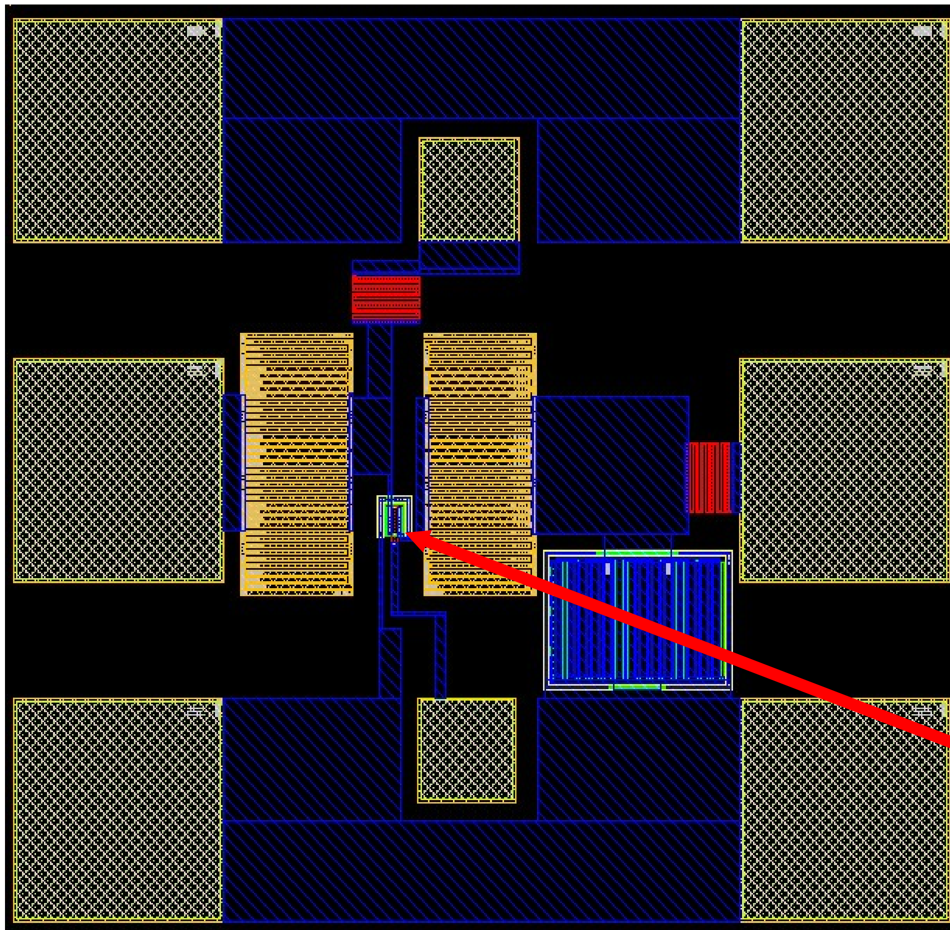
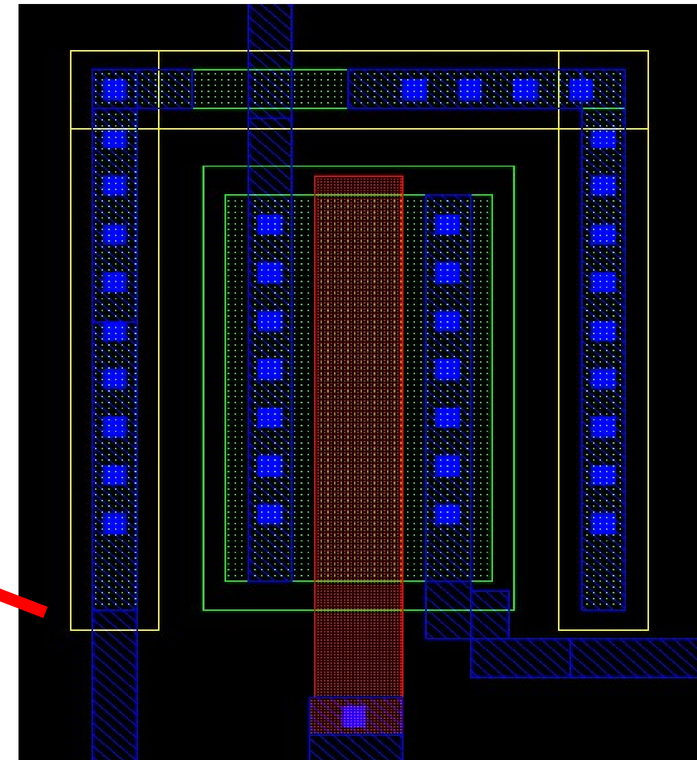
- Layout views

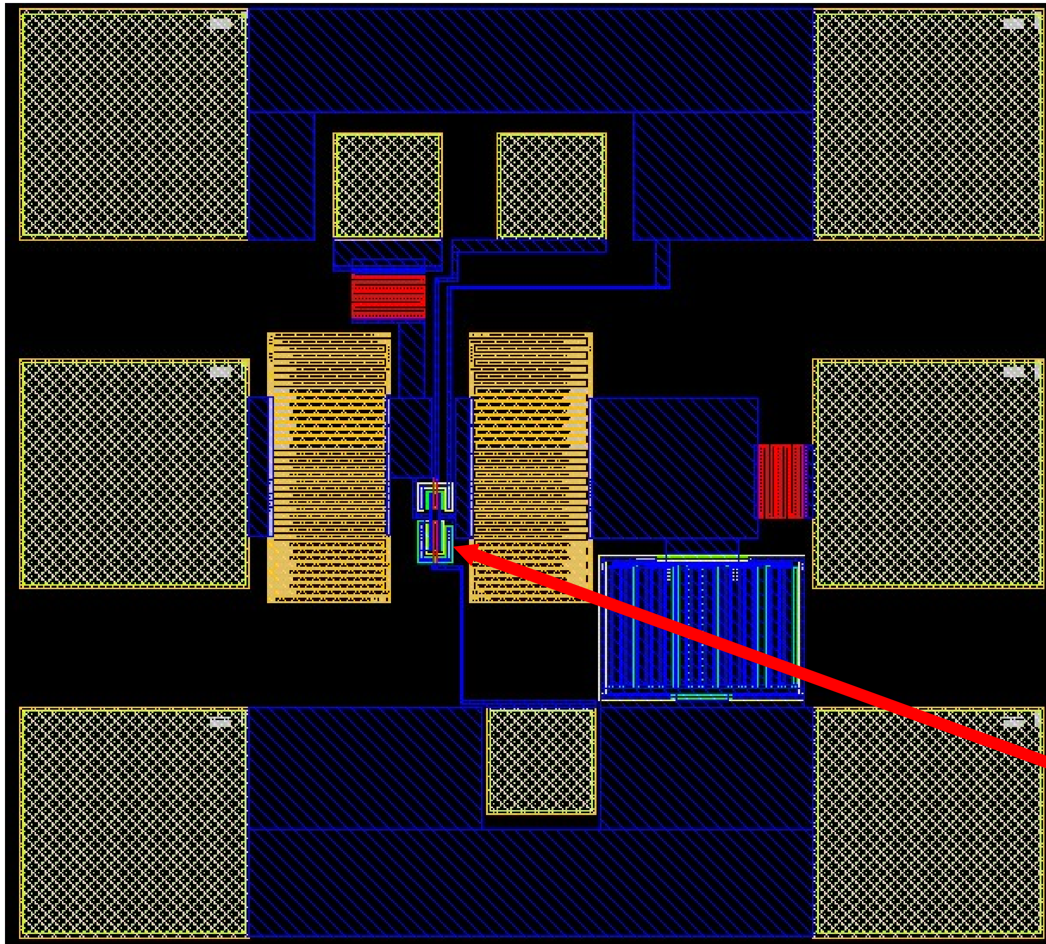


Pass Gate Layout

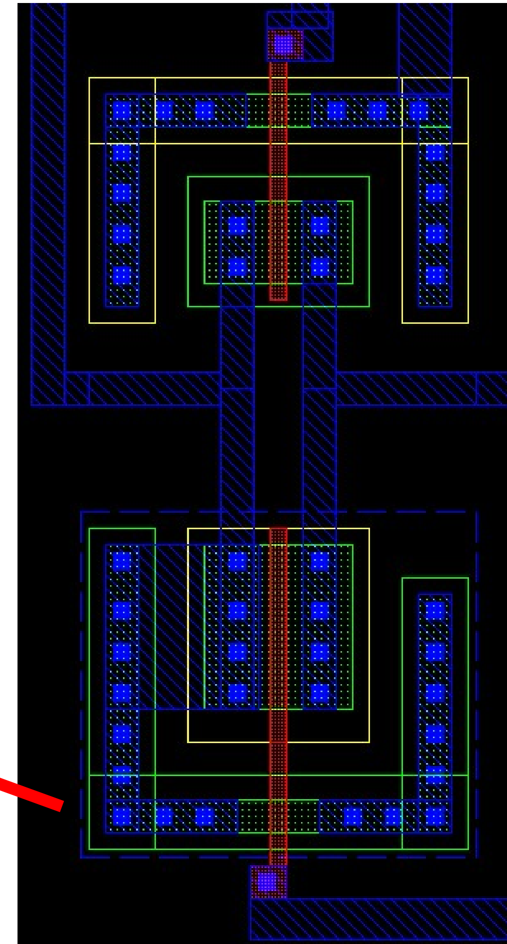


Pass Gate inset

- Layout views cont.



Transmission Gate Layout



TG inset

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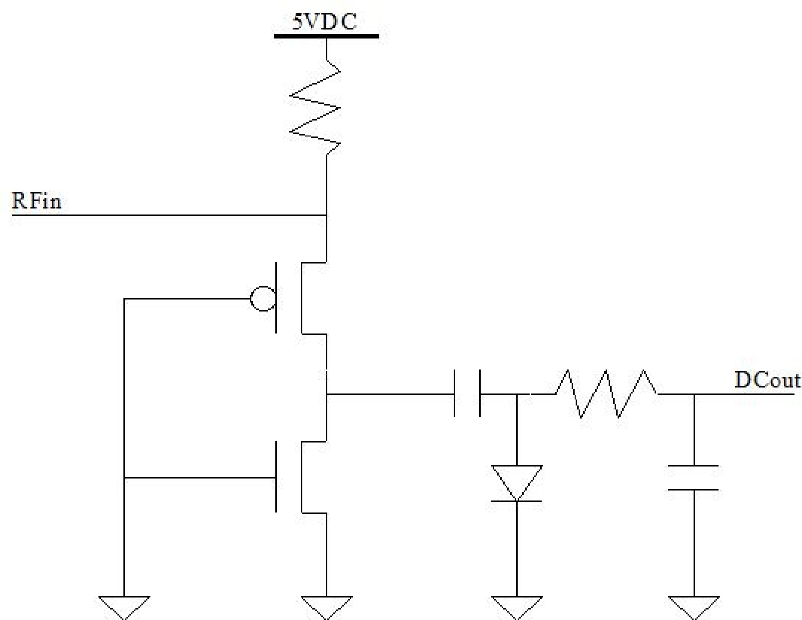
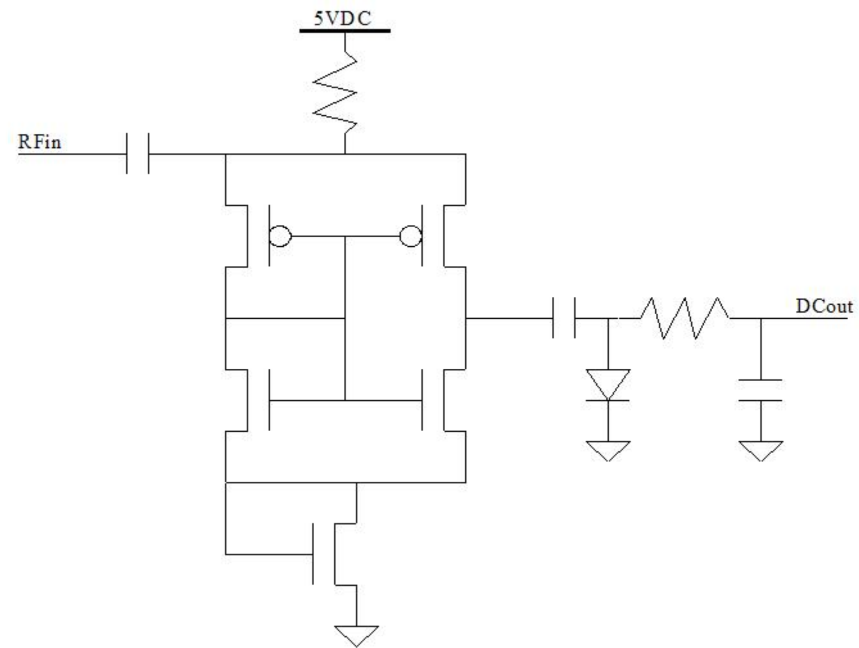
- Layout Schematics cont.

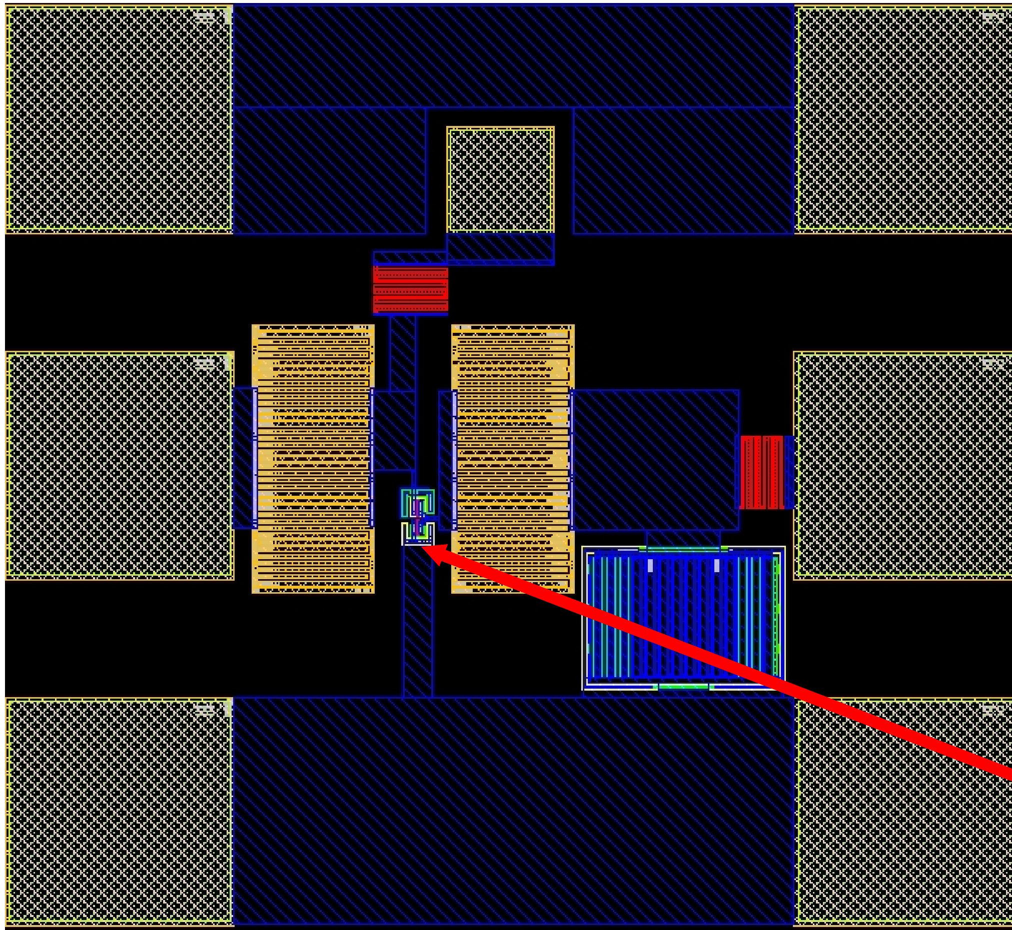
Inverter Schematic



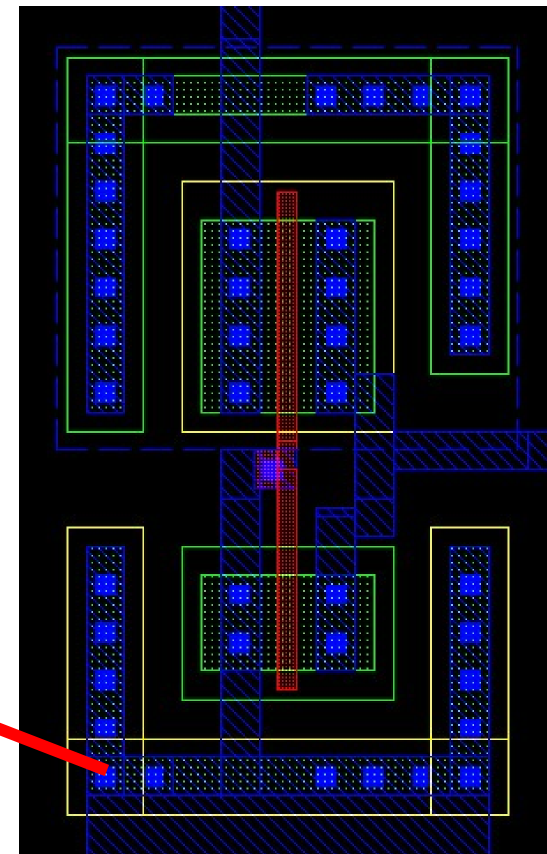
Self-bias diff-amp Schematic



❑ Layout views cont.

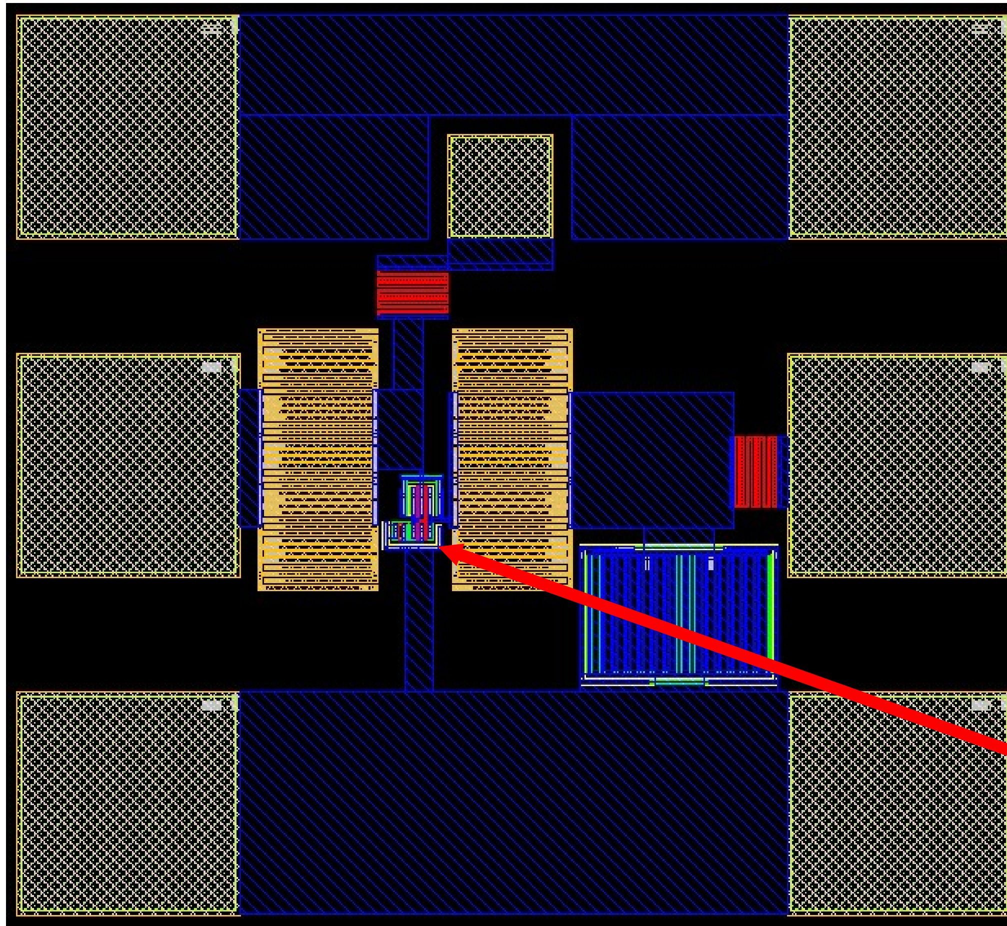


Inverter Layout

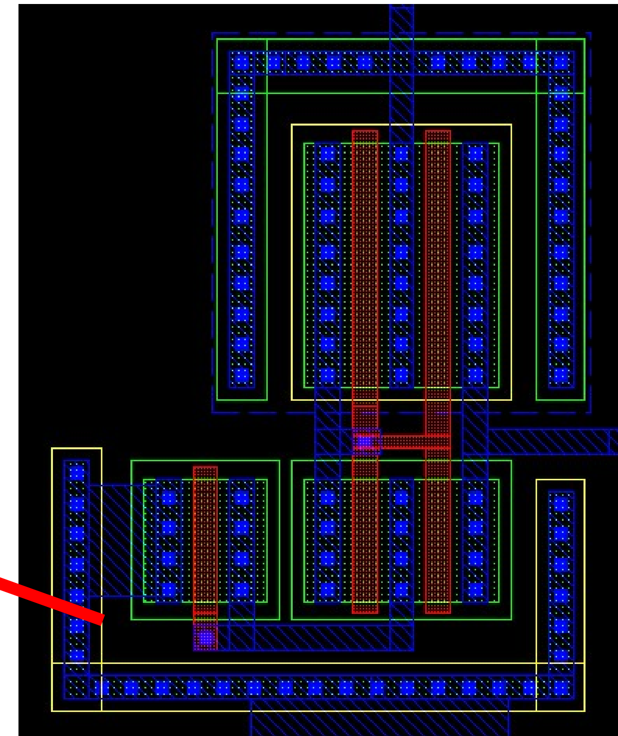


Inverter inset

- Layout views cont.



Layout self-bias diff-amp



Inset diff-amp

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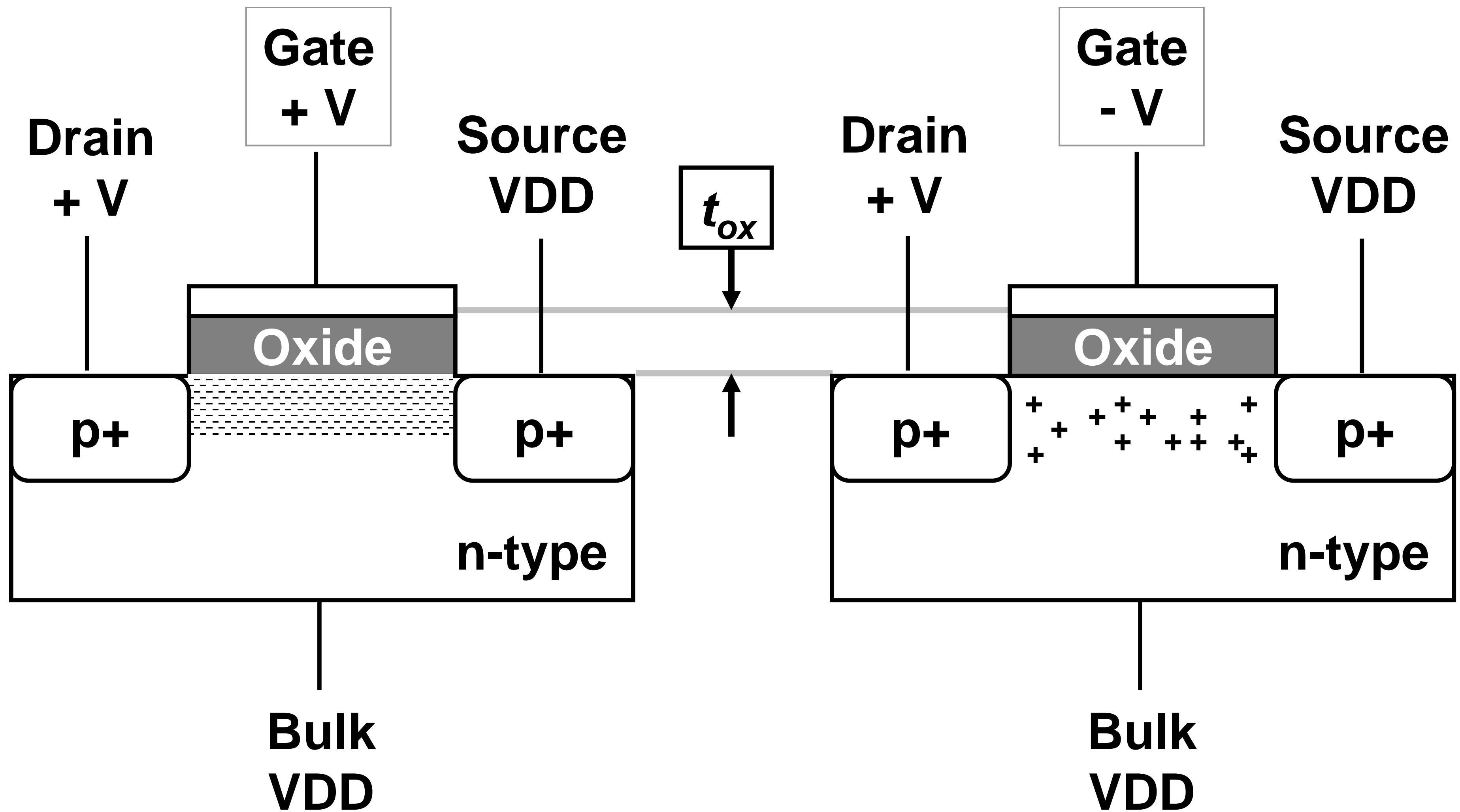
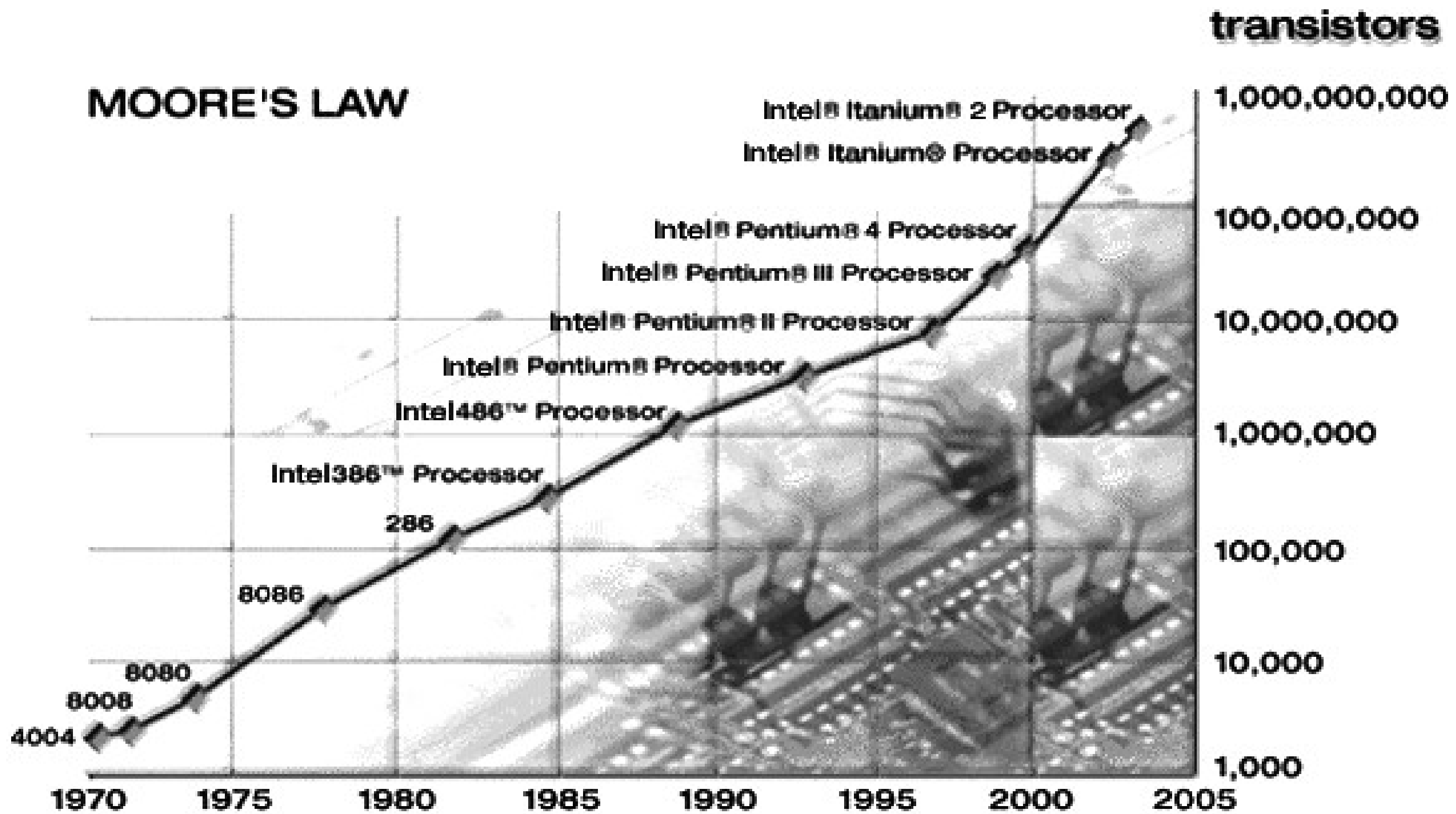
Motivation



Motivation



- Doubling of transistors every couple of years

Gordon Moore. http://www.intel.com/research/silicon/mooreslaw.htm

Motivation

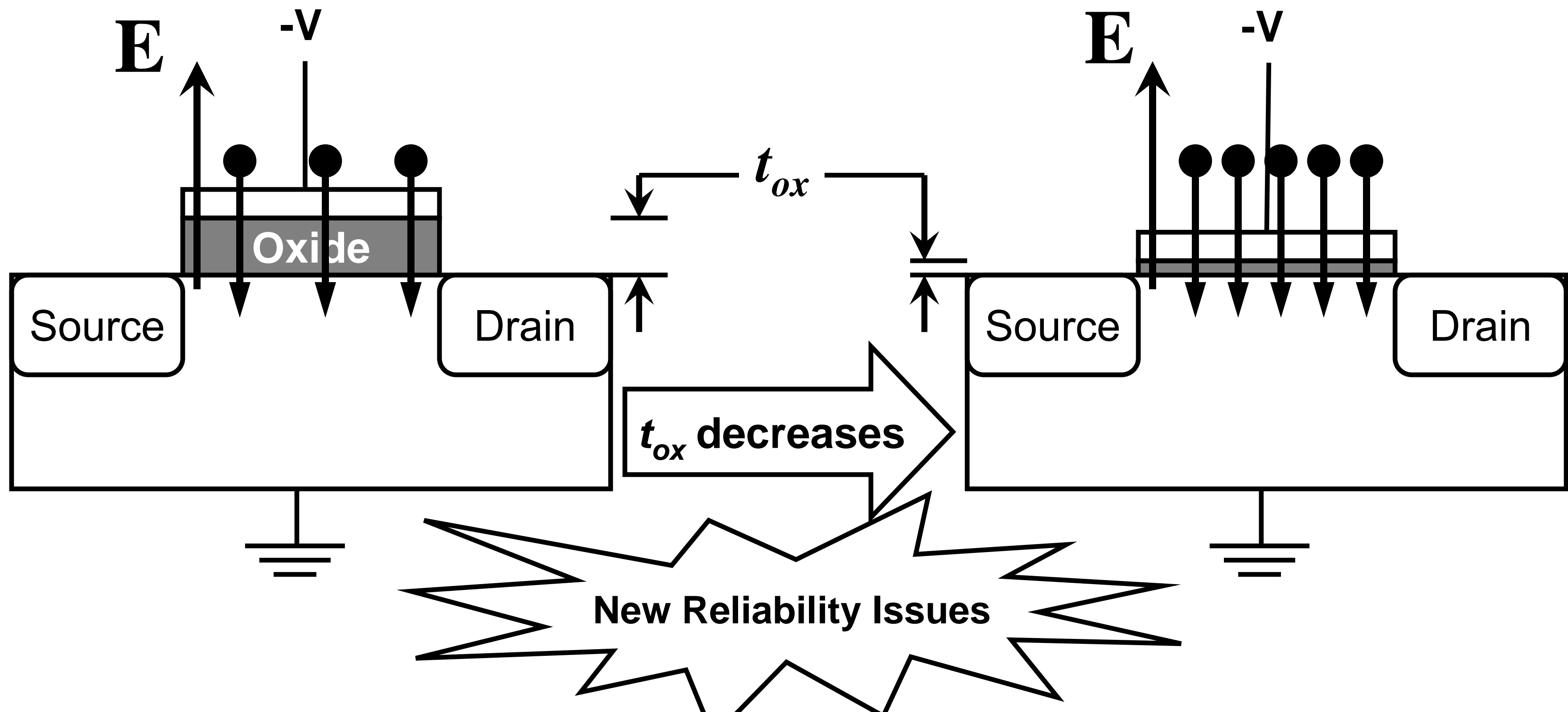
$$E = \frac{V}{t_{ox}}$$

$$E = \frac{1V}{7nm} = 1.4\frac{MV}{cm}$$

$$E = \frac{4V}{7nm} = 5.7\frac{MV}{cm}$$

$$E = \frac{1V}{2.0nm} = 5\frac{MV}{cm}$$

$$E = \frac{4V}{2.0nm} = 20\frac{MV}{cm}$$



[1] R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS: Circuit design, layout, and simulation," IEEE Press, pp. 201-228, 1998.

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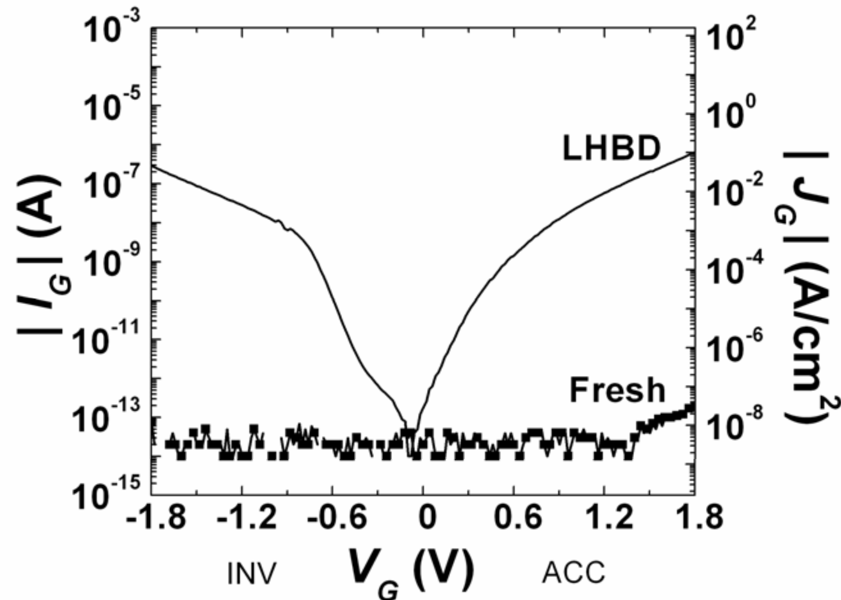
Statement of Work

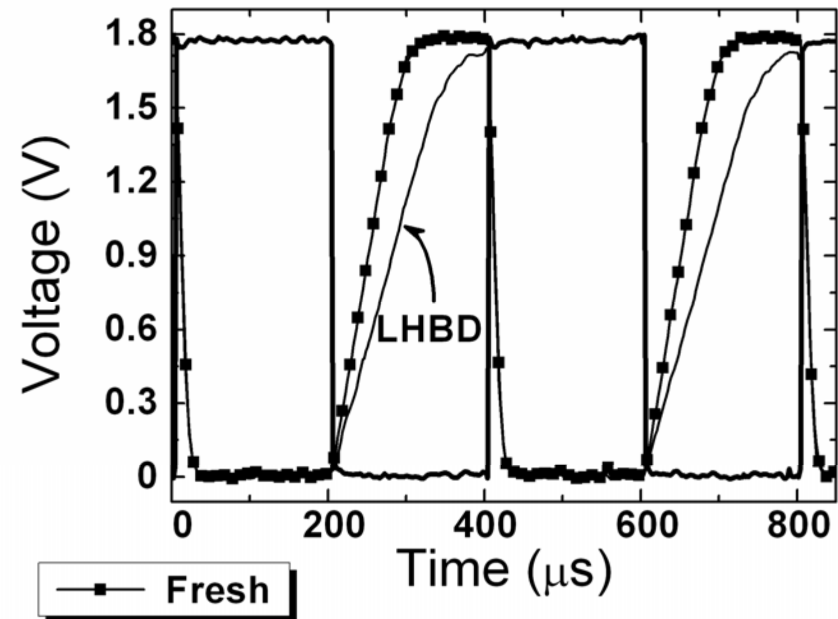
Investigate simple integrated circuit response to low-level leakage current degradation in 2.0 nm gate oxides

How defects accumulated over time in gate oxides affect circuits

Measured Results

Observed effects in 3.2 nm gate oxides:



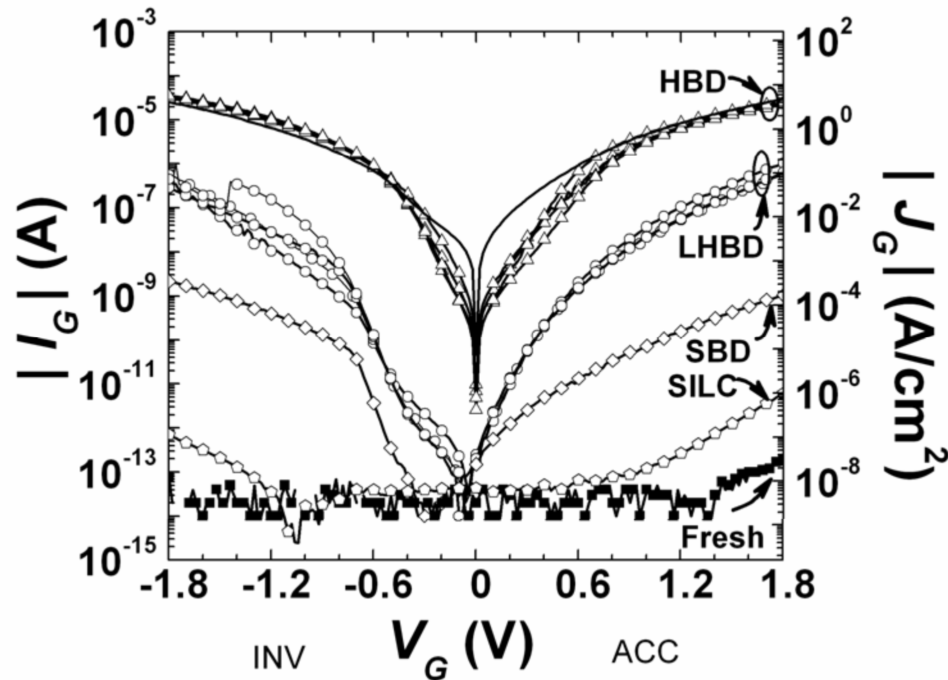


What happens to 2.0 nm gate oxide circuits?

- Will comparable gate oxide degradation produce comparable circuit response?
- Will thinner oxide circuits prove more susceptible to oxide degradation?

Measured Results

3.2 nm Oxide Degradation



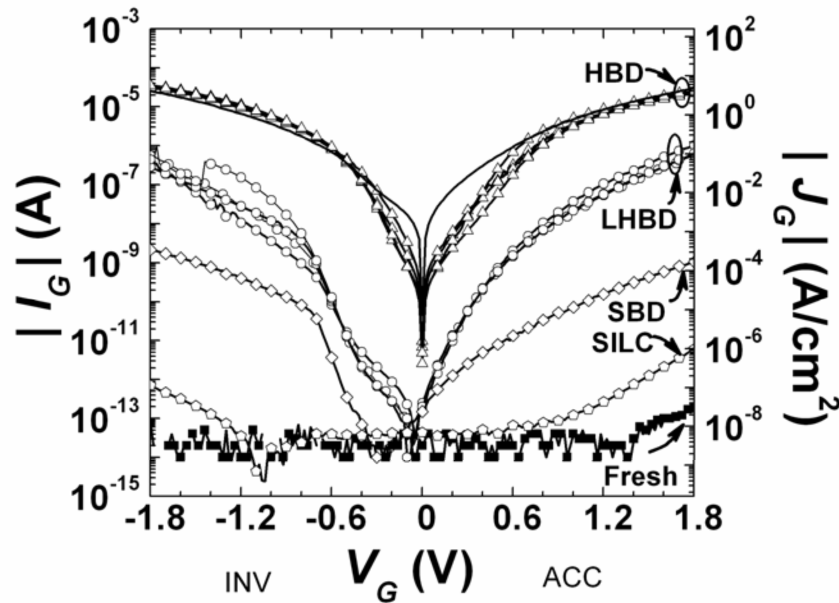
- Observed degradation and breakdown mechanisms:
  - Stressed induced leakage current (SILC)[1,2]
  - Soft breakdown (SBD)[3,4]
  - Limited hard breakdown (LHBD)[5]
  - Hard breakdown (HBD)

- W_P/L_P = 25 µm/ 25 µm
- A_{OX} = 6.25 x 10^{-6} cm^2

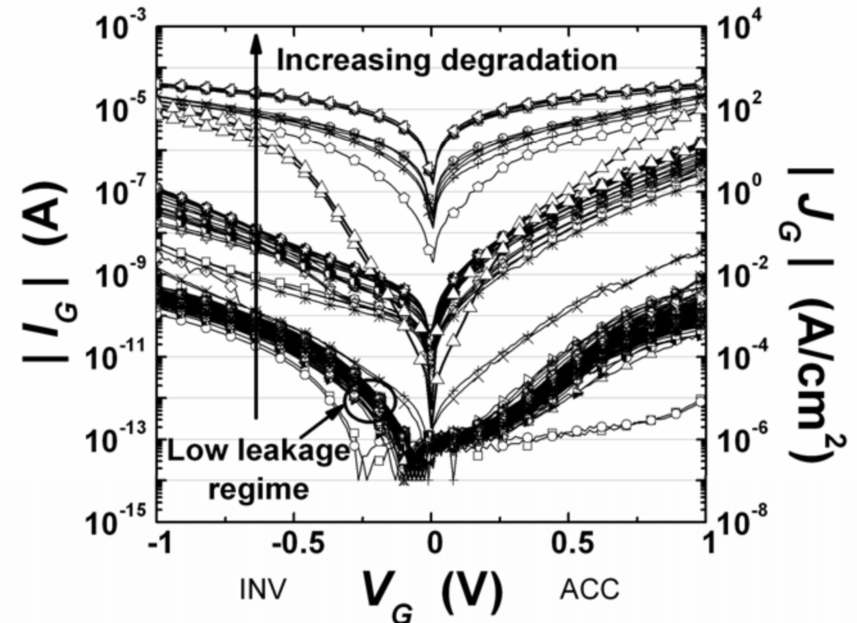
[1] D. J. DiMaria, JAP, vol. 86, pp. 2100-2109, 1999
[2] B. Ricco, et al., IEEE TED, vol. 45, pp. 1154-1555, 1998.
[3] S. Lombardo, F. Crupi, and J. H. Stathis, IEEE IRPS, pp 163-167, 2001.
[4] B. P. Linder, et al., IEEE EDL, vol. 23, pp. 661-663, 2002.
[5] W. B. Knowlton, et al., IEEE International IRW, pp. 87-88, 2001.

Comparison of Oxide Degradation

3.2 nm pMOSFET



2.0 nm pMOSFET



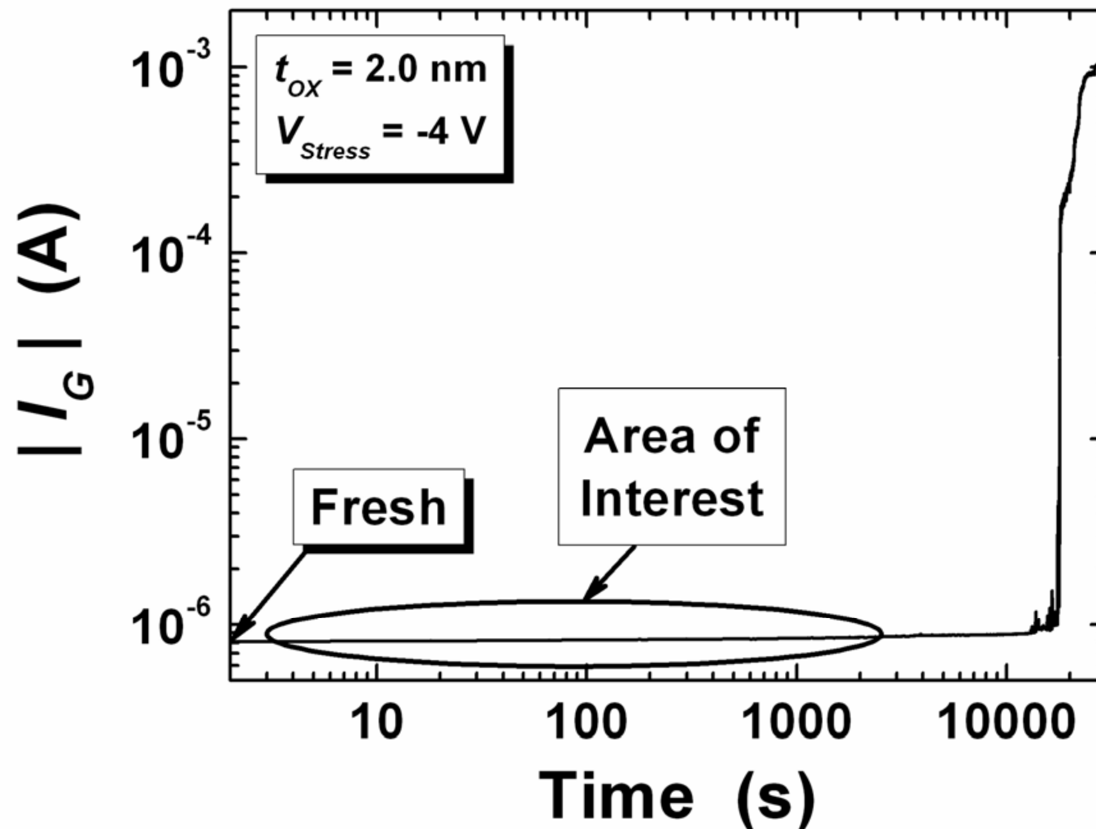
- W_P/L_P = 25 μm/ 25 μm
- A_{OX} = 6.25 x 10^{-6} cm^2

- W_P/L_P = 10 μm/ 1 μm
- A_{OX} = 1 x 10^{-7} cm^2

BD Mechanisms less clear for 2.0 nm → focus on low leakage regime

CVS Technique

- Focus on low leakage regime



[1]S. Lombardo, J. H. Stathis, and B. P. Linder, PRL, vol. 90, 2003. [2]S. Lombardo, et al., "Breakdown transients in ultra-thin gate oxynitrides," presented at IEEE ICICDT, 2004. [3]D. J. DiMaria, JAP, vol. 86, pp. 2100-2109, 1999. [4]B. Ricco, et al., IEEE TED, vol. 45, pp. 1154-1555, 1998.

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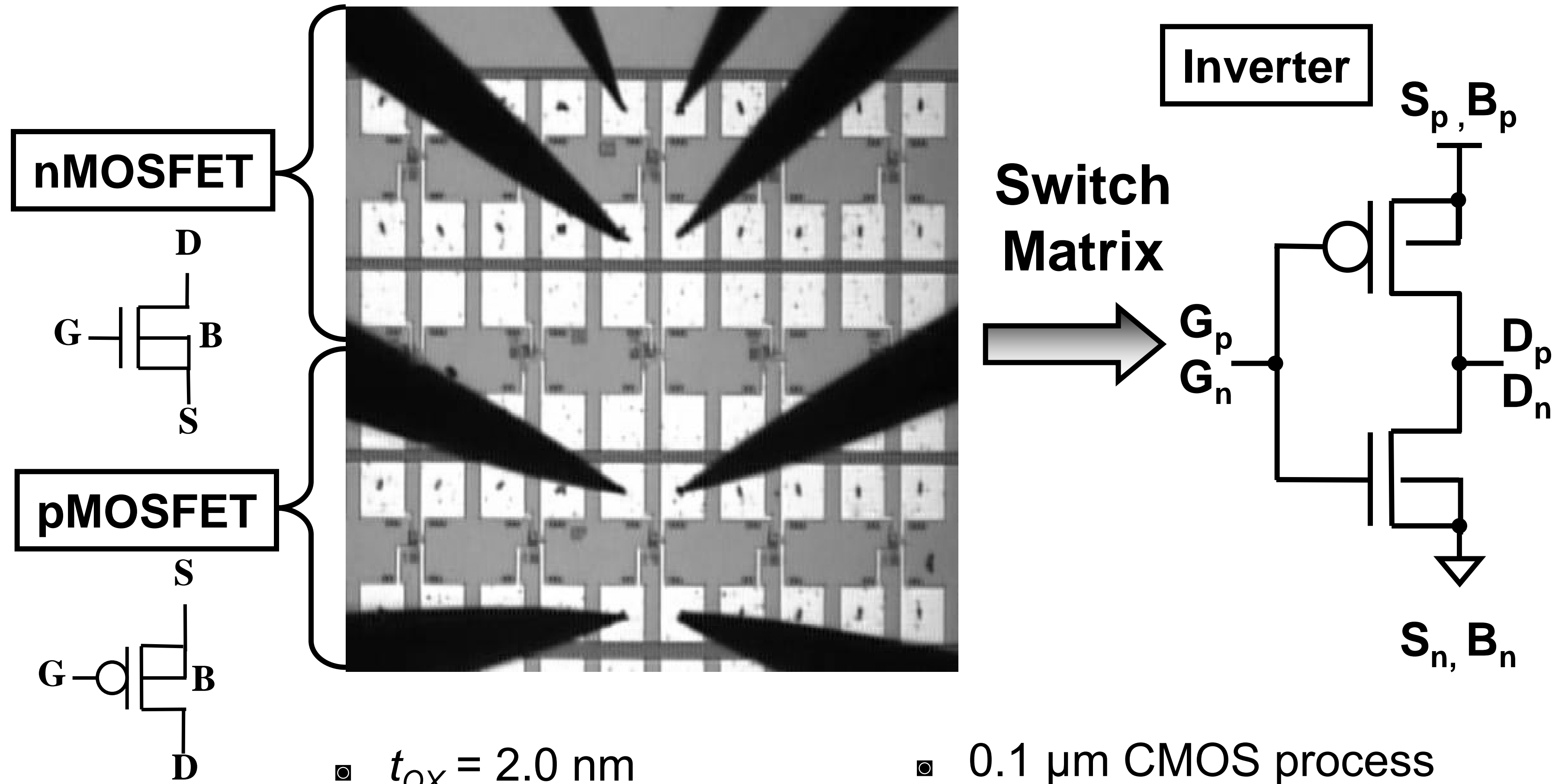
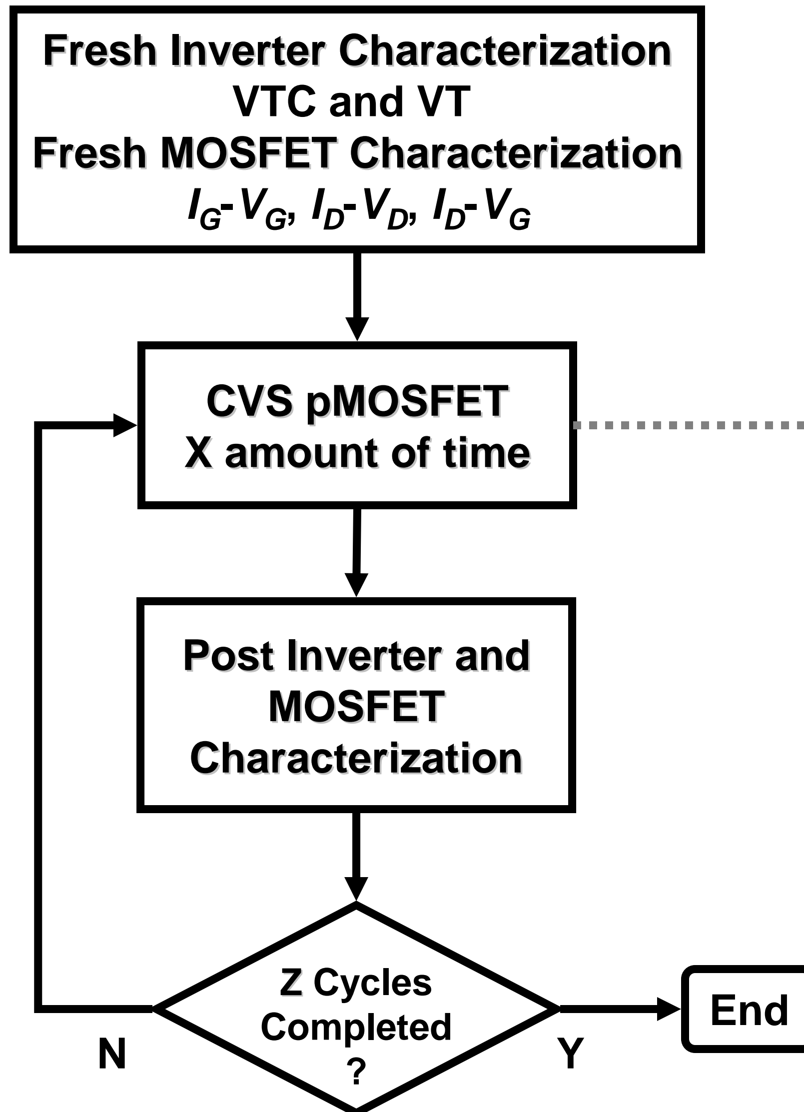
Experimental

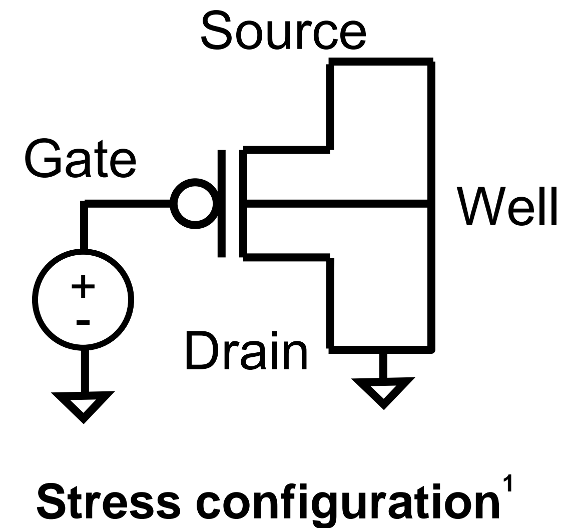
Wafer-level stress and characterization



- t_{OX} = 2.0 nm
- $W_{P,N}/L_{P,N}$ = 10 μm/1 μm
- 0.1 μm CMOS process
- Nominal operating voltage: 1 V

Experimental Procedure



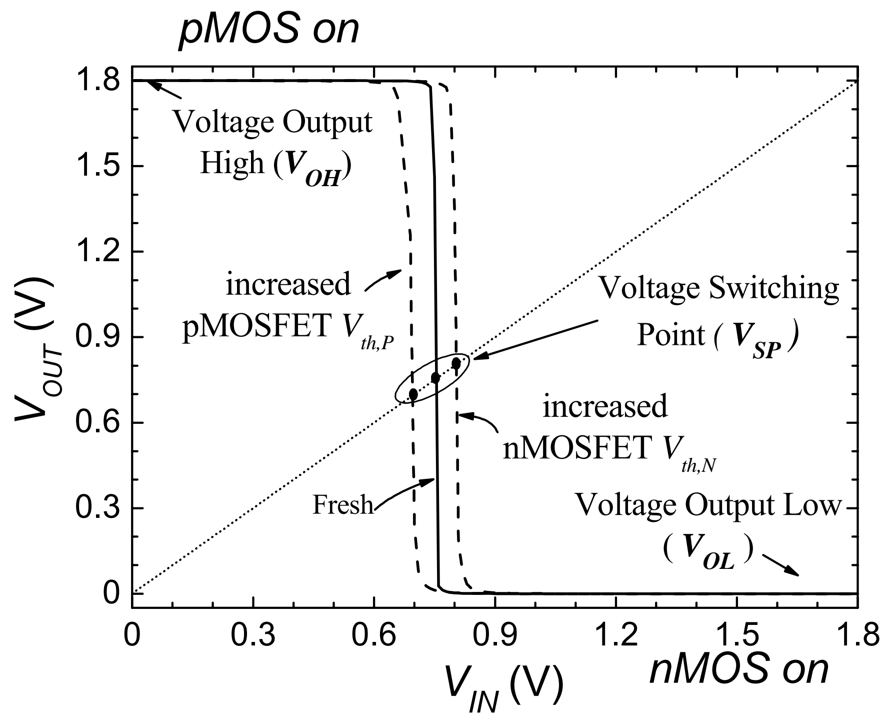


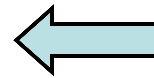
Stress configuration[1]

[1]F. Crupi, *et al.*, *IEEE TED*, vol. 48, pp. 1109-1113, 2001

Experimental Procedure

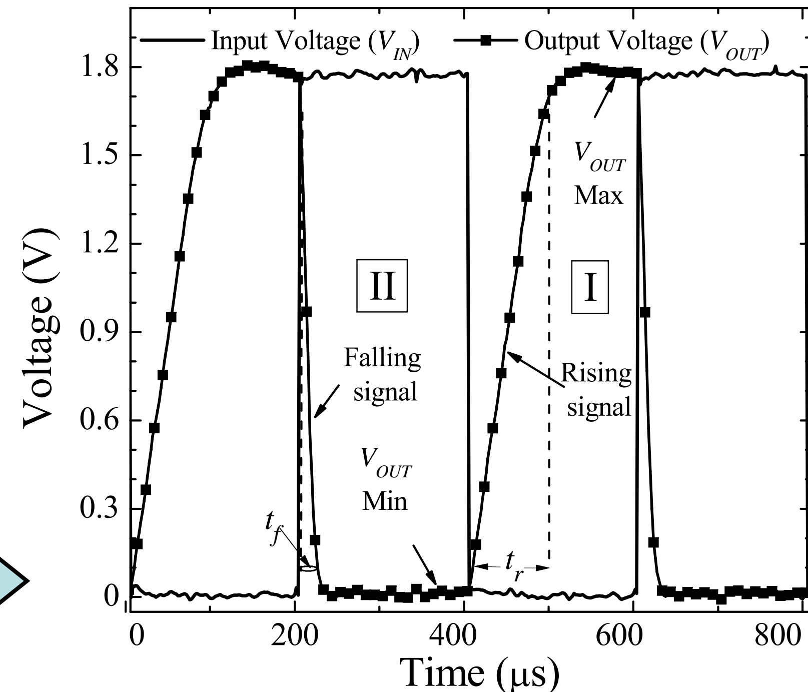
- Inverter parameters defined



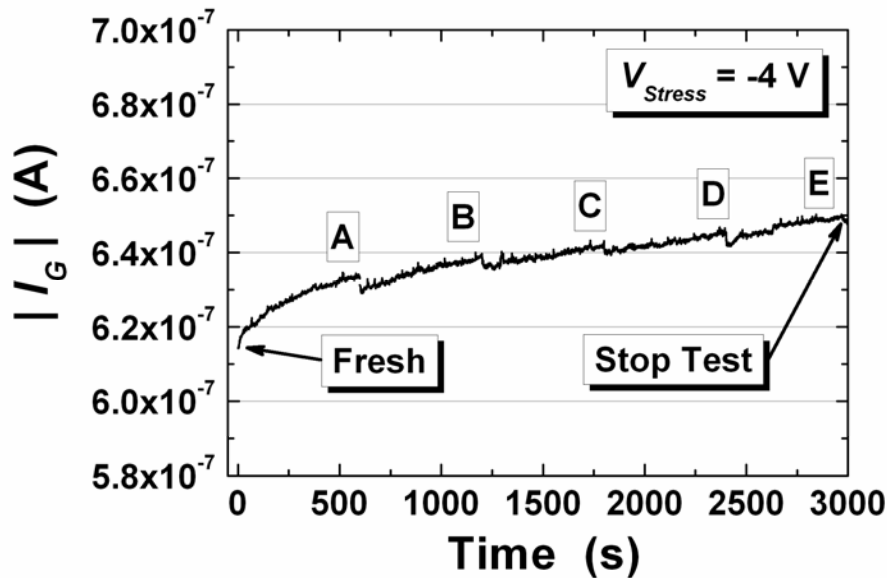


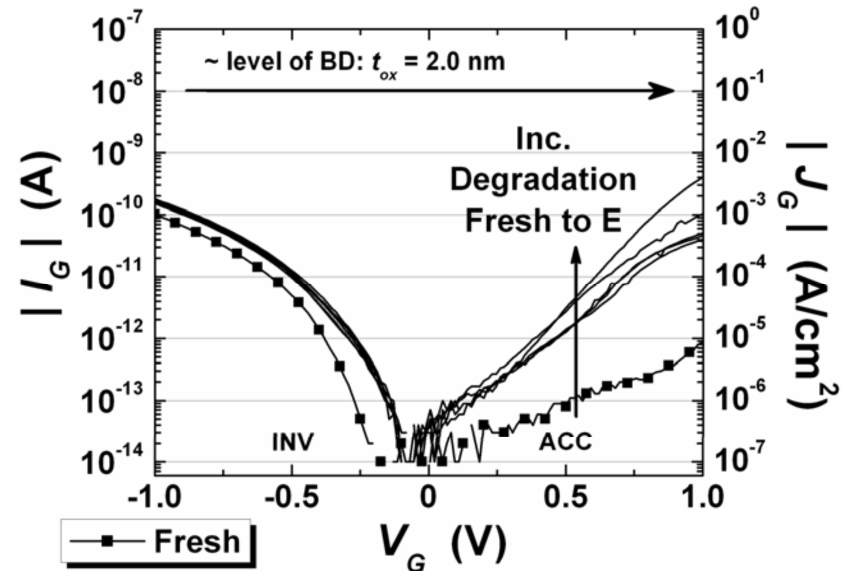
Sample voltage transfer characteristics (*VTC*)

Sample voltage-time (*V-t*) domain



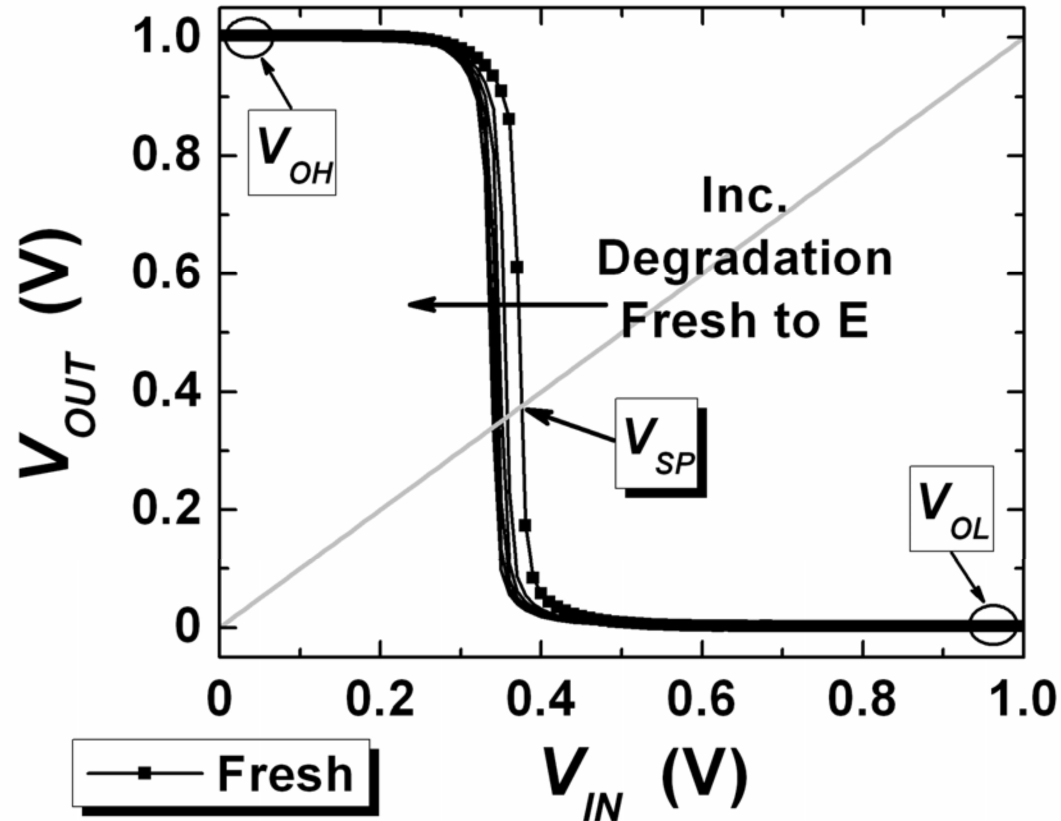
PMOSFET CVS and I_G-V_G





- Observed gate leakage current increase (2.0 nm)
  - Accumulation mode ~ 2 to 3 orders of magnitude
  - Inversion mode < 1 order of magnitude

Inverter Voltage Transfer Characteristics



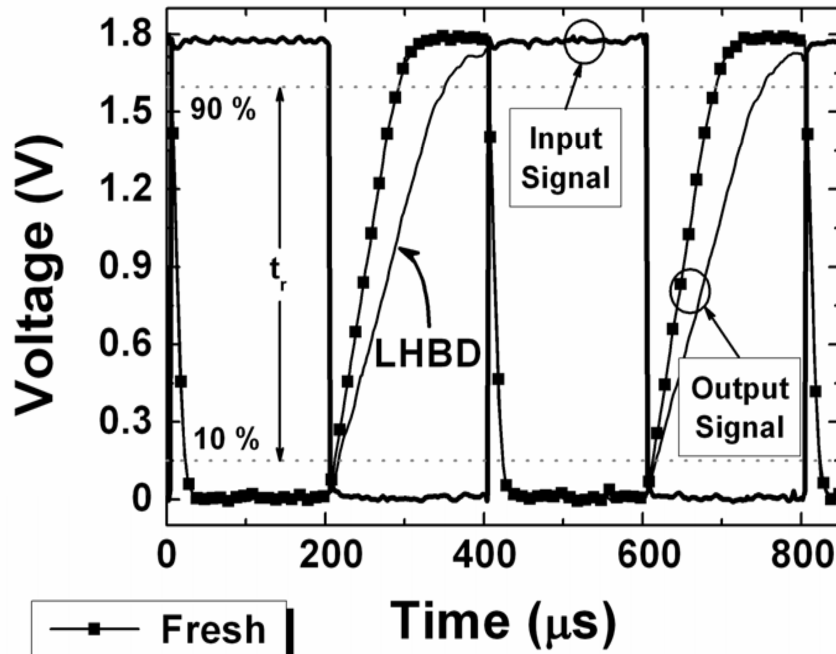
Fresh → E level degradation:

- ΔV_{SP} ~8% shift left[1]
- Output behavior transitions from 1 to 0

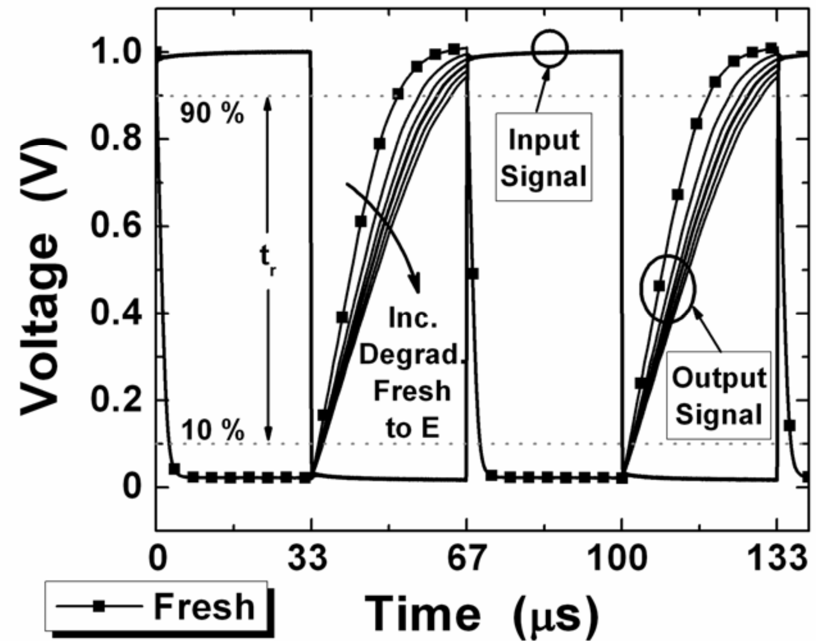
[1] R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS: Circuit design, layout, and simulation," IEEE Press, pp. 201-228, 1998.

Inverter Time Domain

3.2 nm pMOSFET



2.0 nm pMOSFET



Fresh → LHBD

Δ rise time[1] ~32%

Fresh → E level degradation

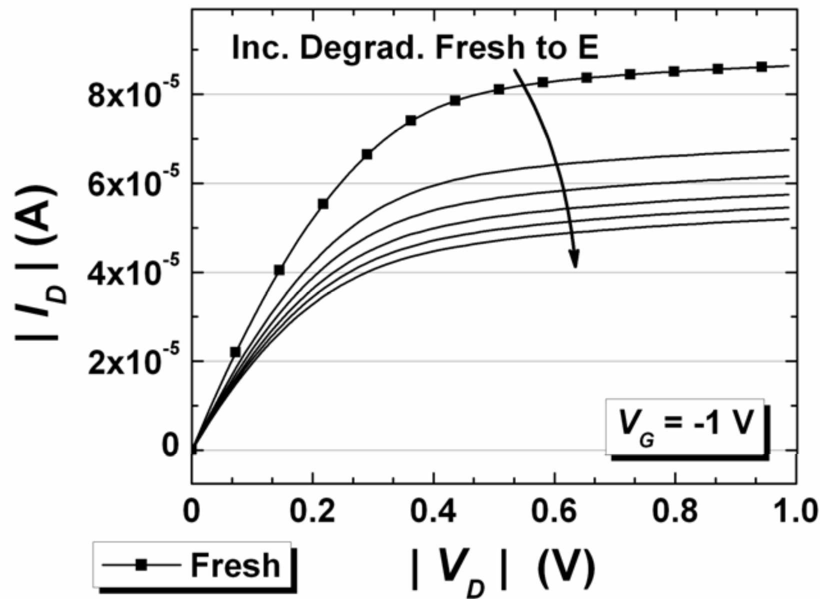
Δ rise time[1] ~36% to 62%

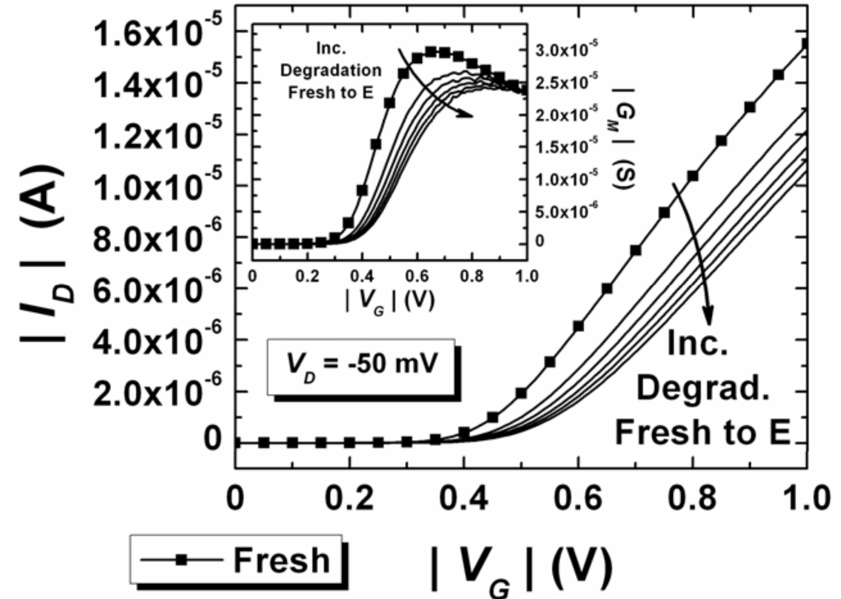
[1]R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS: Circuit design, layout, and simulation," IEEE Press, pp. 201-228, 1998.

Degraded Inverter Characteristics – Why?

What aspect of device characteristics may be causing the inverter to respond to the degradation in this manner?

PMOS I_D-V_D (Drive Current)



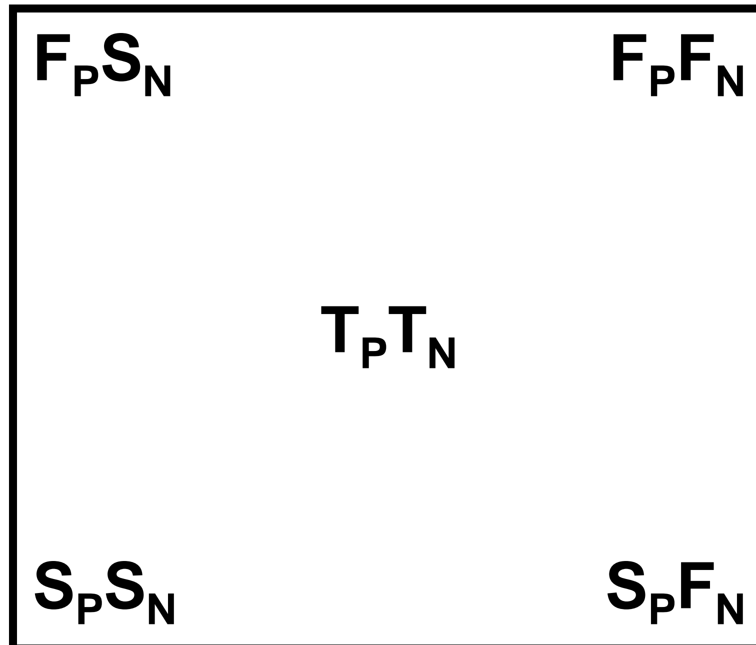


Fresh → E level degradation:

- Δ I_{Drive} ~40% decrease
- Δ $V_{TH,P}$ ~17% to 20% shift
- Δ $G_{M,\ MAX}$ ~16% to 19% decrease

2.0 nm pMOSFET

Relation to Logic Technology



"Corner Parameters"[1]

Fresh → E level degradation:

- $\Delta\ I_{Drive}$ ~40% decrease
- $\Delta\ V_{TH,P}$ ~17% to 20% shift
- $\Delta\ G_{M,\ MAX}$ ~16% to 19% decrease

Typical logic process:

- $\Delta\ I_{Drive}$ ~6% decrease
- $\Delta\ V_{TH,P}$ ~10% shift
- $\Delta\ G_{M,\ MAX}$ ~7% decrease

[1]MOSIS, "AMIS C5N/C5F Family Process: SPICE corner models, "4676 Admirality Way, Marina del Ray, California 90292-6695 USA, 2004.

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Conclusions

- Dramatic decrease in inverter performance directly related to:
  - $\Delta\ I_{Drive}$ (decrease)
  - $\Delta\ V_{TH,P}$ (increase) and $\Delta\ G_M$ (decrease)
- For thinner oxides:
  - Inverter circuits more sensitive to degradation
  - Circuit failure may result before a definite BD event

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Future Work

- NMOS degradation
  - Circuit operation effects
  - Devices effects
- Circuit level inverter stress
  - Circuit operation effects
  - Device effects
- Modeling inverter performance

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2004 Publication Summary

Cheek, Betsy J., Stutzke, Nate, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton, *Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics*, in proceedings of the 2004 IEEE International Reliability Physics Symposium (April, 25-29, 2004) pp. 110-116.

M. L. Ogas, R. G. Southwick III, B. J. Cheek, C. E. Lawrence, S. Kumar, A. Haggag, R. J. Baker, W. B. Knowlton, *Multiple Waveform Pulse Voltage Stress (MWPVS) Technique for Modeling Noise in Ultra Thin Oxides*, poster presentation at 2004 IEEE Workshop on Microelectronics and Electron Devices (April 16, 2004).

Dorian Kiri, Michael L. Ogas, Ouahid Salhi, Richard G. Southwick III, Gennadi Bersuker, Betsy J. Cheek, William B. Knowlton, *Investigation of Ultra Thin Gate OxideReliability in MOS Devices and Simple ICs*, poster presentation at 2004 IEEE Workshop on Microelectronics and Electron Devices (April 16, 2004).

M. L. Ogas, R. G. Southwick III, B. J. Cheek, R. J. Baker, G. Bersuker, W. B. Knowlton, *Survey of Soft Breakdown (SBD) in 2.0 nm Gate Oxides in MOS Devices and Inverter Circuits*, accepted for oral presentation at 2004 IEEE International Integrated Reliability Workshop (Oct, 20-23, 2004).

Betsy J. Cheek, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton, *Examination of Transistor-Level Current Limited Hard Breakdown (LHBD) and Its Effect on CMOS Inverter Circuit Operation*, submitted for publication to IEEE Transactions on Electron Devices.