Electromagnetic Effects on Modern Electronic Devices and Circuits: Modeling and Experiments

Neil Goldsman

Dept. of Electrical and Computer Engineering, UMCP

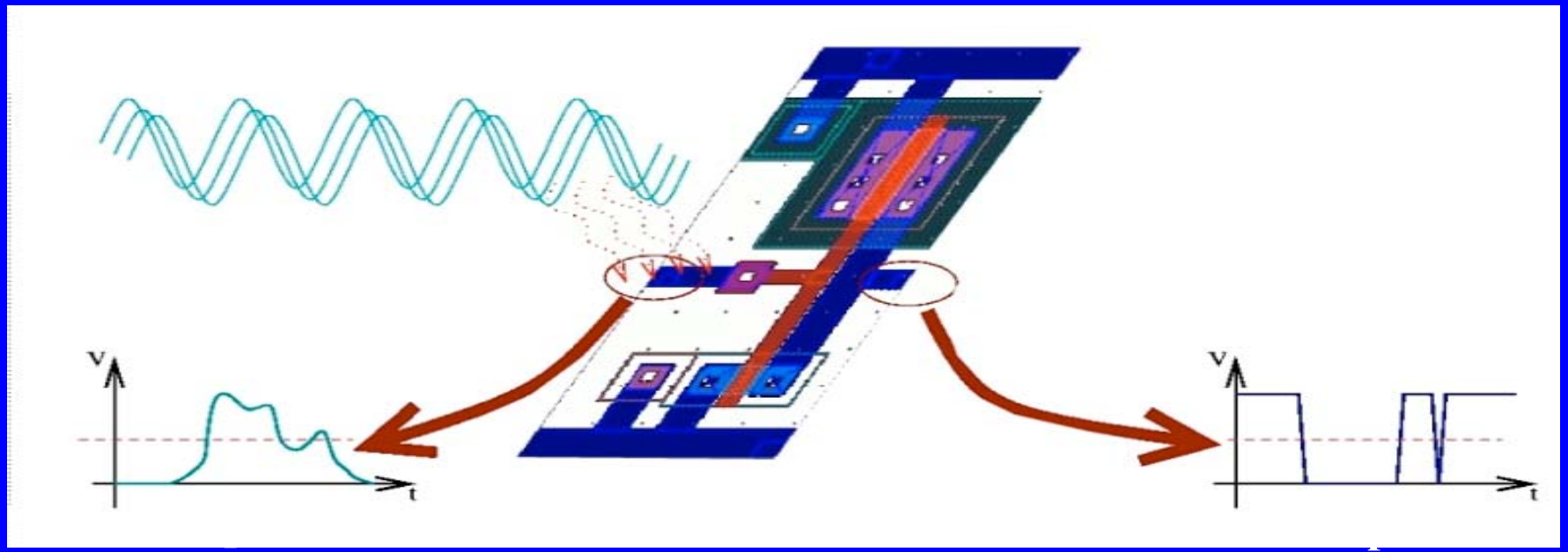
Collaborators so far: B. Jacob, V. Granatstein, A. Akturk, Z. Dilli, Y. Bai, T. Firestone, S. Adl

Outline

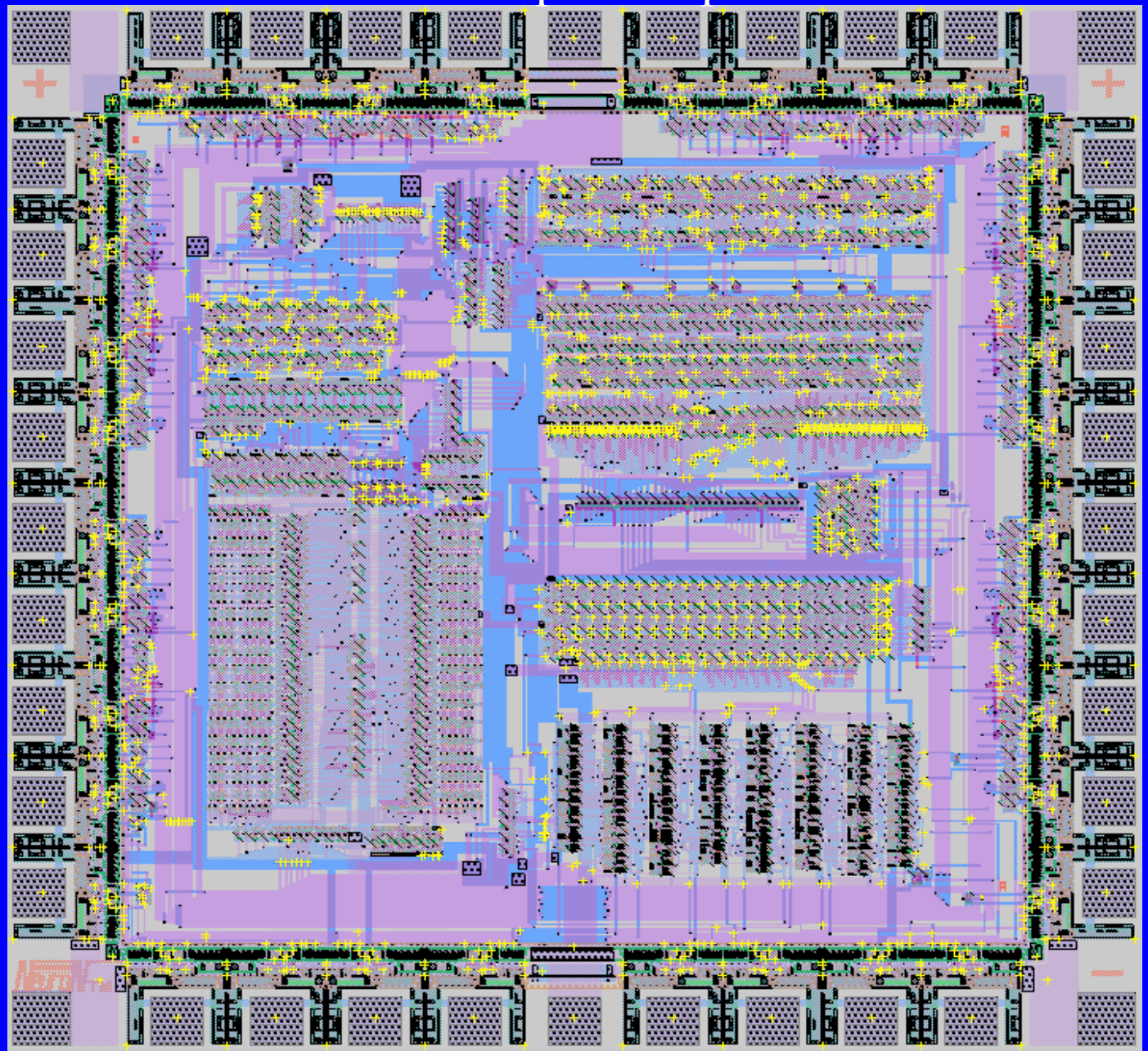
EM Coupling: Levels Investigated

- Device Level (Modeling)
- Interconnects and Passive Elements (Modeling)
- Circuit Prototyping and Testing for EM Coupling (Experiment)

CMOS INVERTER



EM Related Problems in Integrated Circuits
Example Chip



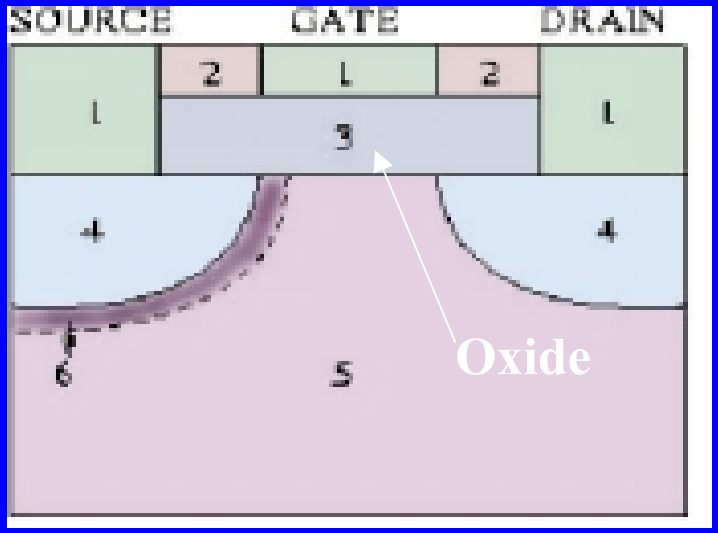
Task 1: Numerical Modeling & Analysis of EM Effects on Nanoscale Devices

Issues:

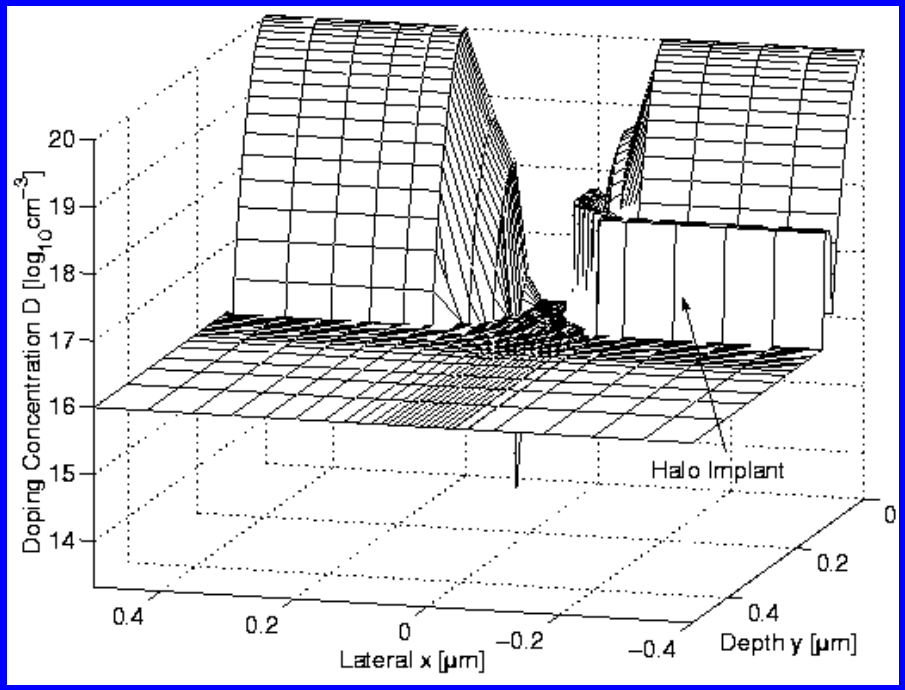
- Chips can contain millions of nanoscale transistors (MOSFETs)
- MOSFETs are very fragile, with gate lengths of 0.2μm and below, and oxide thickness of 35Å.
- EM pulses can couple to device terminals and alter voltage levels
- Such terminal voltage changes can radically alter I-V characteristics and if large enough, can destroy device though oxide breakdown and/or filament formation related to excessive avalanching.

Use Numerical Modeling of Nanoscale Devices to help understanding and to predict consequences of EM coupling to terminals, and to present design alternatives for safeguarding against coupling effects.

Modeling: Use Detailed Device Modeling to Quantify Transistor Failures (MOSFETs)



MOSFET Cross-Section
Gate Length: 0.14µm
Oxide Thickness 35Å



Doping Profile

Solve Transient Semiconductor Device Eqns. Numerically in 2D

DD Equations

$$\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}}(p - n + D)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . \vec{J}_n - R_n + G_n$$

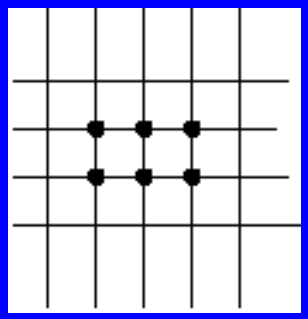
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . \vec{J}_p - R_p + G_p$$

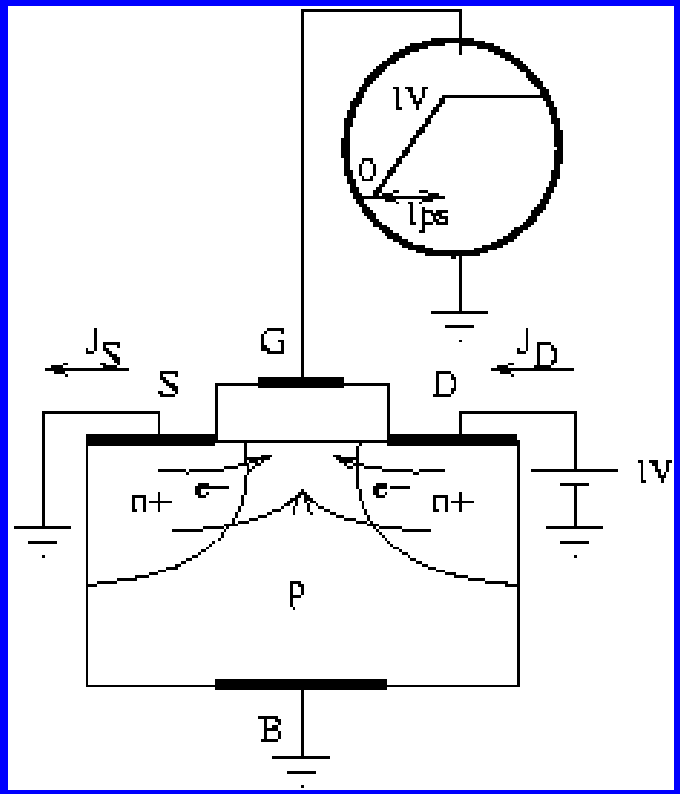
Supplementary DD Equations

$$\vec{J}_n = -q\mu_n n\vec{\nabla\Phi} + q\mu_n V_T \vec{\nabla n}$$

$$\vec{J}_p = -q\mu_p p\vec{\nabla\Phi} - q\mu_p V_T \vec{\nabla p}$$

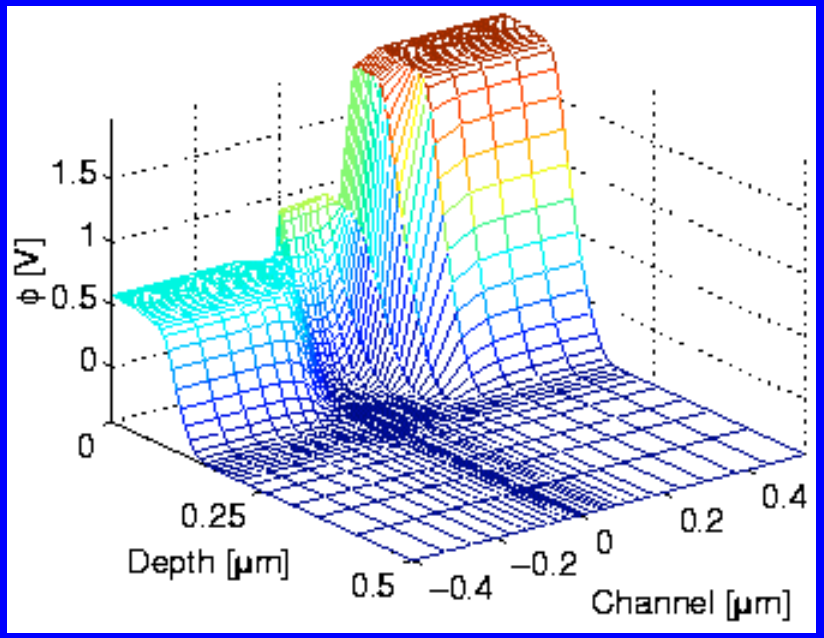
Coupled Discretized DD Equations are solved at each mesh point

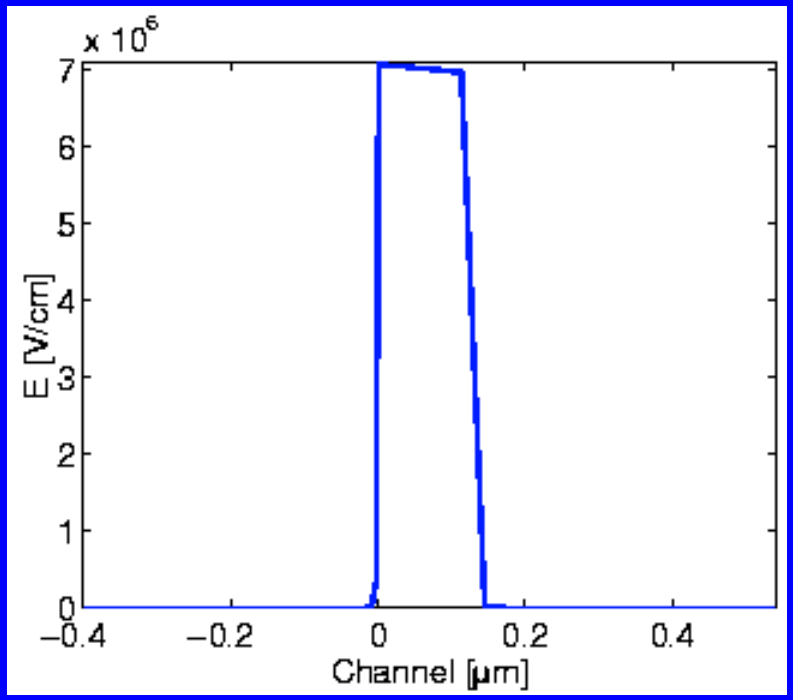




Results give I-V and Potential, Charge Concentrations, Current Densities inside device.

Resulting Electrostatic Potential inside 0.14μm MOSFET: Bias Conditions for Oxide Breakdown





V_G=2.8V V_D=1.4V V_S=V_B=0V

If $|E_y|$ > 7MV/cm => Oxide Breakdown

Device Simulations predicts induced gate voltage of 2X supply causes MOSFET oxide damage

Distributed Circuit Simulations (Inverter)

DD Equations

$$\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}}(p - n + D)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . \overrightarrow{J_n} - R_n + G_n$$

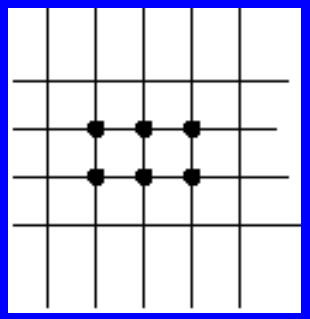
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . \overrightarrow{J_p} - R_p + G_p$$

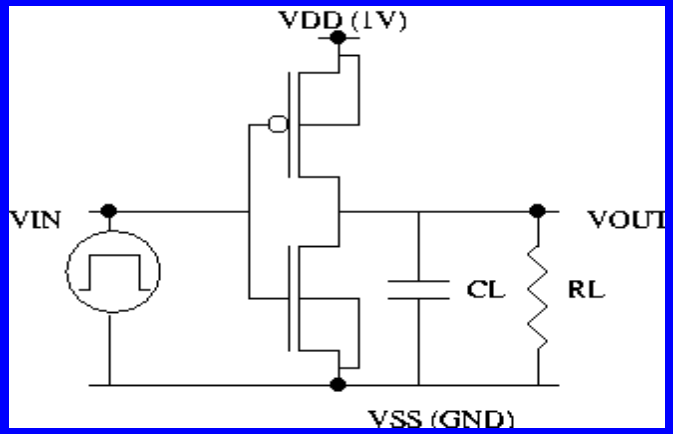
Supplementary DD Equations

$$\overrightarrow{J_n} = -q\mu_n n\overrightarrow{\nabla\Phi} + q\mu_n V_T \overrightarrow{\nabla n}$$

$$\overrightarrow{J_p} = -q\mu_p p\overrightarrow{\nabla\Phi} - q\mu_p V_T \overrightarrow{\nabla p}$$

Coupled Discretized DD Equations are solved at each mesh point





CMOS Inverter (CMI)

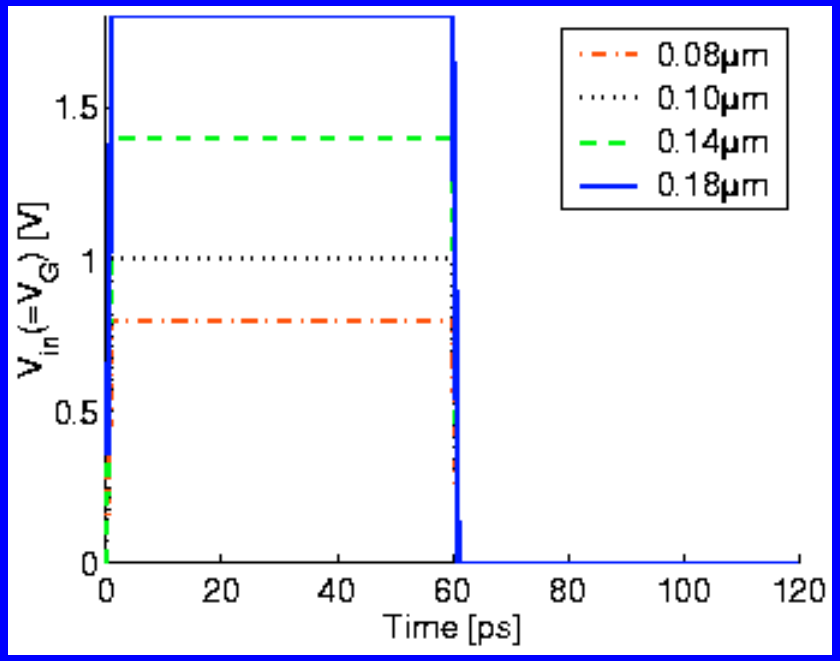
Lumped KCL equation check at the output node and using the KCL equation, the output guess is updated for the next iteration, V_O^{i+1}:

$$I_{DN} - I_{DP} + I_{R_L} + I_{C_L} = 0$$

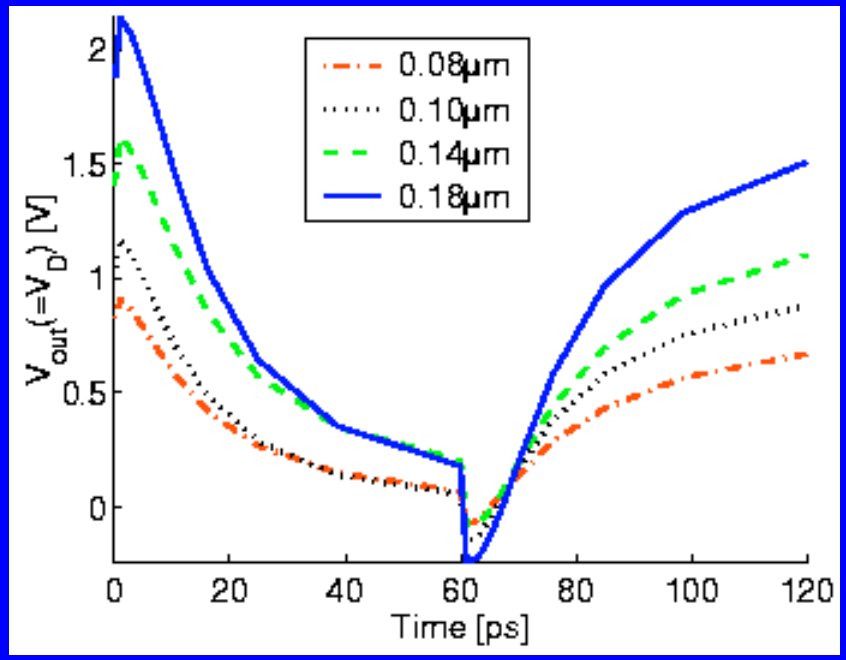
$$A_N + B_N V_o^{i+1} + A_P + B_P V_o^{i+1} + \frac{V_o^{i+1} - V_{SS}}{R_L} + C_L \frac{V_o^{i+1} - V_o^i}{\Delta t} = 0$$

$$V_o^{i+1} = \frac{V_{SS} + V_o^i \frac{R_L C_L}{\Delta t} - (A_N + A_P)R_L}{1 + \frac{R_L C_L}{\Delta t} + (B_N + B_P)R_L}$$

Inverters with Different Gate Lengths: Simulated Response to 60psec Pulse Input



Input



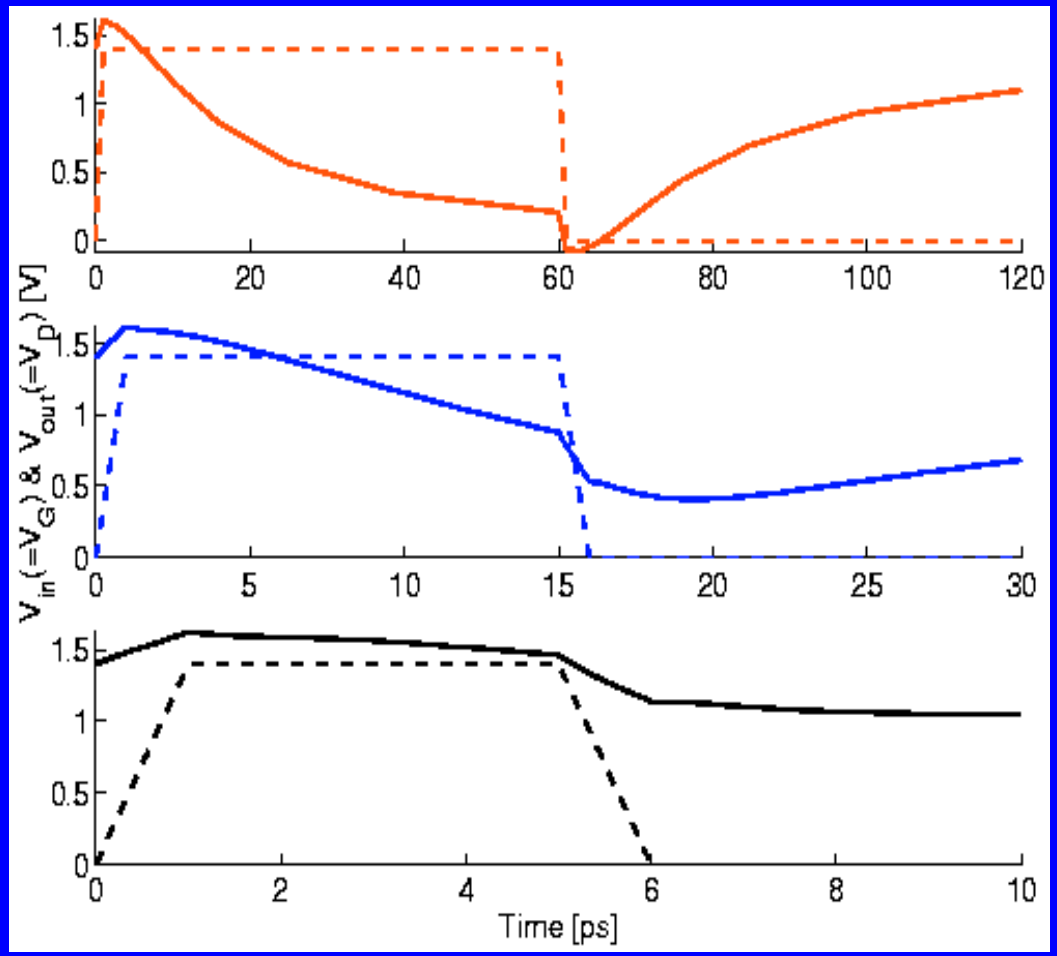
Output

Devices scaled according to design rules.

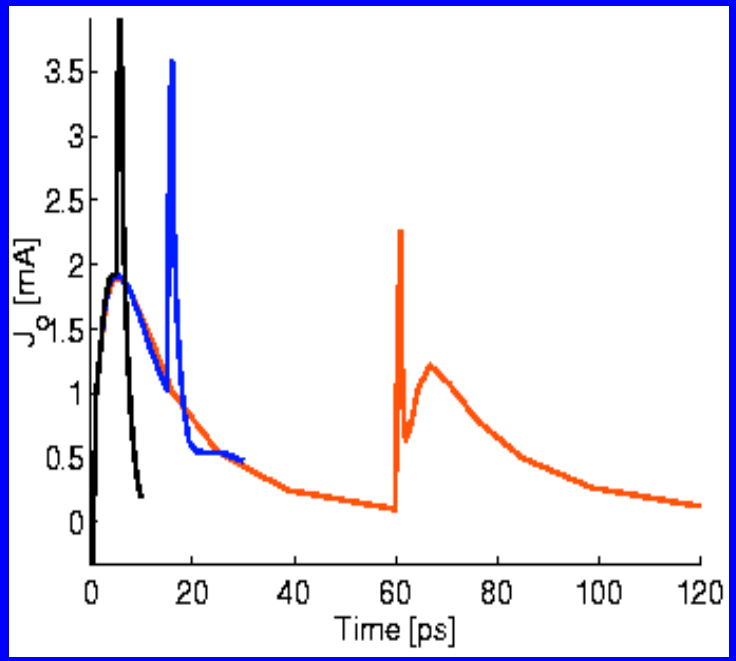
For 0.10μm: t_{ox}=25Å D_{sub}=5x$10^{17}$$cm^{-3}$ VDD=1.0V W=20μm

Response of 0.14μm Physical Gate Length Inverters to Pulses of Different Durations

Induced pulse durations greater than 15psec cause upset

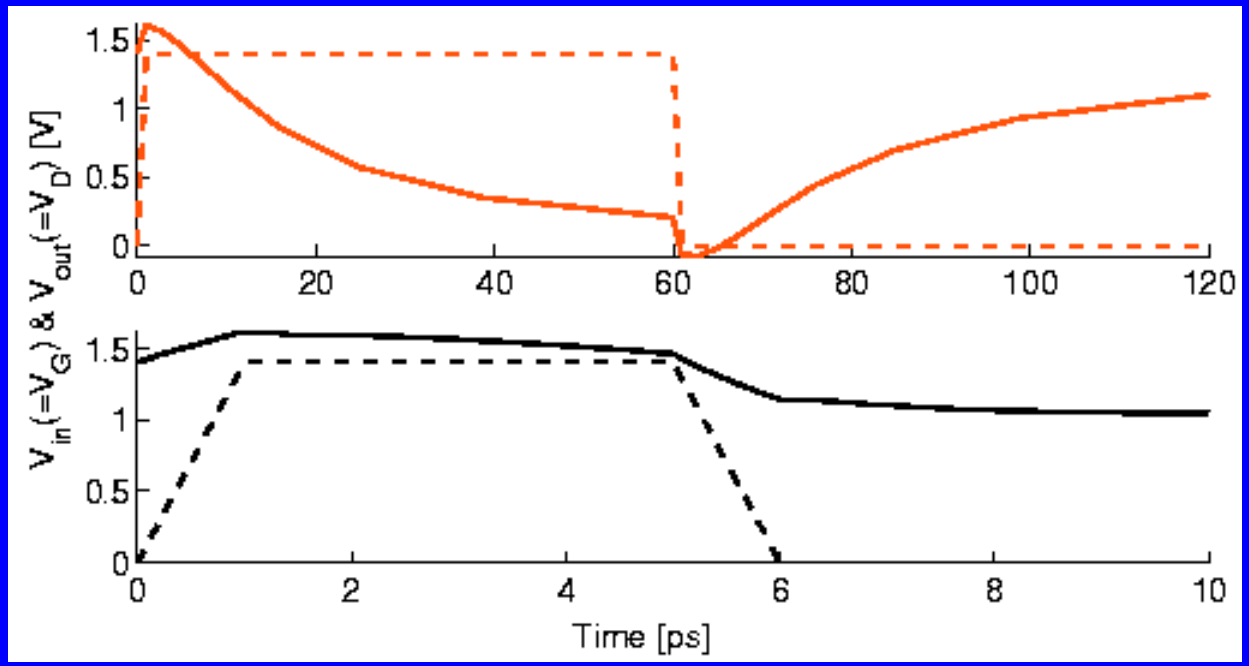


Voltage vs Time

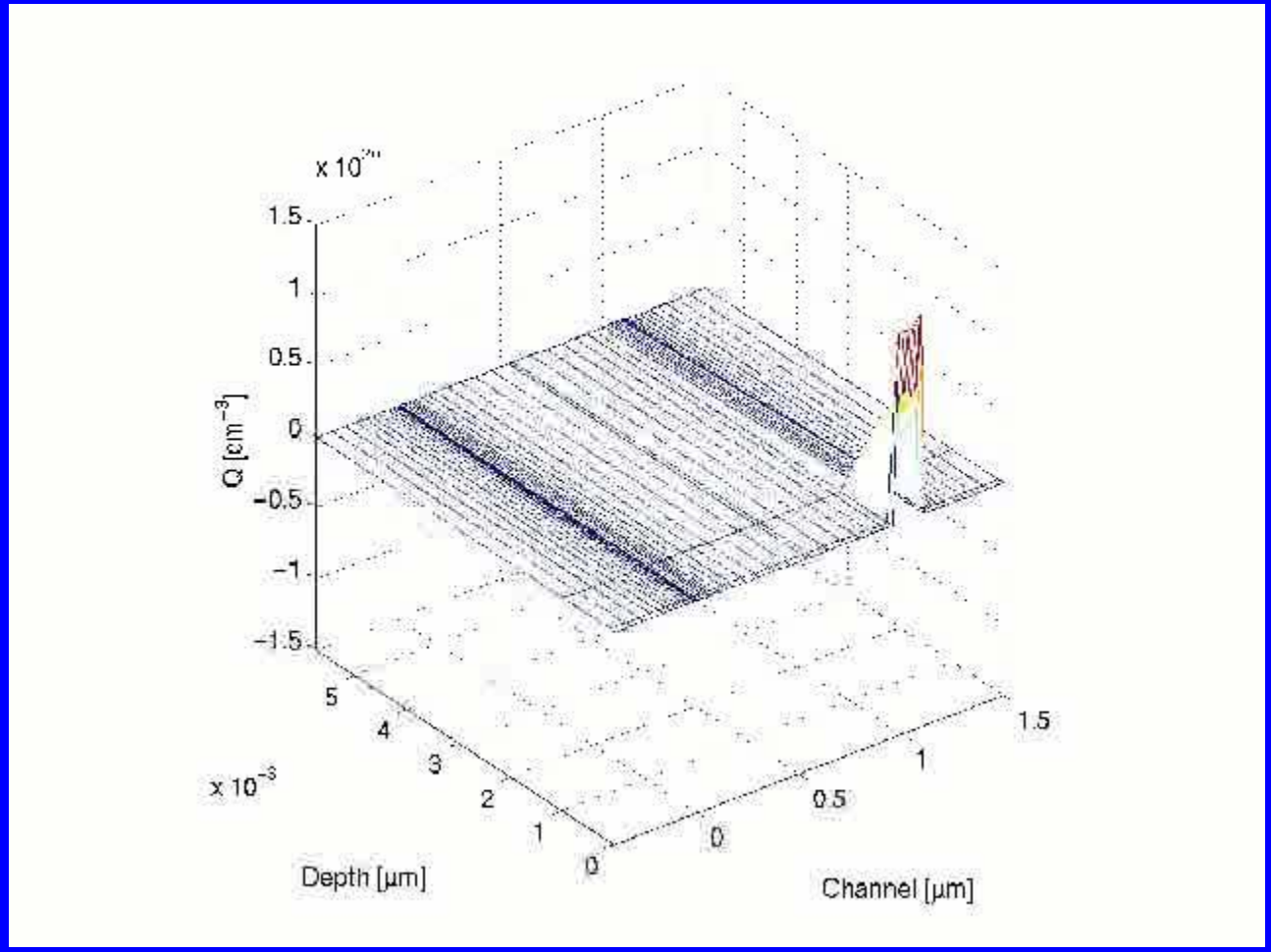


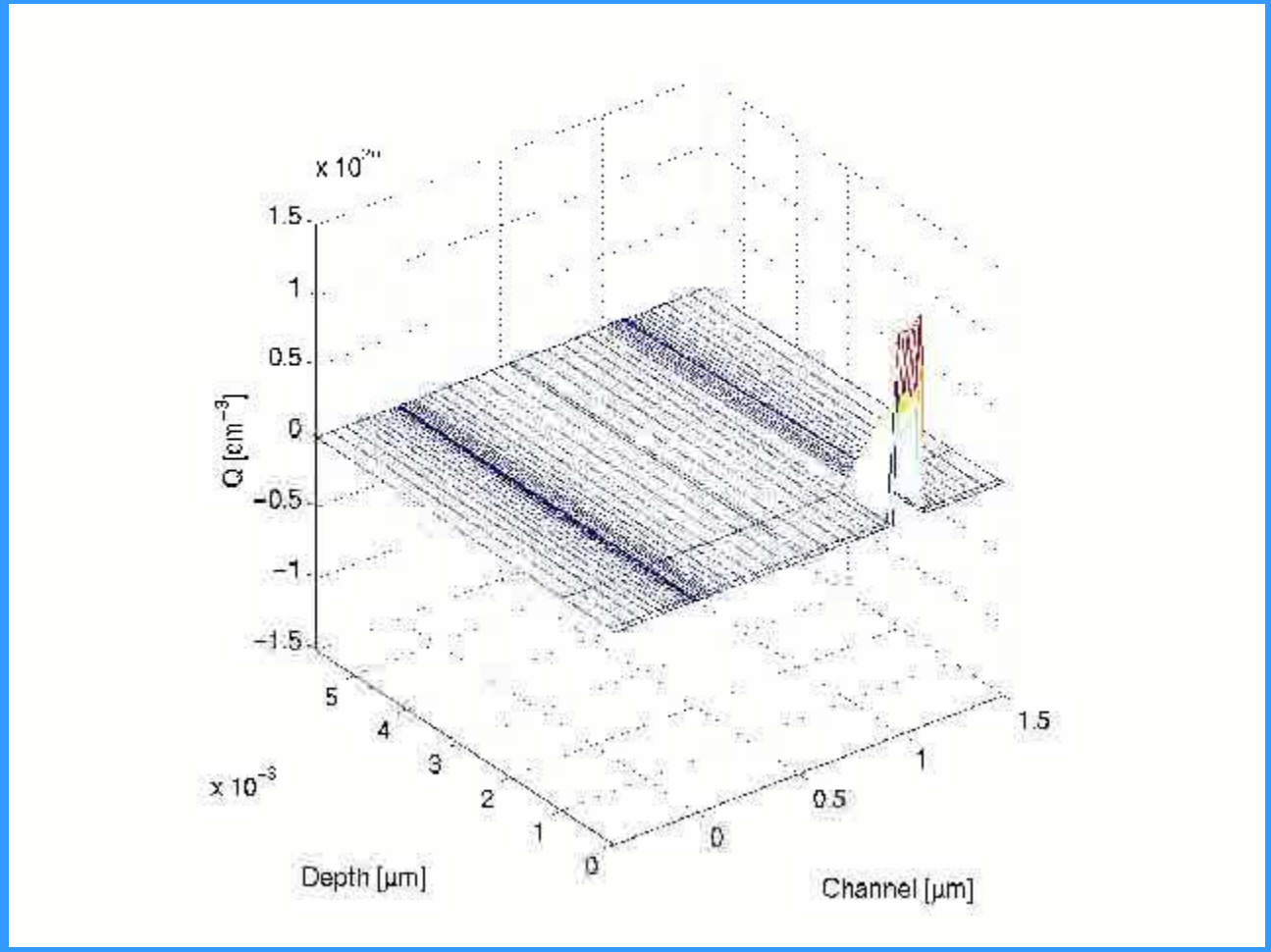
Current vs Time

Following animations shows time-dependent solution of CMOS charge transfers of inverters with following voltage responses



Voltage vs Time

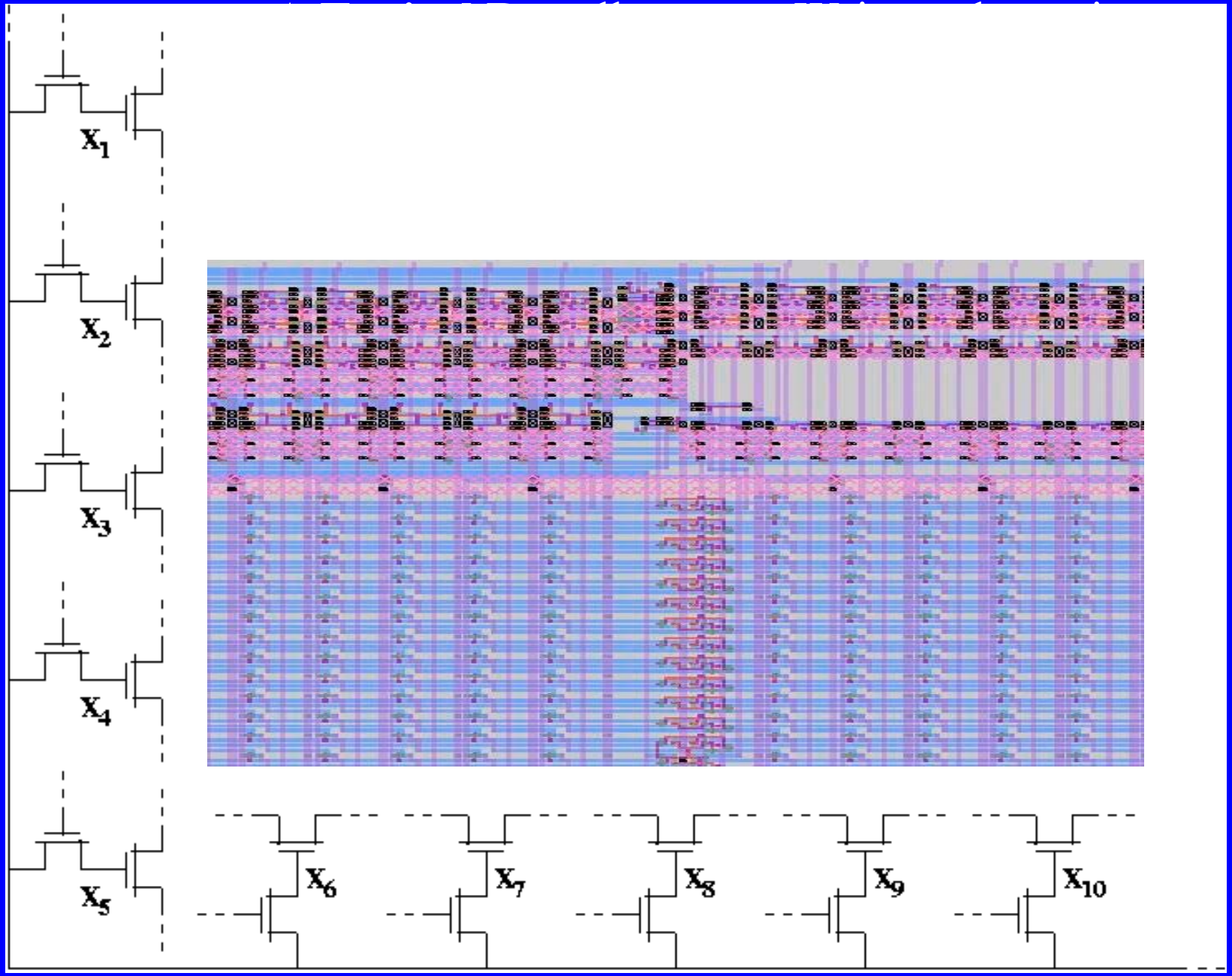

x 10^21
1.5
1
0.5
0
−0.5
−1
−1.5
Q [cm^−3]
5
4
3
2
1
0
x 10^−3
Depth [µm]
0
0.5
1
1.5
Channel [µm]


x 10^21
1.5
1
0.5
0
−0.5
−1
−1.5
Q [cm^-3]
5
4
3
2
1
0
x 10^-3
Depth [µm]
0
0.5
1
1.5
Channel [µm]

Task 2. Interconnects and Passive Elements

Calculation of the Induced Voltage on Passive Elements (Interconnects, Inductors, etc.)

- Stage 1: Static Coupling Approximation
- Stage 2: Incorporate with Device and Circuit Simulators


X1
X2
X3
X4
X5
X6
X7
X8
X9
X10

Interconnect DC Coupling Simulation

We developed a simulation tool to find the induced voltages on the floating metals due to the pins tied up to a fixed voltage source in an arbitrary rectangular geometry.

$$\nabla^2 \Phi = 0$$

$$\frac{\partial^2 \Phi_x}{\partial x^2} + \frac{\partial^2 \Phi_y}{\partial y^2} + \frac{\partial^2 \Phi_z}{\partial z^2} = 0$$

Net Charge is zero inside the metals and the insulator that is filling the region between the metals

$$\int_V \rho_V dV = \int_S \rho_S dS = 0$$

$$\rho_S = \varepsilon_{Ins} E_{Ins} - \varepsilon_{Met} E_{Met} = \varepsilon_{ins} E_{Ins}$$

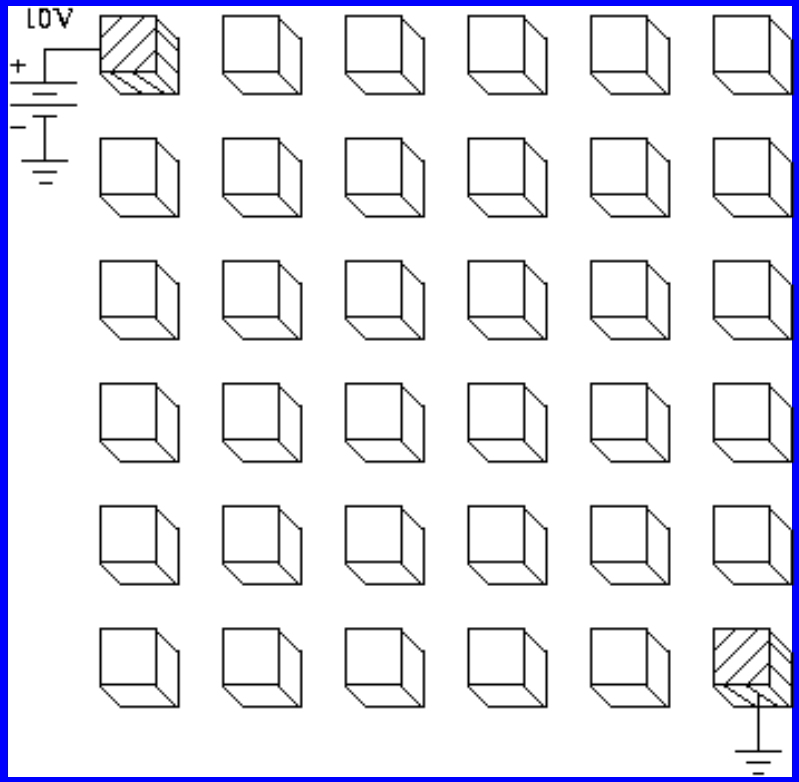
Total charge concentration on the floating metals is zero

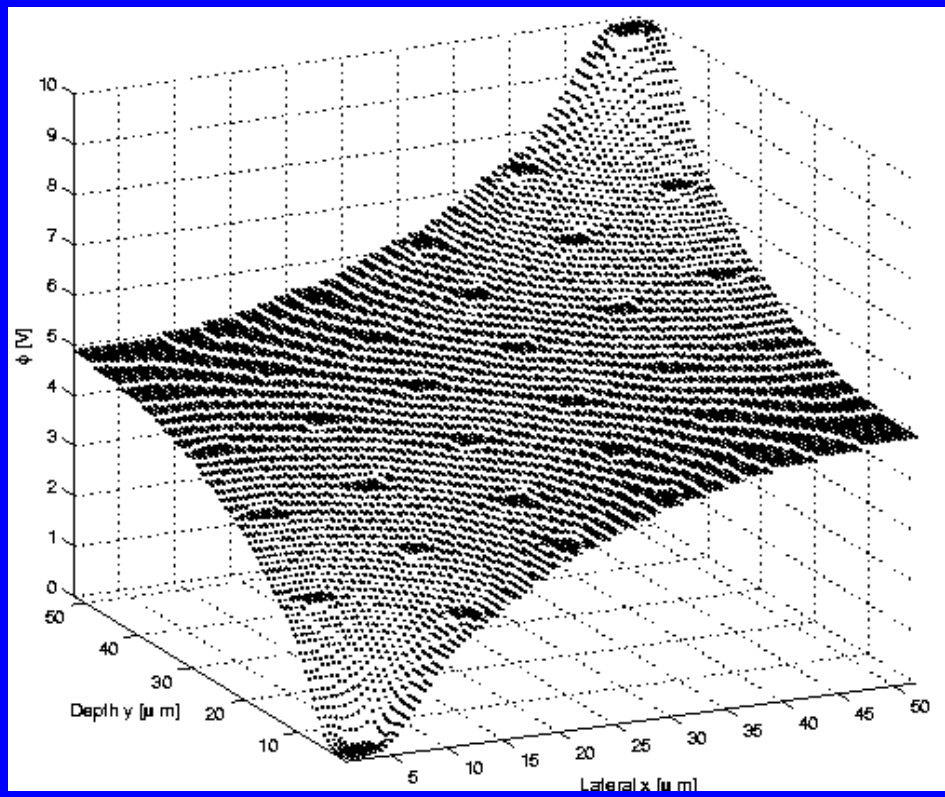
$$\Phi_M = V_{Applied}$$

The potential is constant for the fixed metals

DC Coupling: 2D Simulation Result

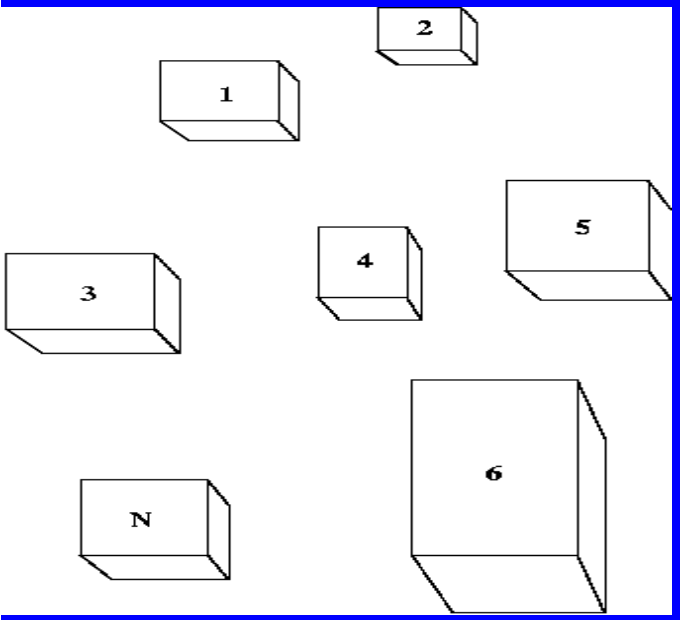
Here, there are 36 metals uniformly distributed on our mesh grid. The voltages on the two metals at the opposite corners are set to 0 and 10V, and the rest is left to float.





Potential Distribution

Capacitances In Multiconductor Systems



$$Q_1 = C_{11}V_1 + C_{12}V_2 + \ldots + C_{1N}V_N$$
$$Q_2 = C_{21}V_1 + C_{22}V_2 + \ldots + C_{2N}V_N$$
$$\vdots$$
$$Q_N = C_{N1}V_1 + C_{N2}V_2 + \ldots + C_{NN}V_N$$

The relation between potential and charge is linear

$$C_{ji} = \left.\frac{Q_i}{V_i}\right|_{V_j=0,\, j\neq i} \Rightarrow C = \begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1N} \\ C_{21} & C_{22} & \cdots & C_{1N} \\ \vdots & & & \vdots \\ C_{N1} & C_{N2} & \cdots & C_{NN} \end{bmatrix}$$

By LU decomposition, we find the voltages on the floating metals, (V_{F1}-V_{FL}), using the C matrix and the voltages of the fixed metals, (V_{M1}-V_{MM}).

$$C_{F_1F_1}V_{F_1} + C_{F_1F_2}V_{F_2} + \ldots + C_{F_1F_L}V_{F_L} = -C_{M_1M_1}V_{M_1} - C_{M_1M_2}V_{M_2} - \ldots - C_{M_1}V_{M_M}$$
$$C_{F_2F_1}V_{F_2} + C_{F_2F_2}V_{F_2} + \ldots + C_{F_2F_L}V_{F_L} = -C_{M_2M_1}V_{M_1} - C_{M_2M_2}V_{M_2} - \ldots - C_{M_2}V_{M_M}$$
$$\vdots$$
$$C_{F_LF_1}V_{F_1} + C_{F_LF_2}V_{F_2} + \ldots + C_{F_LF_L}V_{F_L} = -C_{M_MM_1}V_{M_1} - C_{M_MM_2}V_{M_2} - \ldots - C_{M_M}V_{M_M}$$

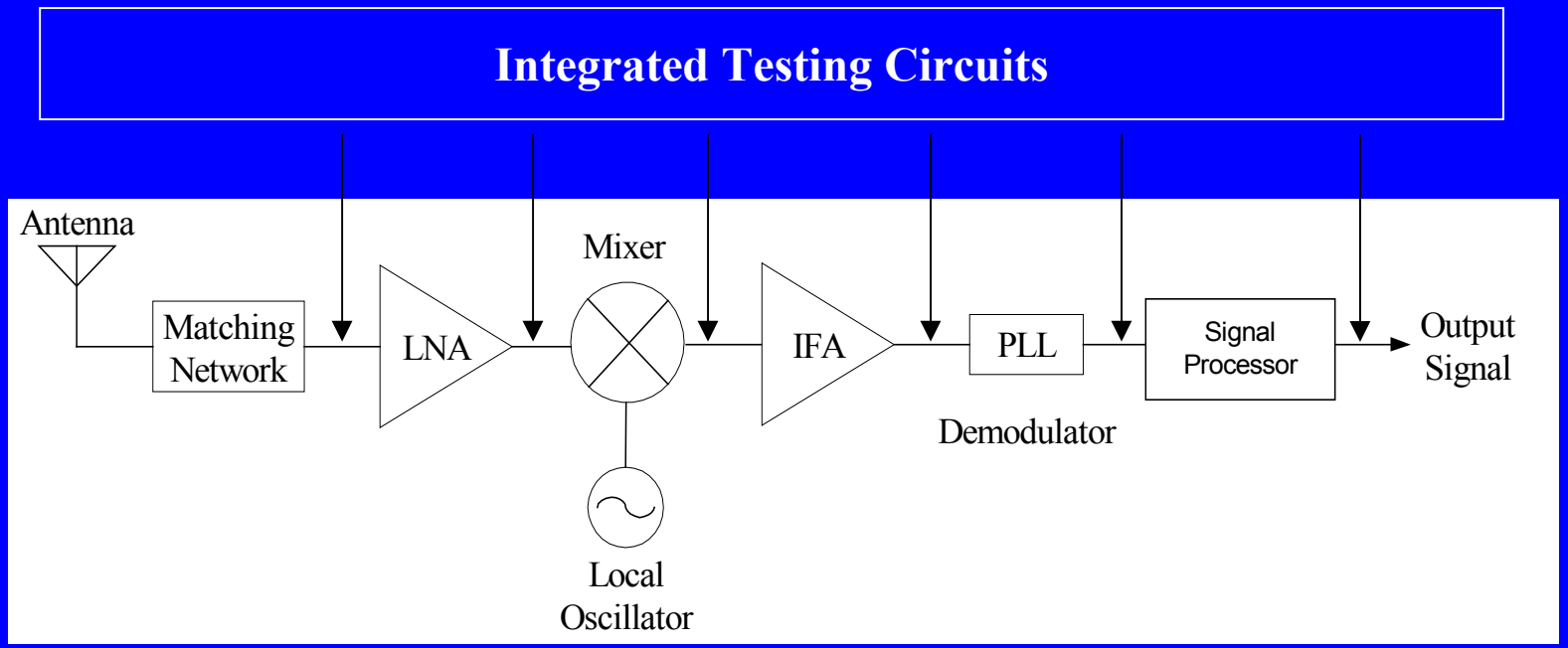
Then, we find the potential distribution by the utilization of the Conjugate Gradient Method.

Task 3. Test Circuit Experiments

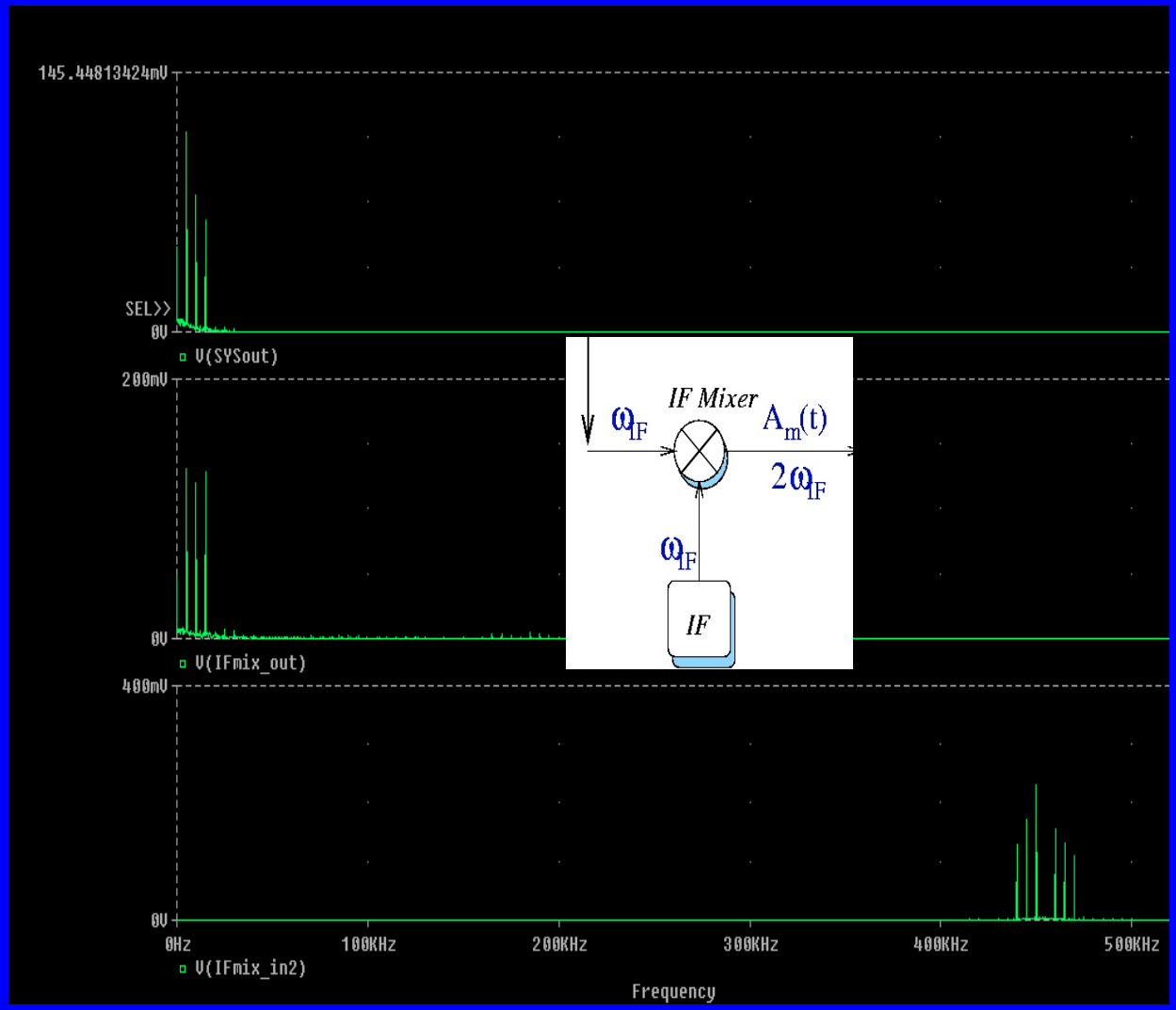
Design and prototype communication-type circuits for experiments on EM coupling.

Receiver

The receiver receives the signal sent out by the transmitter, down-converts it to intermediate frequency, and demodulates the signal to recover the information.



Results, 1: Operation in Frequency Domain, III

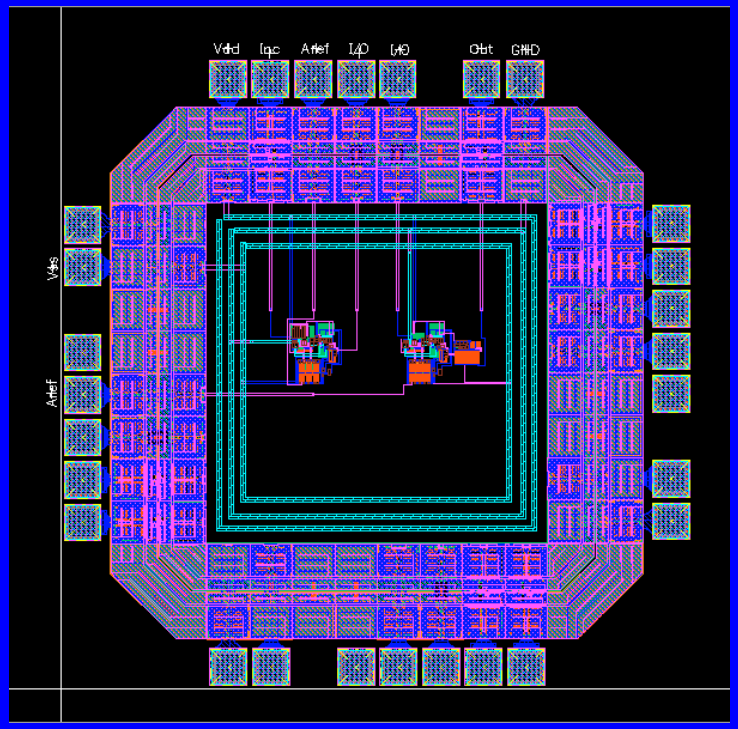


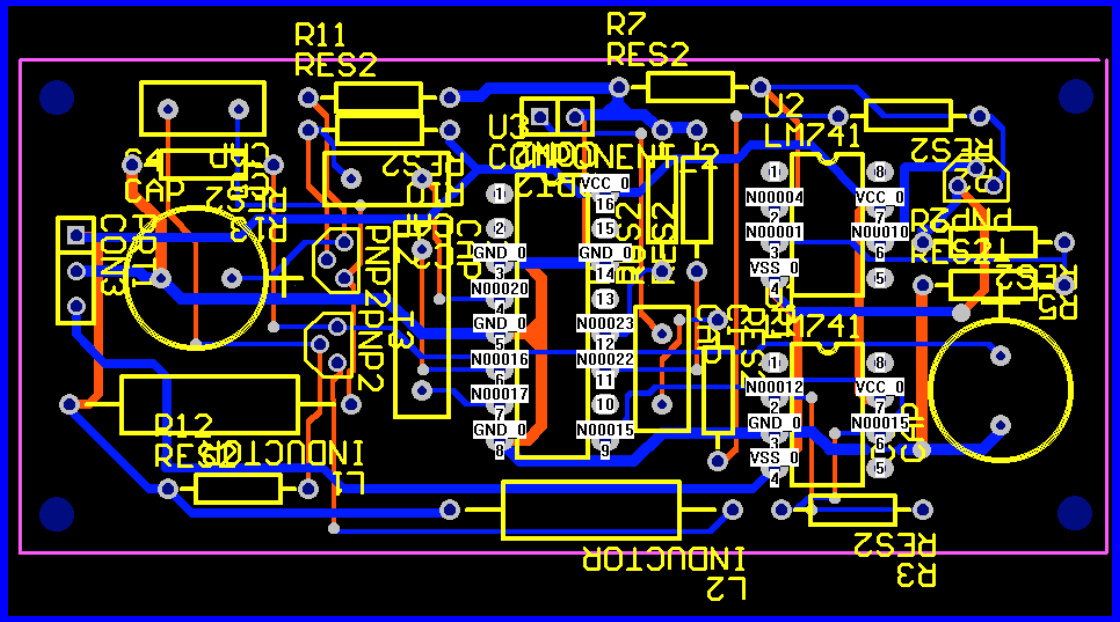
System output

IF mixer output

IF mixer input

Test Circuit Design





Test Receiver Layout on-Chip and on-Board

Summary

- Device simulators have been developed to model effects of EM coupling: Models.
- Models indicate induced voltages of approximately 2X supply voltage can damage nanoscale device.
- Minimum pulse duration to cause upset calculated.
  - 15psec for 0.14μm device
- Methodology developed for modeling interconnect coupling: Next, couple to Device Simulator and SPICE
- Communication test system and circuits being developed with built-in test equipment.