Electromagnetic Effects on Modern Electronic Devices and Circuits: Modeling and Experiments

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Outline

EM Coupling: Levels Investigated

• Device Level (Modeling)
• Interconnects and Passive Elements (Modeling)
• Circuit Prototyping and Testing for EM Coupling (Experiment)

CMOS INVERTER
EM Related Problems in Integrated Circuits
Example Chip
Task 1: Numerical Modeling & Analysis of EM Effects on Nanoscale Devices

Issues:

- Chips can contain millions of nanoscale transistors (MOSFETs)
- MOSFETs are very fragile, with gate lengths of 0.2µm and below, and oxide thickness of 35Å.
- EM pulses can couple to device terminals and alter voltage levels
- Such terminal voltage changes can radically alter I-V characteristics and if large enough, can destroy device though oxide breakdown and/or filament formation related to excessive avalanching.

Use Numerical Modeling of Nanoscale Devices to help understanding and to predict consequences of EM coupling to terminals, and to present design alternatives for safeguarding against coupling effects.
Modeling: Use Detailed Device Modeling to Quantify Transistor Failures (MOSFETs)

MOSFET Cross-Section
Gate Length: 0.14\,\mu m
Oxide Thickness 35\,\AA

Doping Profile
Solve Transient Semiconductor Device Eqns. Numerically in 2D

**DD Equations**

\[
\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}} (p - n + D)
\]

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla . \overrightarrow{J_n} - R_n + G_n
\]

\[
\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla . \overrightarrow{J_p} - R_p + G_p
\]

**Supplementary DD Equations**

\[
\overrightarrow{J_n} = -q\mu_n n \overrightarrow{\nabla \Phi} + q\mu_n V_T \overrightarrow{n}
\]

\[
\overrightarrow{J_p} = -q\mu_p p \overrightarrow{\nabla \Phi} - q\mu_p V_T \overrightarrow{p}
\]

Coupled Discretized DD Equations are solved at each mesh point

Results give I-V and Potential, Charge Concentrations, Current Densities inside device.
Resulting Electrostatic Potential inside 0.14µm MOSFET:  
Bias Conditions for Oxide Breakdown

\[ V_G = 2.8\text{V} \quad V_D = 1.4\text{V} \quad V_S = V_B = 0\text{V} \]

If \( |E_y| > 7\text{MV/cm} \) \( \Rightarrow \) Oxide Breakdown

Device Simulations predicts induced gate voltage of 2X supply causes MOSFET oxide damage
Distributed Circuit Simulations (Inverter)

**DD Equations**

\[
\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}} (p - n + D)
\]

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n - R_n + G_n
\]

\[
\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \vec{J}_p - R_p + G_p
\]

**Supplementary DD Equations**

\[
\vec{J}_n = -q\mu_n n \nabla \Phi + q\mu_n V_T \nabla n
\]

\[
\vec{J}_p = -q\mu_p p \nabla \Phi - q\mu_p V_T \nabla p
\]

**Coupled Discretized DD Equations**

Lumped KCL equation check at the output node and using the KCL equation, the output guess is updated for the next iteration, \(V_{o}^{i+1}\):

\[
I_{DN} - I_{DP} + I_{R_L} + I_{C_L} = 0
\]

\[
A_n B_n V_{o}^{i+1} + A_p B_p V_{o}^{i+1} + \frac{V_{o}^{i+1} - V_{SS}}{R_L} + C_L \frac{V_{o}^{i+1} - V_{o}^{i}}{\Delta t} = 0
\]

\[
V_{SS} + V_{o}^{i} \frac{R_C L}{\Delta t} (A_n + A_p) R_L
\]

\[
V_{o}^{i+1} = \frac{R_C L}{\Delta t} (A_n + A_p) R_L
\]

\[
1 + \frac{R_C L}{\Delta t} + (B_n + B_p) R_L
\]
Inverters with Different Gate Lengths: Simulated Response to 60psec Pulse Input

Devices scaled according to design rules.
For 0.10µm: \( t_{ox} = 25\text{Å} \ D_{sub} = 5 \times 10^{17}\text{cm}^{-3} \ VDD = 1.0\text{V} \ W = 20\mu\text{m} \)
Response of 0.14µm Physical Gate Length Inverters to Pulses of Different Durations

Induced pulse durations greater than 15psec cause upset.

Voltage vs Time

Current vs Time
Following animations shows time-dependent solution of CMOS charge transfers of inverters with following voltage responses

Voltage vs Time
Task 2. Interconnects and Passive Elements

Calculation of the Induced Voltage on Passive Elements (Interconnects, Inductors, etc.)

- Stage 1: Static Coupling Approximation
- Stage 2: Incorporate with Device and Circuit Simulators
A Typical Bus allows one write and certain number of reads through a single line while the remaining connections are kept in high impedance or floating states.
Interconnect DC Coupling Simulation

We developed a simulation tool to find the induced voltages on the floating metals due to the pins tied up to a fixed voltage source in an arbitrary rectangular geometry.

\[ \nabla^2 \Phi = 0 \]

\[ \frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} + \frac{\partial^2 \Phi}{\partial z^2} = 0 \]

Net Charge is zero inside the metals and the insulator that is filling the region between the metals.

\[ \int_V \rho_v dV = \int_S \rho_s dS = 0 \]

\[ \rho_s = \epsilon_{\text{Ins}} E_{\text{Ins}} - \epsilon_{\text{Met}} E_{\text{Met}} = \epsilon_{\text{ins}} E_{\text{Ins}} \]

Total charge concentration on the floating metals is zero.

The potential is constant for the fixed metals.

\[ \Phi_M = V_{\text{Applied}} \]
Here, there are 36 metals uniformly distributed on our mesh grid. The voltages on the two metals at the opposite corners are set to 0 and 10V, and the rest is left to float.
The relation between potential and charge is linear

\[ Q_i = C_{1i}V_1 + C_{12}V_2 + ... + C_{1N}V_N \]
\[ Q_2 = C_{21}V_1 + C_{22}V_2 + ... + C_{2N}V_N \]
\[ \vdots \]
\[ Q_N = C_{N1}V_1 + C_{N2}V_2 + ... + C_{NN}V_N \]

By LU decomposition, we find the voltages on the floating metals, \((V_{F1}-V_{FL})\), using the \(C\) matrix and the voltages of the fixed metals, \((V_{M1}-V_{MM})\).

\[
C_{ji} = \frac{Q_i}{V_i} \bigg|_{V_j=0, j \neq i} \Rightarrow C = \begin{bmatrix}
C_{11} & C_{12} & \cdots & C_{1N} \\
C_{21} & C_{22} & \cdots & C_{1N} \\
\vdots & \vdots & \ddots & \vdots \\
C_{N1} & C_{N2} & \cdots & C_{NN}
\end{bmatrix}
\]

Then, we find the potential distribution by the utilization of the Conjugate Gradient Method.
Task 3. Test Circuit Experiments

Design and prototype communication-type circuits for experiments on EM coupling.
The receiver receives the signal sent out by the transmitter, down-converts it to intermediate frequency, and demodulates the signal to recover the information.
Results, 1: Operation in Frequency Domain, III

System output

IF mixer output

IF mixer input
Test Circuit Design

Test Receiver Layout on-Chip and on-Board
Summary

- Device simulators have been developed to model effects of EM coupling: Models.
- Models indicate induced voltages of approximately 2X supply voltage can damage nanoscale device.
- Minimum pulse duration to cause upset calculated.
  - 15psec for 0.14μm device
- Methodology developed for modeling interconnect coupling: Next, couple to Device Simulator and SPICE
- Communication test system and circuits being developed with built-in test equipment.