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RELIABLE  
COMPUTER  
ARCHITECTURES

MURI Review  
June 8, 2002

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Bruce Jacob

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University of  
Maryland

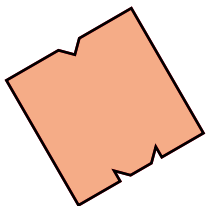
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# **EFFECTS OF MICROWAVES**

## **Robust Computer Architectures**

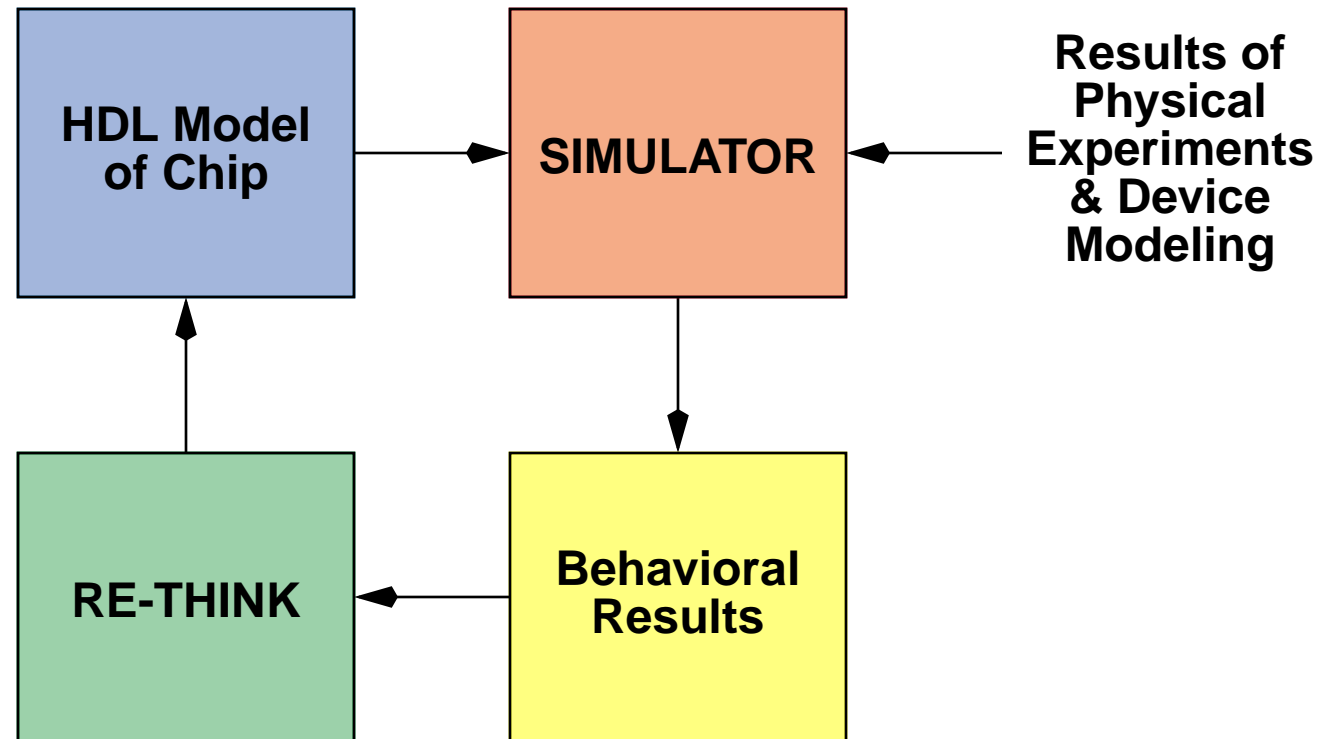
**Prof. Bruce Jacob**

**Electrical & Computer Engineering**  
**University of Maryland, College Park**



UNIVERSITY OF MARYLAND

# System Modeling



***WHEN systems fail, HOW do they fail?***

**We use this information  
to develop & test reliable architectures**

# Tasks (Talk Outline)

## ACCOMPLISHED

- Verilog models of two bootable microprocessors (simple/advanced)
- Initial work on robust architectures (reliability studies, draft floorplan)

## IN PROGRESS

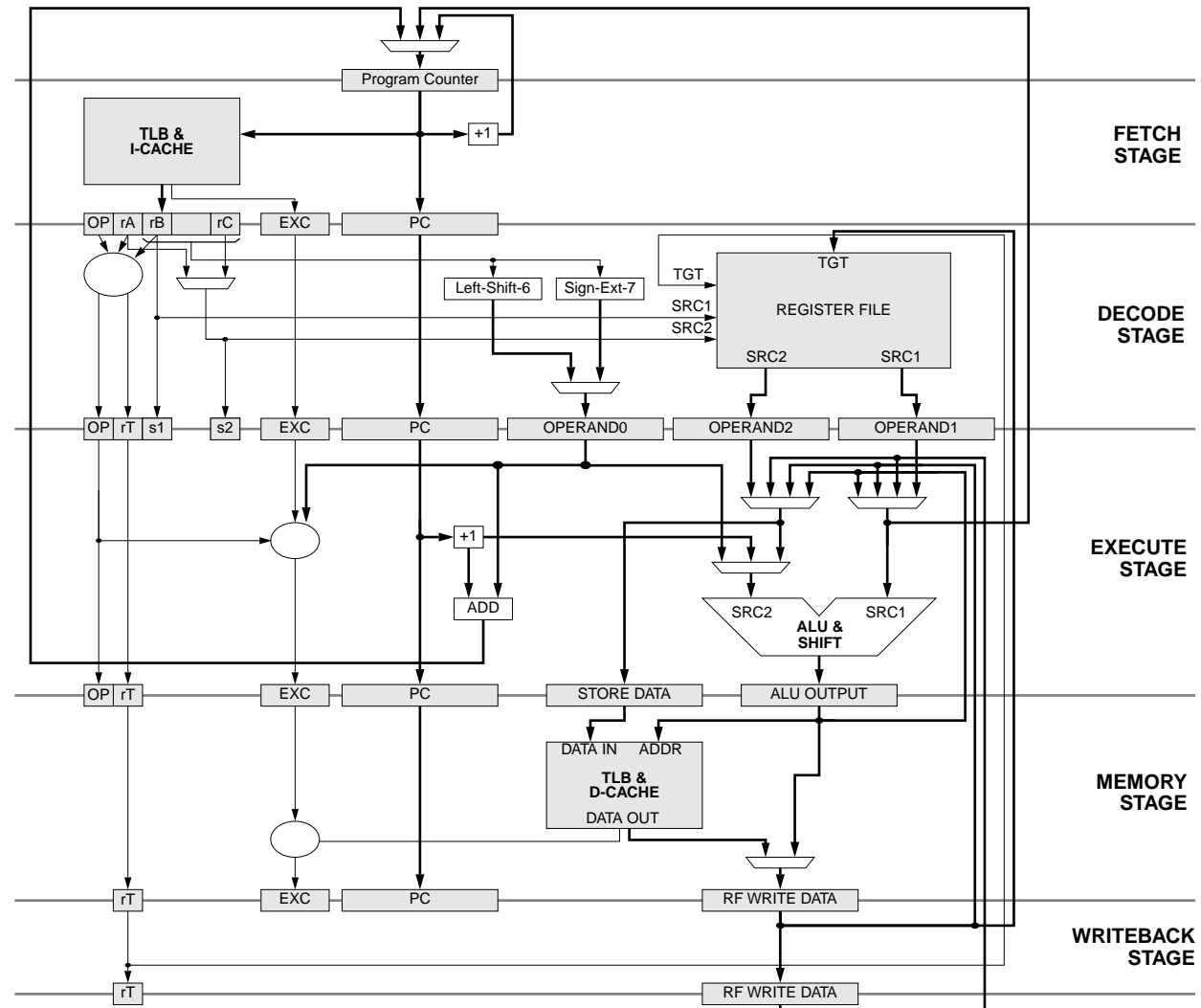
- Verilog model of microprocessor with hardware checkpoint/repair

## FUTURE WORK

- Fabricate and test physical designs
- Enhanced Verilog and SPICE software

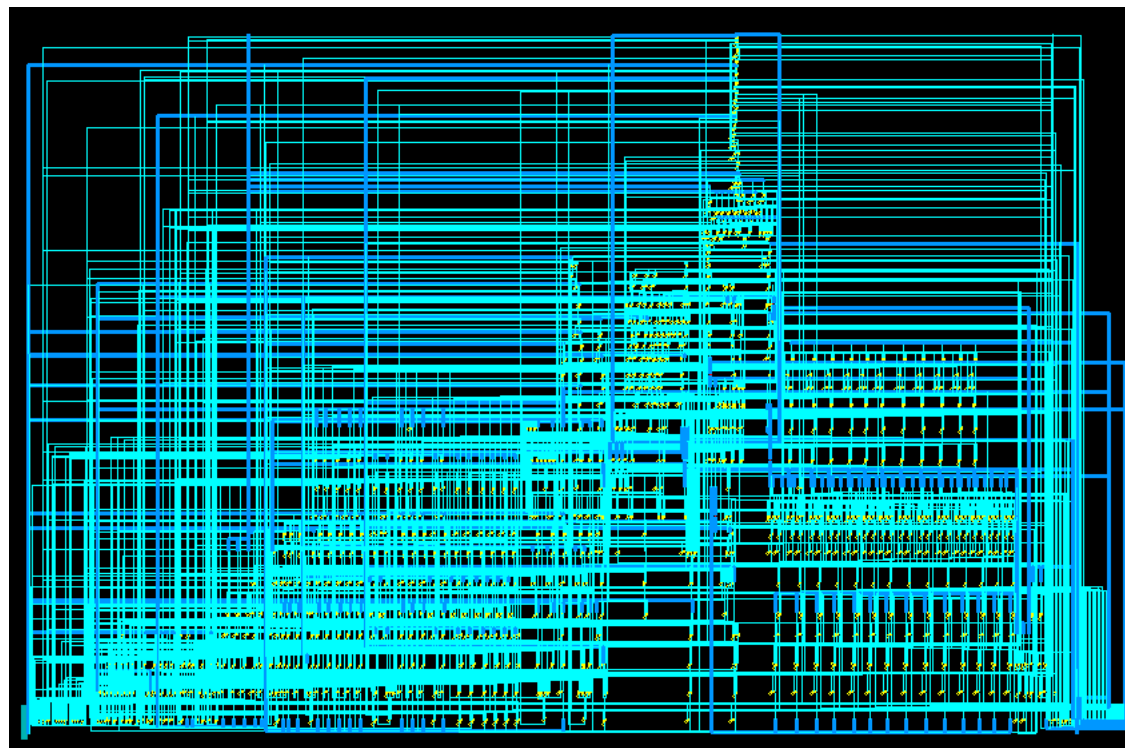
# Processor Model: simple

## Single-Issue, In-Order, Five-Stage Pipeline



# Processor Model: simple

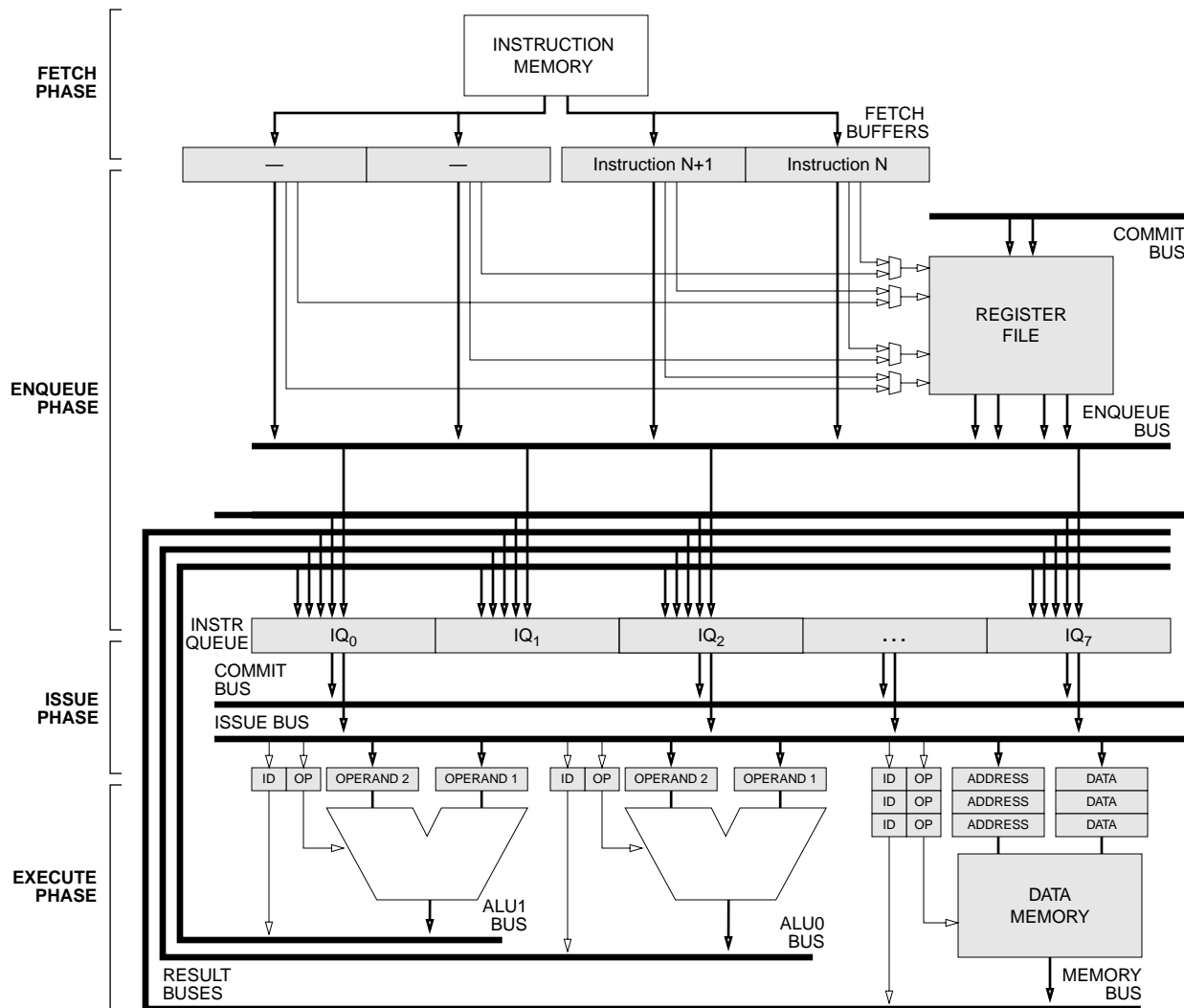
## Single-Issue, In-Order, Five-Stage Pipeline



**16-bit processor core**  
**Handles interrupts precisely**

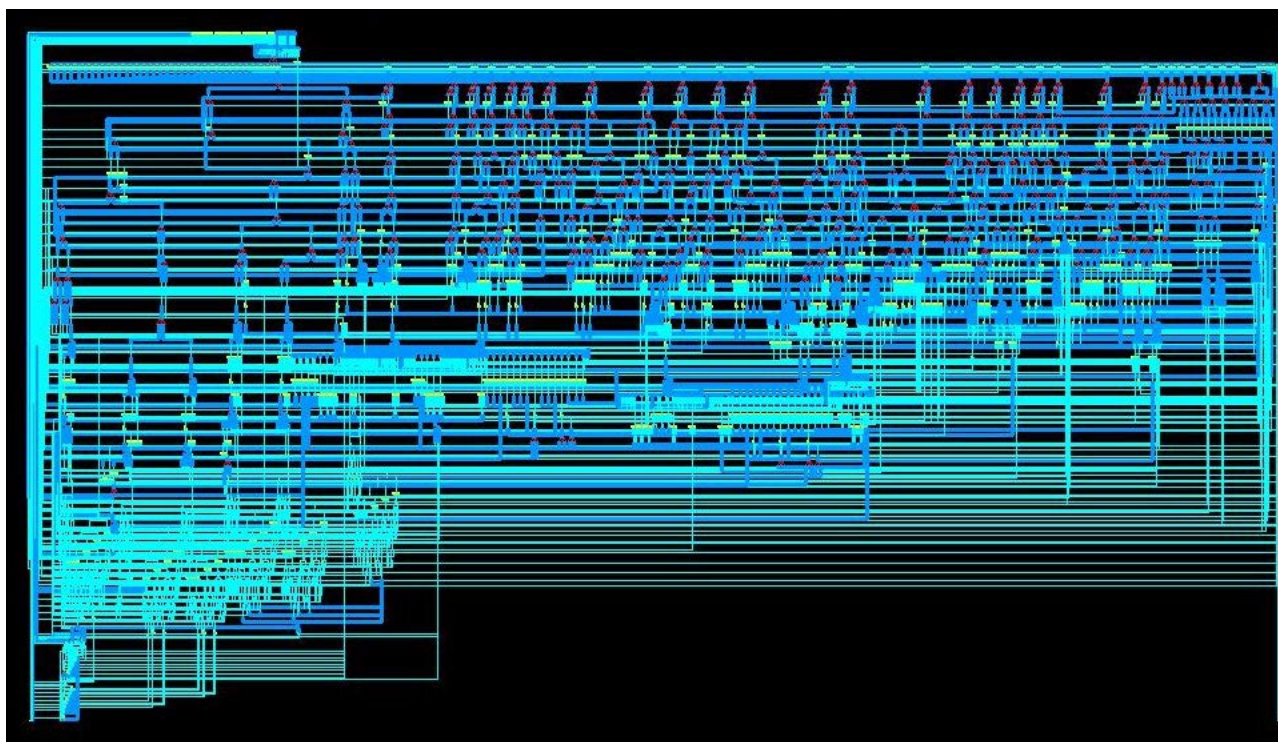
# Processor Model: advanced

## High-Performance Out-of-Order Core



# Processor Model: advanced

## PowerPC ISA with AltiVec SIMD Unit

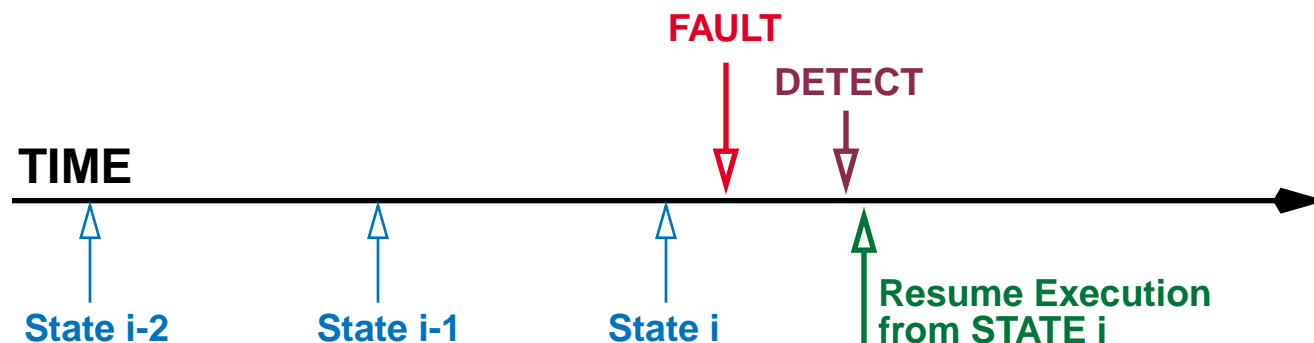


**Design & layout of core in progress  
(AltiVec multiplier above)**

# Robust Architectures

## INITIAL STUDY: Assume the Worst Case

### Checkpoint/Repair ...



### CHECKPOINT:

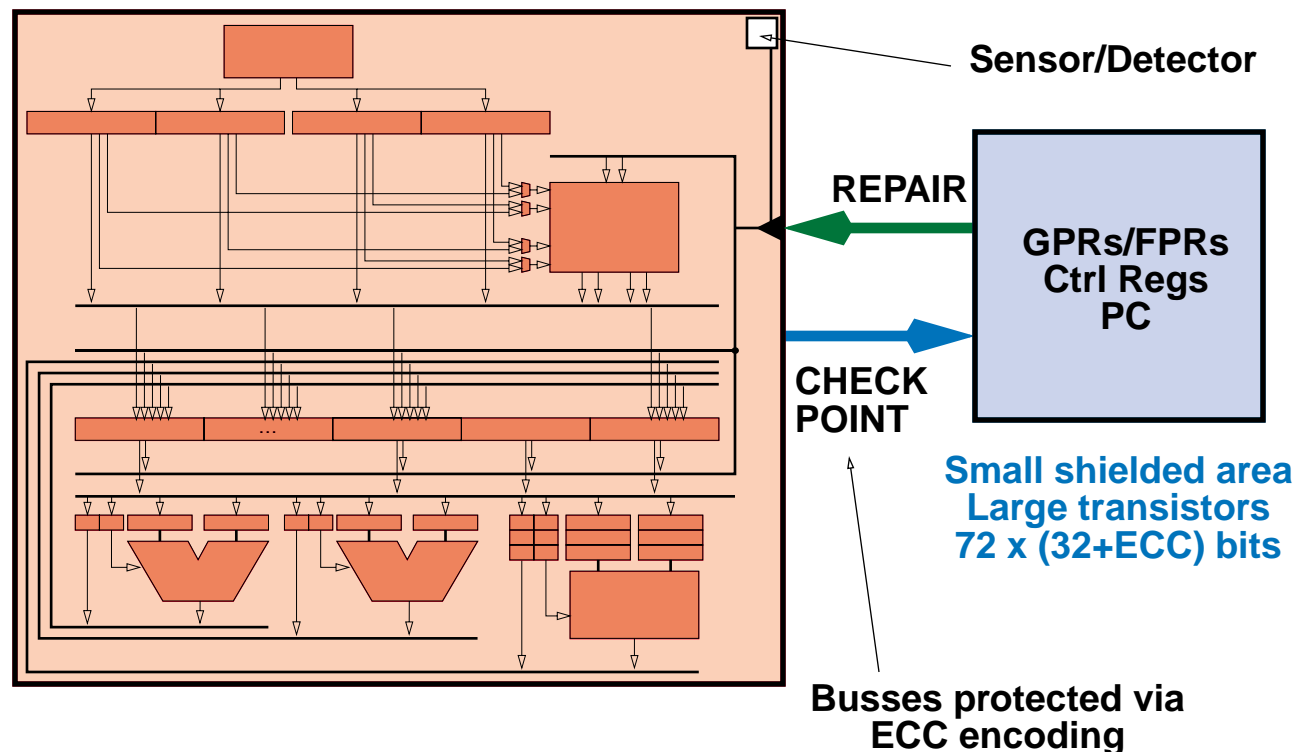
Periodically save **KNOWN-GOOD STATE**

In case of **FAULT**, **REPAIR** to last saved state



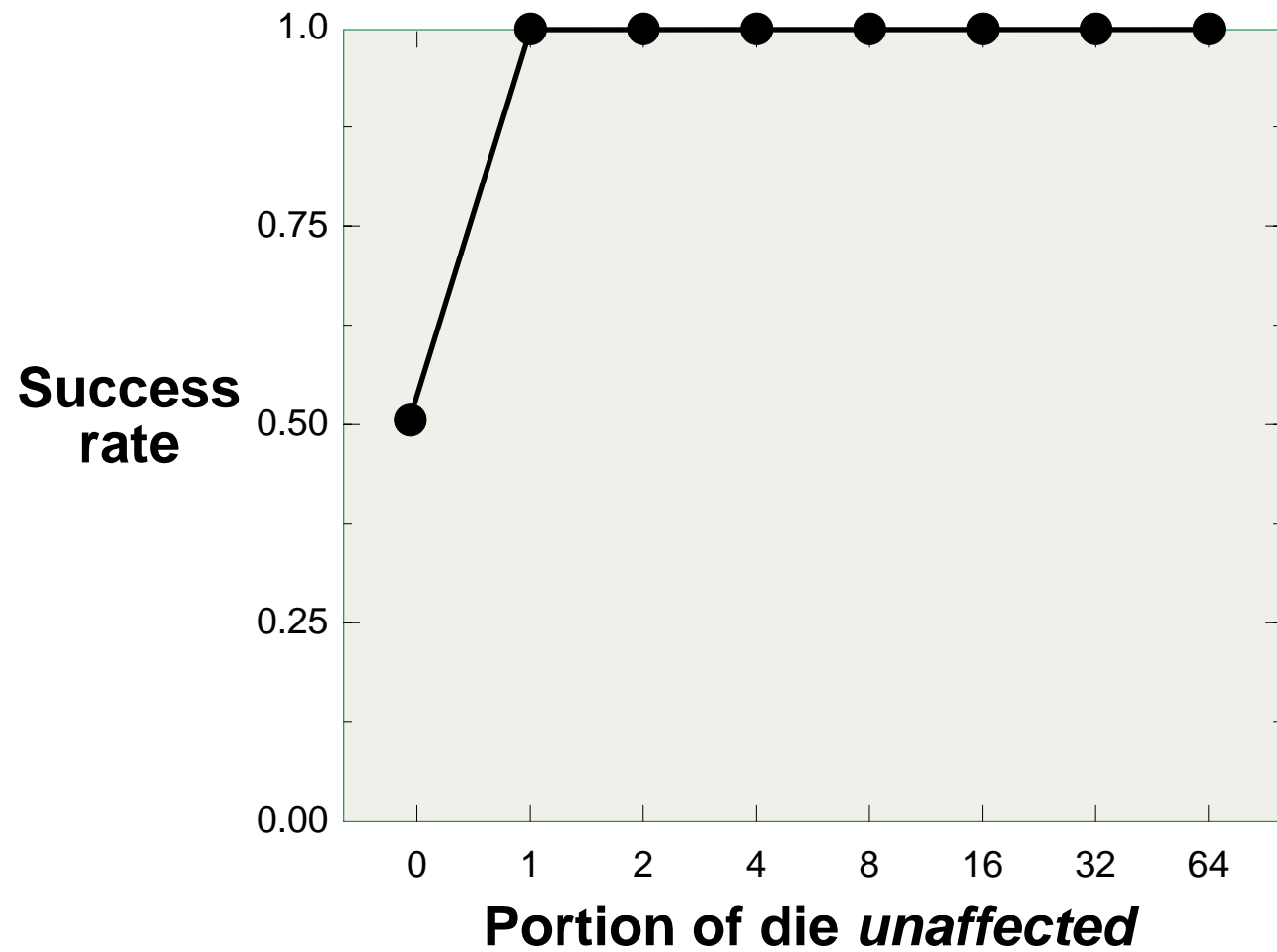
# Robust Architectures

## INITIAL STUDY: Assume the Worst Case

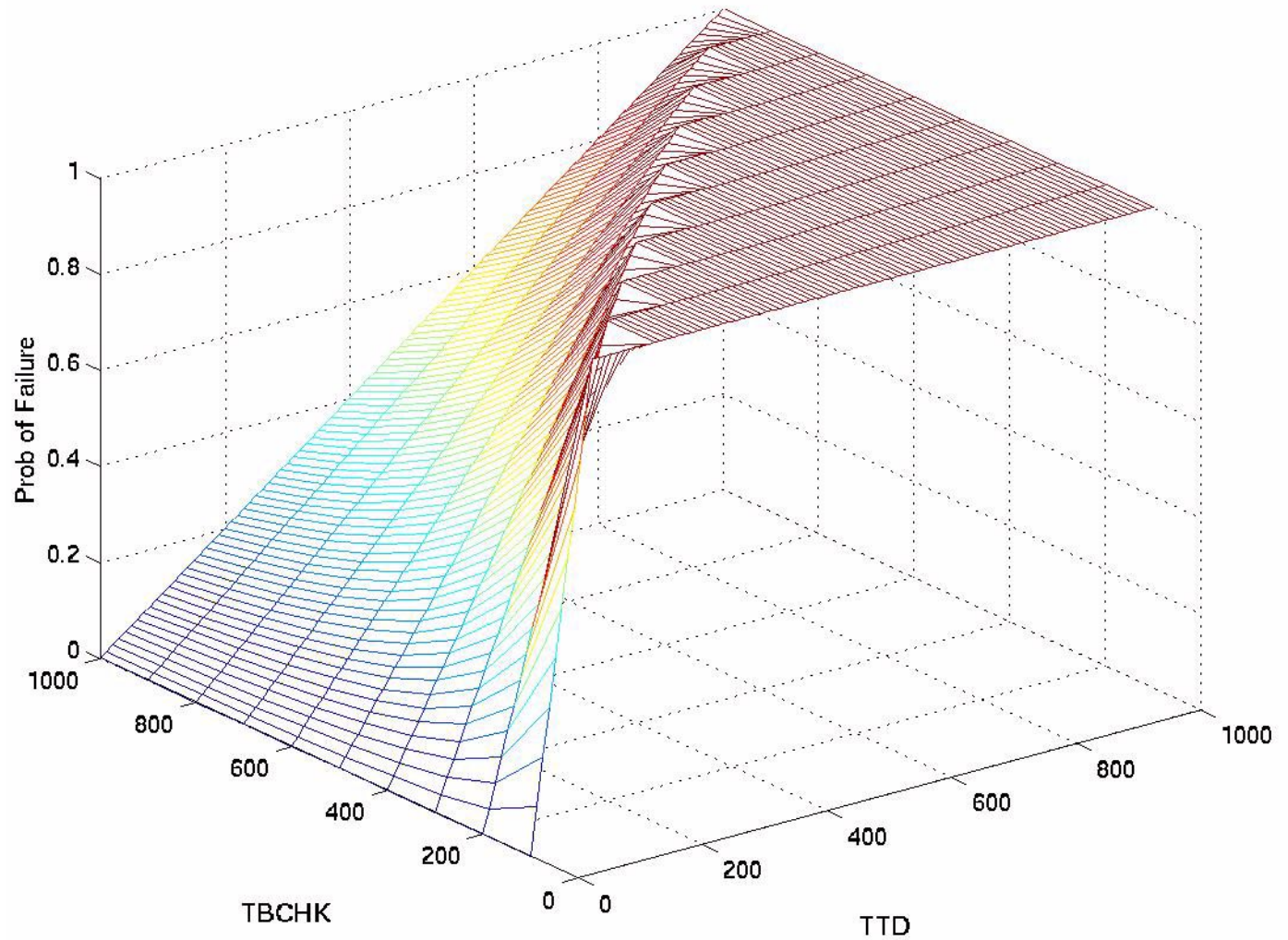


Implementation can be single- or multi-chip

# Robust Architectures

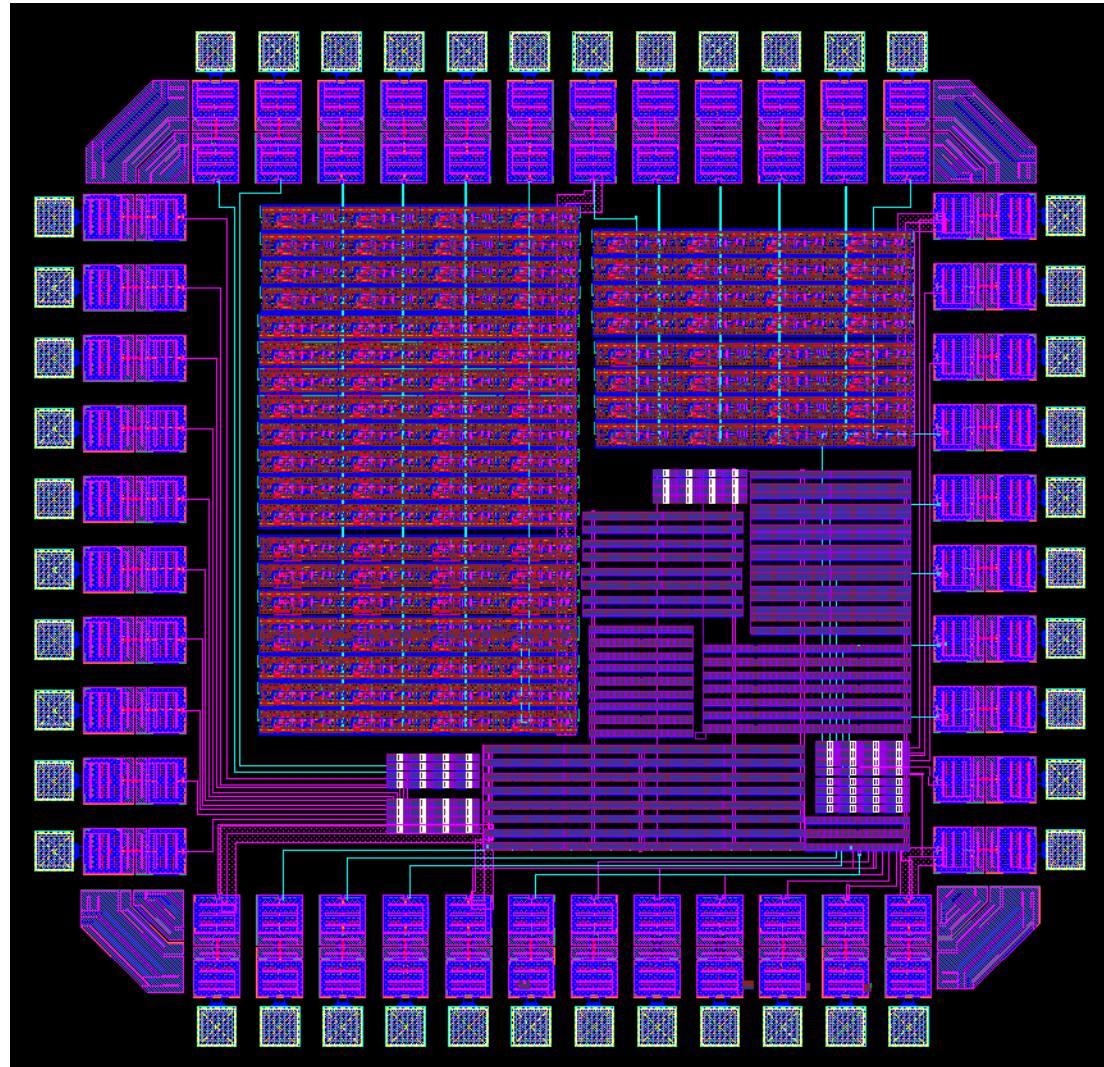


# Robust Architectures



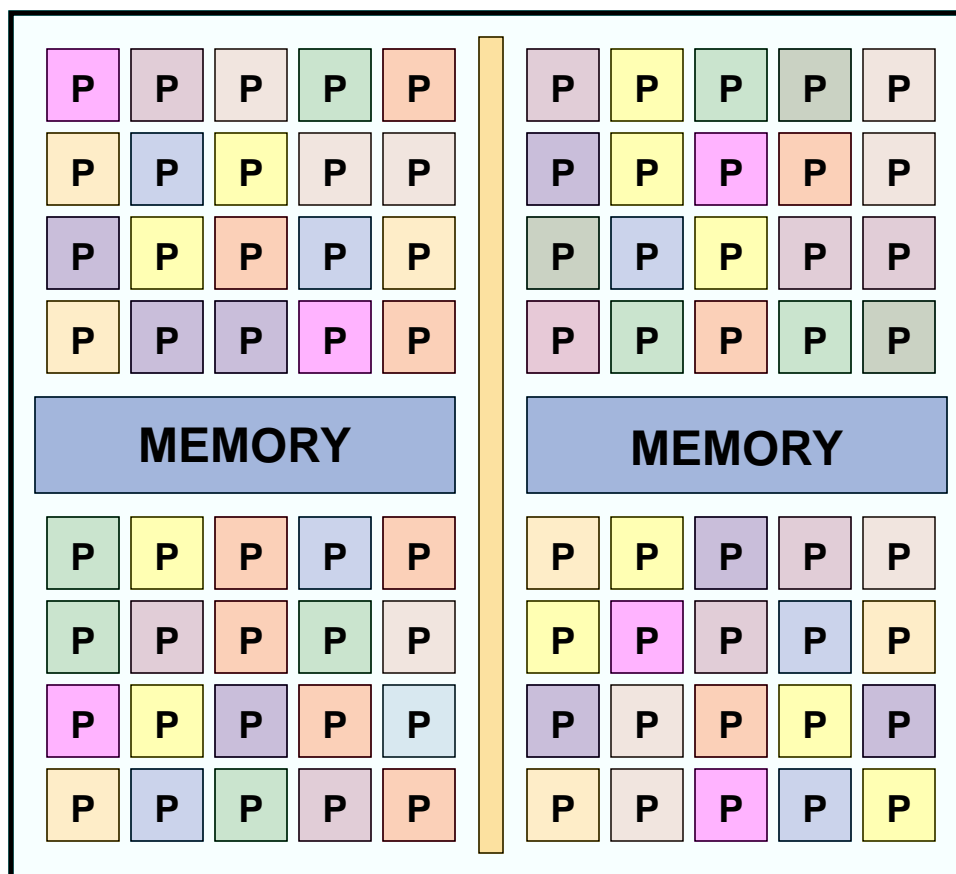
# Robust Architectures

## Initial Floorplan (simple CPU + safestore)



# Globally Asynchronous

**ASSUMPTION: Clock Net is Weak Point**



**Processing elements generate local clocks  
Synchronize at inter-node communication**

# Future Work

## Synthesize, Fabricate, Test Canonical Forms

- **Clock trees**
- **Busses (w/ and w/o ECC)**
- **Memories (w/ and w/o ECC)**
- **Arithmetic/Logic Units**

**Incorporate Drift-Diffusion into CAD tools  
(more accurate SPICE/Verilog modeling)**

# Participants

Profs. **Bruce Jacob & Neil Goldsman, UMCP**

A host of grad students:

- Azadeh Davoodi, Cagdas Dirik,  
Amol Gole, Samuel Rodriguez,  
Ohm Tuaycharoen (**Architecture**)
- Akin Akturk, Zeynep Dilli,  
Tejas Chitnis (**Microelectronics**)

