Experimental Studies of RF Interference and Upset in Devices and Gates

Agis A. Iliadis
Electrical and Computer Eng. Dept.,
University of Maryland,
College Park, MD 20742
agis@eng.umd.edu

Students: N. Narayanan
Xingzhi Wen

Goals

- Start with the study of the effects on the fundamental units of IC circuits, ie individual devices (MOSFETs) and gates (CMOS Inverters),.
- Identify most prominent vulnerabilities of the units for interference, upset, and damage, and examine how they critically affect circuit operation.
- Establish the failure mechanisms for each regime and develop hardened IC device/circuit designs.
- Evaluate response of device with RF pulse parameters and use well characterized devices as on-chip sensing and protecting elements.
- Develop on-chip sensing, registration, and protection circuitry.

Effects on Devices and Gates

- Metal I/O pins and slits on sealed (packaged) IC's, and actual antennae in communication modules, can become effective inputs (antennae) for the RF to couple into the chip and disrupt operation.
- Thus RFI coupled through these ports of entry will affect the operating point, the gain, input and output impedances of the device, and the stability, response and transfer characteristic of gates, thus affecting circuit performance in unpredictable ways.
- They may cause bits to flip in digital systems, and temporary or permanent malfunction of systems with damage on p-n junctions, gate dielectrics and/or metallizations.
- Due to the complexity theoretical and experimental evaluation necessary

Methodology

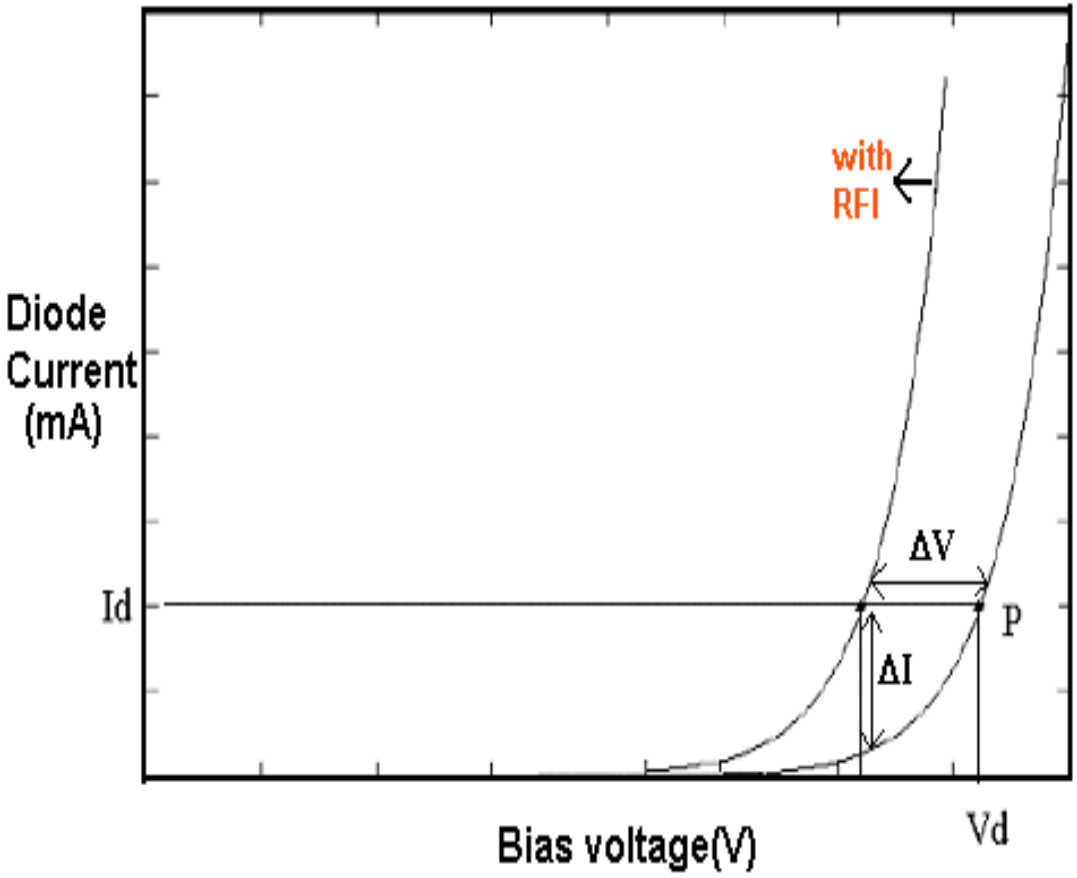
- Unpackaged chips with arrays of individual devices and gates will be tested by controlled RF pulses injected directly into the inputs and outputs.
- The effects on operational parameters will be measured and evaluated at DC operation, small and large signal operation, and high frequency operation (f_T and f_{max}).
- Effects on junction temperature, non-linear interactions at break-down, “hot” electron, gate oxide, interface and metallization degradation, will be studied using electrical, AFM, TEM, SIMS, and XPS analysis.
- Effective protection and RF hardened design will be developed

RFI Effect on Diode I-V Characteristics

- I-V curve shifts upwards
- Equations:

$$\Delta V = -\frac{V_m^2}{4V_T} \qquad \Delta I = \frac{V_m^2}{4}\frac{I_d + I_s}{V_T^2}$$

- Vm is the RFI amplitude & Is is the reverse saturation current of the diode

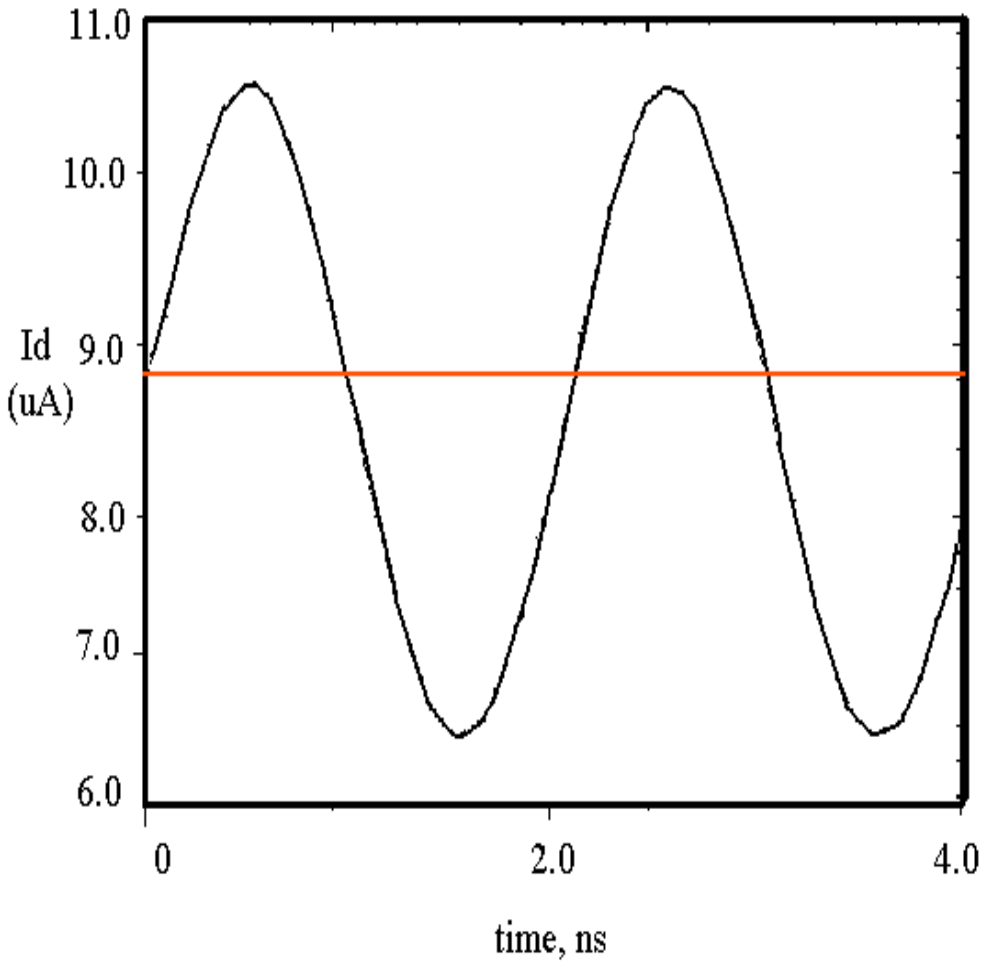


RF Effects on MOSFETS

- RF can couple to all four (gate, source, drain, body) device terminals, causing different degrees op operational changes in the output characteristics.
- As such the effects are more complex than in diode, and need significant modeling and characterization to clarify.
- Expected shifts in I-V characteristics, gain, I/O impedances, threshold voltages and other parameters can be simulated, but need to be verified with carefully controlled experimental investigation (section C).
- The devices and gates will be experimentally studied both under injected and incident RF radiation.
- RF pulse width, height and repetition rate are main parameters in this study.

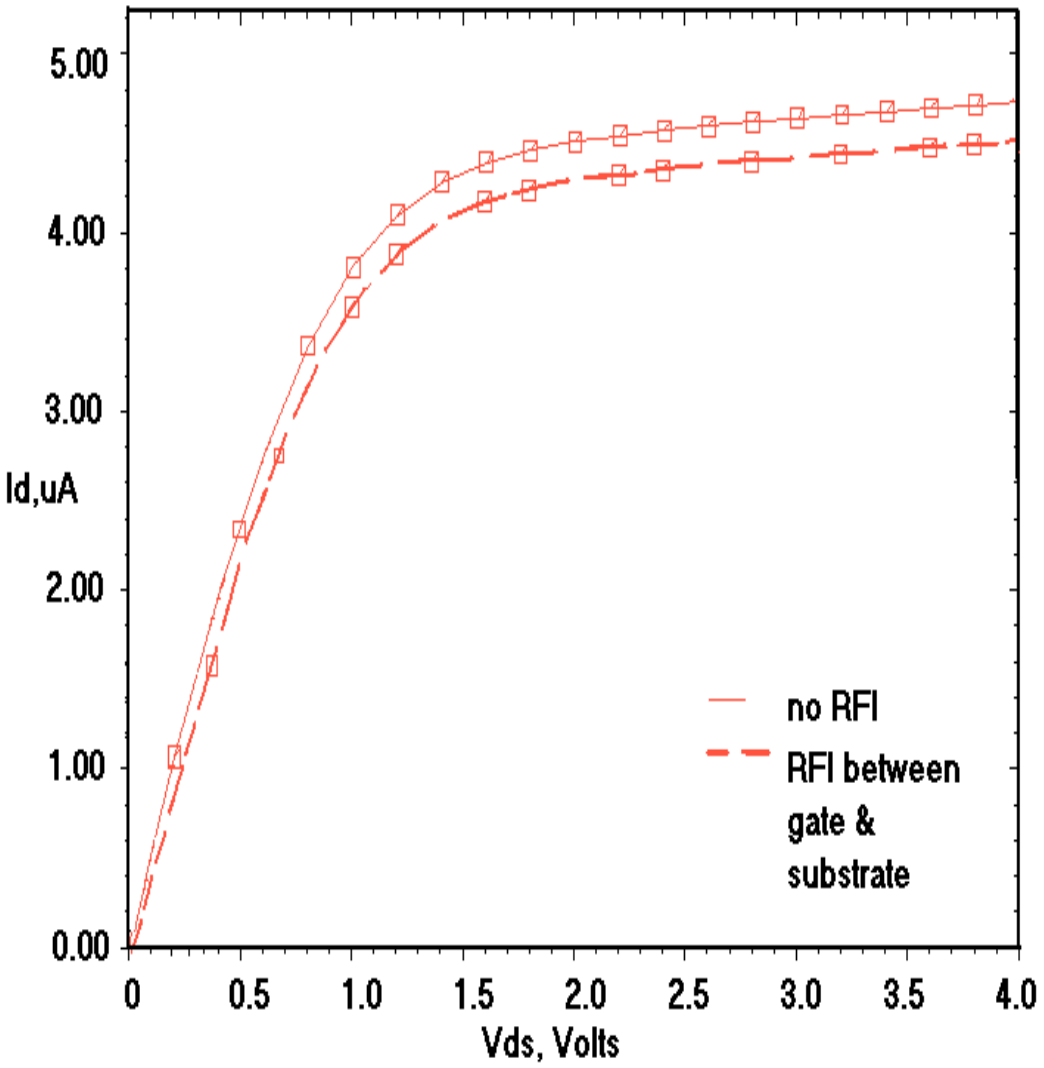
MOSFET Transient Drain Current due to RF at Gate

- **Example:**RF coupling between gate and body
- Simulated drain current using **MEDICI**-Avant! simulator
- Red line is the quiescent point for device
- **Non-symmetrical** drain current waveform with a negative shift is evident from this simulation



MOSFET I-V Output Characteristic with RF

- **Example:**MOSFET I-V characteristics derived using **MEDICI-**Avant! device simulator.
- DC drain current curve shifts downwards due to RFI between gate and body (as shown by dashed line).
- Experimental verification necessary



"Sense and Protect" Schemes

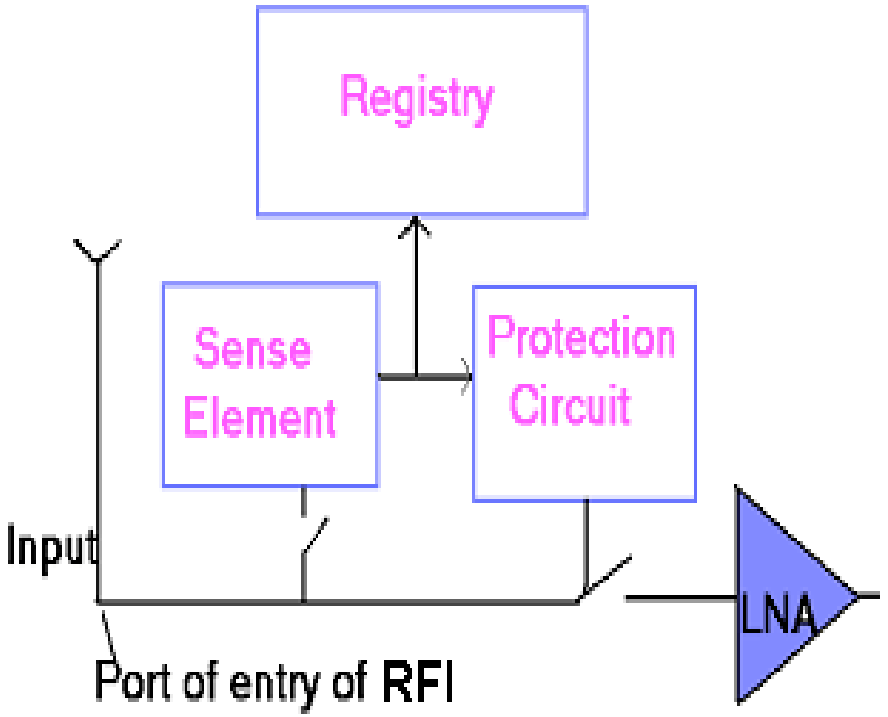
- Protection schemes for most sensitive areas need to be developed.
- Assume RF signals couple through I/O/antenna ports, and neglect bouncing signals within the packaged chip (section B –Chaos theory).
- RF signals in amplitude larger than a few hundred mV and with frequency greater than a 100kHz are considered.
- Signals of smaller amplitude are considered noise or legitimate signals and have to be treated separately.
- "Sense" and "disconnect" circuit at RF port of entry proposed for an antenna/LNA communications module.
- Sense and protect circuit **integrated on-chip with LNA.**
- Scheme can be adapted for use in all other susceptible ports.
- Scheme also generates control signals to register RF events.

Desirable Features for Protection Circuit

- Fast disconnect response capability upon RF occurrence.
- Fast re-connect capability upon RF event termination.
- Efficient disconnect capability with minimal coupling with LNA in the off-state .
- Protection can be designed for wide frequency and amplitude range of events.
- Minimal LNA redesign to accommodate protection circuit.
- On-chip design simple and cost-effective when using same family of devices (in this case MOSFETs).

"Sense and Protect" Circuit Concept

- Sense element based on MOSFET well characterized devices.
- Protection based on fast switches.
- Efficient disconnect capability with minimal coupling to the rest of circuit in the off-state
- Neural net based registry counts RF events.
- Designed for wide frequency and amplitude range of events



Schematic of Protection System

Protection Circuit Features

- Response time to disconnect LNA is targeted at the ns range.
- Restoration of connection after RF event is usually longer and depends on the duration of the RF event.
- For high GHz range protection,system must be scaled-down to sub-micron scale.
- Protection effective for RF voltages >500mV (adjustable to lower levels) to large voltages until physical damage occurs.

Summary

- The experimental study of RF effects on electronic systems will proceed by examining the effects on the fundamental units of which ICs are composed: MOSFETs and CMOS gates.
- Initial results using MEDICI device simulator indicate complex behavior that needs to be experimentally evaluated.
- A versatile “sense and protect” scheme based on well characterized MOSFET devices is proposed and its features outlined.
- System has potential for GHz frequency protection by scaling technology to smaller feature size MOSFETs.
- The study targets the understanding of failure under RFI and the development of RF hardened ICs by improved device/system design and the use of improved materials.