Final Performance Report

AFOSR Grant Number F496200110374

Descriptive Title: "Effects of High Power Microwaves and Chaos in 21st Century Analog and Digital Electronics"

Grantee Institution: Institute for Research in Electronics and Applied Physics
University of Maryland, College Park, MD 20743-3511

Principal Investigator: Victor L. Granatstein

Co-Principal Investigators: Steven Anlage

Thomas M. Antonsen, Jr.

Neil Goldsman

Agis Iliadis

Bruce Jacob

John Melngalis

Edward Ott

Omar Ramahi

John Rodgers

Subcontract to: Boise State University
Principal Investigator, R. Jacob Baker;
Co-Principal Investigator, William B. Knowlton

Reporting Period: September 1, 2005 to July 31, 2006

TABLE OF CONTENTS

1. Introduction and Objectives

This is the sixth and final report on the MURI 2001 program, "Effects of High-Power Microwaves and Chaos in Analog and Digital Circuits", being carried out at the University of Maryland, College Park (UMCP) with subcontract to Boise State University. The program was initiated in May 2001 and ended on July 31, 2006. The present report covers the period September 1, 2005 to July 31, 2006. The objective is to study at a fundamental level the effects of high power microwave pulses and chaos in electronic devices, circuits and systems that might lead to upset or damage.

The program at UMCP has four interrelated parts as follows:

1. Chaos studies, especially wave chaos which provides a statistical description of microwave field in complex topologies such as circuits in boxes;
2. Analysis, simulation and testing of microwave effects on devices, circuits and systems. The testing is primarily in the frequency range 300 MHz to 10 GHz while pulse duration and power level are varied;
3. Custom-design and fabrication of integrated circuits with on-chip microwave diagnostics;
4. Studies of enclosures and shielding.

Progress in the current reporting period on each of these topics at UMCP will be reported in section 3 of this report. Section 2 will summarize the status of the research with stress on the major accomplishments in the five-year long program.

A separate report of progress at Boise State University is appended.

2. Status of Effort

Our studies in the area of wave chaos have yielded a stochastic formalism, the Random Coupling Model (RCM), for describing the statistical properties of 3-dimensional microwave cavities which can support multiple modes and have a complex geometry including ports and wall loses. Salient predictions of this formalism have now been confirmed experimentally for both the one-port and two-port cases. The two-port studies in particular are enabling one to predict the probability distribution function of electric field on an electronic component inside a partially shielded enclosure from a knowledge of microwave power entering a "port" (such as a cooling vent) and minimal information about the properties of the enclosure (such as cavity dimensions compared with wavelength and cavity Q); the formalism allows the "target" electronic component to be viewed as the output "port". In recent theory progress, we have developed a code which simulates pulse-modulated signals interacting with chaotic microwave cavities. We have also included in this report a comparison of our RCM approach with the approach for EM modeling in complicated cavities at Sandia National Laboratory; our approach is not limited to 2-D analysis and essentially encompasses all the features of the Sandia model.

We have also included in this report a description of recent progress in circuit chaos studies. A basic investigation of chaos resulting from the nonlinearity of the p/n junction was carried out with a stress on the role of various time scales involved. The diode reverse recovery time was found to play a central role in the onset of chaos. In place of the "classical" lumped

parameter Resistor-Inductor-Diode (RLD) circuit which has exhibited chaos when excited at relatively low frequencies (kHz to MHz), we have studied a distributed parameter transmission line terminated in a diode. We have observed chaos in this circuit at driving frequencies in excess of 1 GHz. Nonlinear dynamics and chaos can serve as an organizing principle in understanding microwave effects in circuits.

On the topic of microwave effects in circuits and systems, a ubiquitous vulnerability to high power microwave attack has been identified. This involves down-conversion of the microwave signal frequency by the Electro-Static Discharge (ESD) diodes that are present in almost all modern electronic systems. The down-converted signals change voltage levels in the circuits leading to system upset. The effects are greatly magnified at spurious circuit resonances in the frequency range 0.3 - 3 GHz; such resonances involve the capacitance of the ESD diodes and lead inductances. Various circuit upset mechanisms have been studied experimentally and successfully modeled with PSPICE. Upset was found to occur for an RF injected voltage between 0.4 - 1 Volt.

In experiments on RF effects, we moved beyond our studies of upset in circuits to include studies of effects in systems. The parasitic inductance-diode-conductance model developed previously proved to be very effective at predicting effects in a wide variety of integrated circuits. However, when many thousands or even millions of these circuits are combined into networks and ultimately into systems, the cascaded interaction between many electronic stages could generate new dynamics and upset mechanisms. As a result of the continued decrease in the size of advanced integrated circuits, the margin of error for signal voltages and transient levels have become very small. Consequently, signal integrity and system stability have become critical reliability issues. Circuit controllers and power regulators are often required to provide timing and voltage levels, respectively, with very tight tolerances. In order to achieve a high degree of operating stability, these circuits typically include sensors which feed back status signals to systems regulators. Often, the response of the control loop must be fast (wideband) in order to maintain stability during transient operating conditions. The gain bandwidth of the loop must be restricted (usually with filters) to reject noise and spurious electromagnetic interference (EMI). However, these networks reject signals only over a limited bandwidth. . We have found that that some high frequencies pass through the filter with minimal attenuation due to parasitic elements in the network. This effect working in concert with circuit nonlinearity can produce upset in systems at microwave frequencies.

These upset studies provide an informed basis for developing High Power Microwave (HPM) sources that might be used to degrade electronics. One should develop sources in L-band with peak power in the range 1-100MW that have high power spectral density that and at the same time cover a wide bandwidth. A candidate source would be a high power BWO with delayed feedback which could be made to operate chaotically. Such an oscillator would produce an output with high spectral power density and with stochastic frequency hopping over a wide band.

As mentioned above, upset was found to occur in our experiments with injected RF voltage in the range 0.4-1 Volt. At higher RF voltage levels exceeding 2 volts device damage is expected. A semiconductor simulation tool which we have developed models breakdown inside

MOS transistors. The thin oxide layer in the MOSFET gate region is susceptible to electron avalanching and punch-through. In contrast to circuit simulators such as SPICE, our device simulator probes inside transistors to locate precisely where damage occurs. Extensive studies of MOSFET damage due to HPM exposure have been carried out by the group at Boise State University as reported in the appendix of this report.

Another important aspect of our studies concerns modeling of Electromagnetic (EM) coupling and performance of interconnects in Integrated Circuits (ICs). EM coupling from point to point within integrated circuits causes performance degradation and can lead to failure. In this report, we describe a random impulse response method for characterizing on-chip interconnects. The method uses a coupled time and space domain impulse response (Green's function) approach to fully characterizing a chip. Once a chip is characterized, its response to any microwave input can be predicted; the microwave input can be either random or deterministic.

On the topic of developing on-chip microwave detectors, we can report that three kinds pulsed power detectors have been fabricated and tested; viz., Focused Ion Beam (FIB) fabricated Schottky diode, Schottky diodes fabricated on a CMOS processed chip and a MOSFET power detector circuit. The best performance parameters achieved included a dynamic range of 36 dB, a sensitivity at 1 GHz of -21dBm, and a pulse risetime of 56 nanoseconds.

Finally, in the area of HPM mitigation technologies two efforts have been undertaken. The first has developed a robust computer architecture which can compensate for a detected HPM attack. This architecture has been implemented and a prototype chipset has been fabricated. The second effort involves studies of enclosures and shielding. Here, lossy material coatings have been shown to be effective in reducing radiation penetration through apertures. Also, magnetic bandgap structures have been shown to be effective in significantly reducing RF "noise" in printed circuit boards and in reducing RF coupling between cavities.

3. RESEARCH ACCOMPLISHMENTS

3.1. Chaos Studies

(Prof. Thomas M. Antonsen Jr., Prof. Edward Ott, Prof. Steven Anlage.
Students: Vassili Dermergis, James Hart, Sameer Hemmady, X. Henry Zheng)

3.1.1 Wave Chaos and the Random Coupling Model

We have examined the general question of microwave effects on electronics from the perspective of nonlinear dynamics and chaos. We have developed a quantitative statistical theory of induced voltages for objects inside complicated enclosures and subjected to microwave attack. This theory has been verified through extensive measurements in an idealized microwave enclosure, as well as in a computer box. The understanding gained from this combined theoretical and experimental effort has been imparted to DoD through our Random Coupling Model web site and code (see http://www.csr.umd.edu/anlage/RCM/index.htm).

The theory begins by considering electronics contained within complicated metallic enclosures (such as an avionics bay or an aircraft fuselage). For short wavelength waves in complex geometries the field distributions are highly sensitive to frequency and/or small perturbations. Very often the ray trajectories will be chaotic, setting the stage for our theoretical approach. Under these circumstances it is essentially impossible to directly calculate the field patterns of the enclosure with great precision. The system is simply too sensitive to perturbations. The only alternative for a quantitative understanding of what happens is to use a statistical description of the fields.

Our Random Coupling Model (RCM) shows that the resulting statistical properties are described by a single parameter that depends on a special combination of three things: the volume and loss of the enclosure, as well as the frequency of the attacking waveform. The other essential ingredient of the RCM is knowledge of the radiation impedance properties of the ingress points of the enclosure, as well as the target electrical component of interest. With this information, we can construct a complete statistical description of the induced voltage on the target component.

The RCM predictions have been examined in great detail through microwave experiments on ray-chaotic enclosures such as a computer box (containing all of its components) and a small mode-stirred chamber. The computer box experiment is illustrated in Fig. 1.

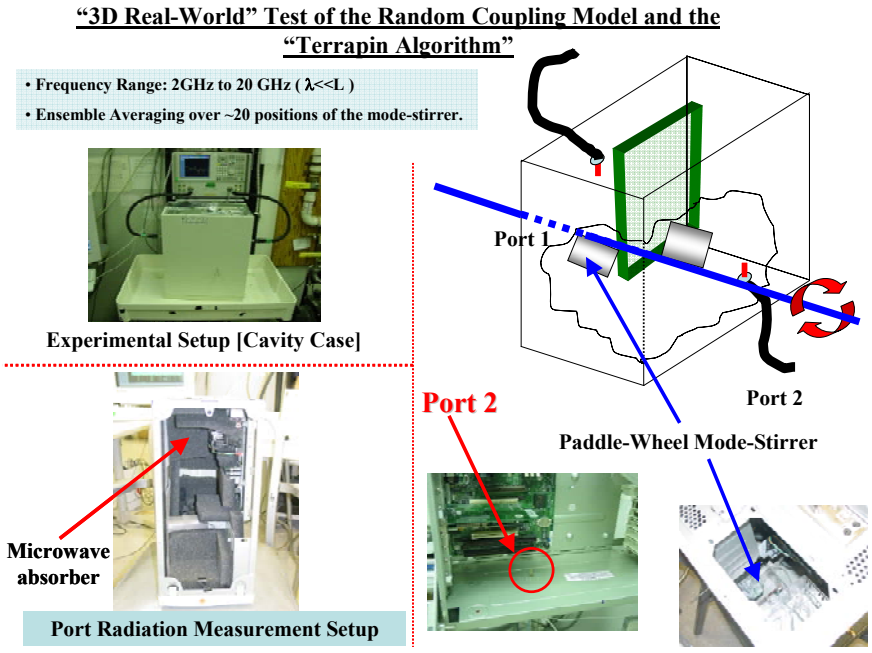


Fig. 1. Computer box experimental test of the Random Coupling Model. Clockwise from upper left: measurement of the computer box with a vector network analyzer, illustration of paddle wheels inserted in the box, one of the ports on the box, illustration of the radiation impedance measurement.

The measured statistical quantities are illustrated in Fig. 2. In this case we had two coaxial antennas inserted through the walls of the computer box. One antenna broadcast an "attacking waveform" with spectral properties shown in the upper parts of Fig. 2. Fig. 2(a) shows a flat power profile from 8 to 9 GHz, while Fig. 2(b) shows a Gaussian profile between the same two frequencies. The main parts of Fig. 2 show the resulting statistics of induced voltages on antenna 2 (representing a component inside the box). The stars are the measured probability distribution function (pdf), while the solid red lines are the predictions of the RCM. Good agreement is observed.

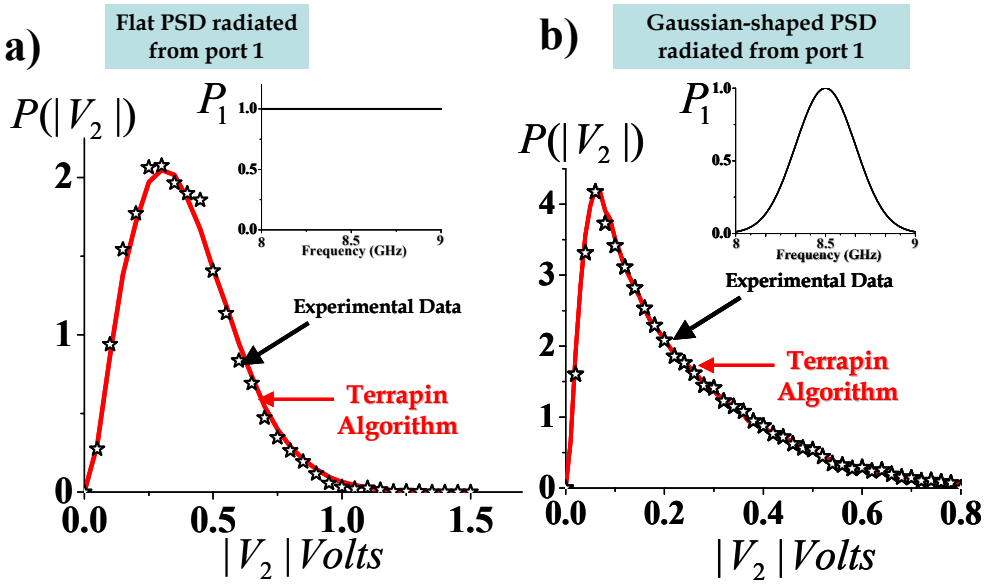


Fig. 2 Statistics of induced voltages in the computer box. The upper plots show the power-frequency profile (power spectral density – PSD) of the signal applied to antenna 1, while the main plots show the pdf of voltages induced in antenna 2.

At the MURI'01 Final Review in Albuquerque in July, 2006 we gave out 32 copies of our RCM software to the attendees.

3.1.2. Nonlinear Dynamics and Chaos as an Organizing Principle for Microwave Effects

The evidence for HPM effects on electronics is anecdotal and at best statistical in nature. Many questions have arisen: How reproducible are the effects? Can we predict effects with confidence? Are there unrecognized and qualitatively new ways to produce effects out there that nobody has forseen?

Our approach to this problem has been to frame the questions in the context of the quantitative theory of nonlinear dynamics and chaos. We believe that this point of view allows one to create a sound scientific approach to understanding HPM effects, creates a systematic

framework in which to conceptualize, quantify and classify HPM effects, and may provide new opportunities for circuit upset and failure.

The most common nonlinear object that is found in all electronics is the p/n junction. This object enjoys several types of nonlinearity:

- Nonlinear current - voltage characteristic, leading to rectification of high frequency signals.
- Voltage-dependent capacitance, leading to chaotic oscillations of voltage on the junction under suitable circumstances.
- Nonlinear reverse recovery effects leading to nonlinear feedback on the junction and also leading to chaotic voltage oscillations under suitable conditions.

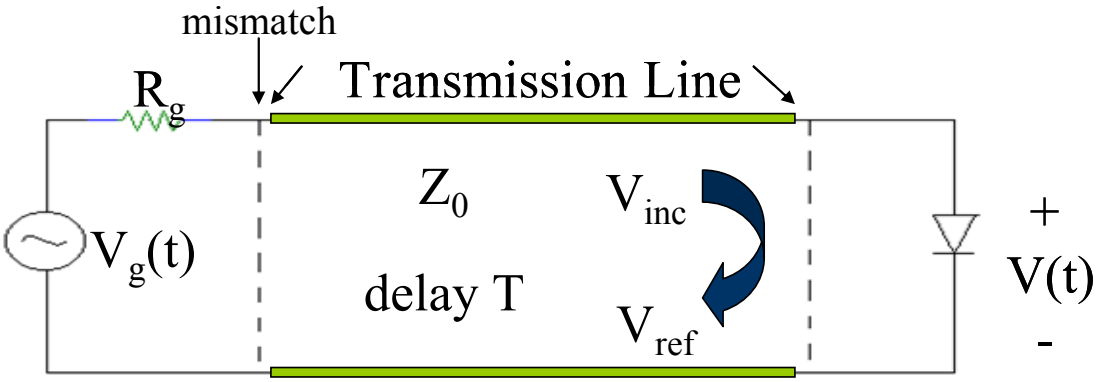
The first two types of nonlinearity had been fairly intensively investigated before we began our work. Most of this work had studied the nonlinear dynamics of the p/n junction at kHz and low-MHz frequency scales. Because modern electronics operates at the upper-MHz and GHz frequency scales, we decided to generalize the existing work and look at chaos at higher frequencies. This led us to examine the third type of nonlinearity, nonlinear delayed feedback caused by the finite reverse recovery time (τRR) due to the dynamics of minority charge accumulation in the p/n junction. The reverse recovery time of p/n junctions ranges from the ms to the sub-ns time scale, depending on materials, junction doping profiles and geometry. We did a basic study of how reverse recovery limits the range of parameters that lead to chaos in a driven p/n junction [1].

We also investigated what happens when a p/n junction is embedded in a complicated circuit topology [2]. This work was motivated by work in the former Soviet Union suggesting that a 2-tone stimulus could make circuits suffer a chaotic instability at very low input power levels. We found that the circuit could be driven into chaos at low frequencies (~MHz) due to irradiation at much higher frequencies (~GHz). This was explained in terms of a combination of all three nonlinearities listed above.

Continuing to generalize to higher frequencies, we recognized a major vulnerability of modern electronics, namely the p/n junctions contained in Electrostatic Discharge (ESD) circuits. All integrated circuits are protected from low-frequency voltage spikes by a ring of ESD diodes. However, at higher frequencies these ESD components can be resonant with parasitic inductances, leading to nonlinear oscillation. In addition, these ESD diodes lie at the end of transmission line circuits which support waves moving in both directions. If there is an impedance mismatch on the transmission line, it will lead to a nonlinear delayed feedback on the p/n junction, possibly giving rise to chaotic oscillations.

We studied the ESD chaotic instability through the simple model illustrated in Fig. 3. The harmonic source drives the diode at the end of a transmission line giving rise to a delay T. The source is mismatched with the transmission line, giving rise to reflected and re-reflected signals that come back to the diode at integer multiples of the delay time T. We wrote down the equations for this system and solved them numerically. They show period doubling and chaos under suitable conditions. Experiments were carried out to test the theory [3]. The results are shown in Fig. 4 as a bifurcation diagram and as a spectrum of diode voltage in the chaotic state.

It was possible to induce period doubling and chaos in a variety of diodes under a variety of experimental conditions.



A simple model of p/n junctions in computers

Fig. 3 Model of a diode-terminated transmission line, with impedance mismatch with the driving harmonic source.

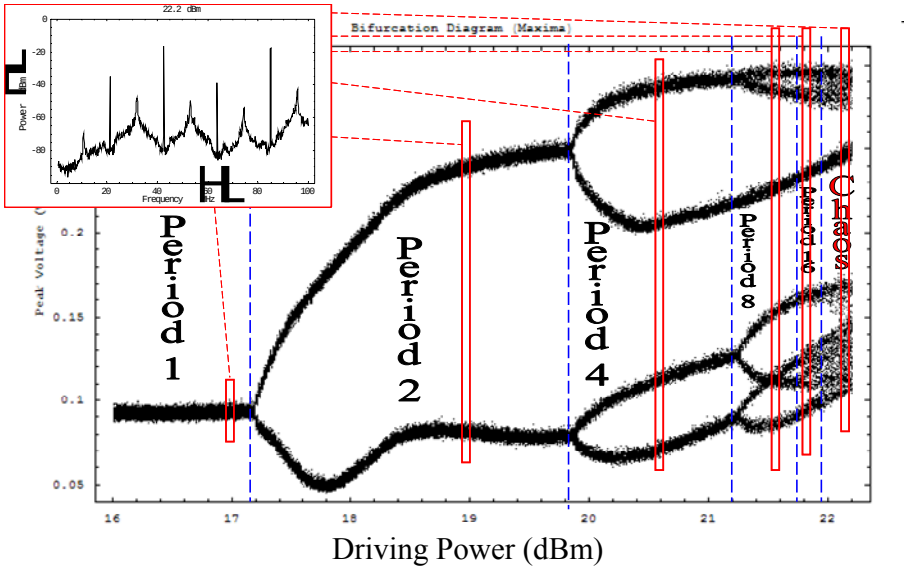


Fig. 4 Bifurcation diagram of a driven diode transmission line system, driven at 85 MHz with the driving power shown on the horizontal axis. The vertical axis shows values of voltage on the diode sampled once every period of the driving signal. The inset shows a spectrum of the diode voltage in the chaotic state.

We conclude that nonlinearity and chaos are ubiquitous phenomena in modern electronics, facilitated mainly by the presence of p/n junctions. Future work would be to unify our wave chaos and circuit chaos studies into a unified description of nonlinearity, wave chaos and circuit chaos. We also believe that more efficient driving signals can be created to create nonlinear instabilities in a wide variety of modern circuits and systems.

References

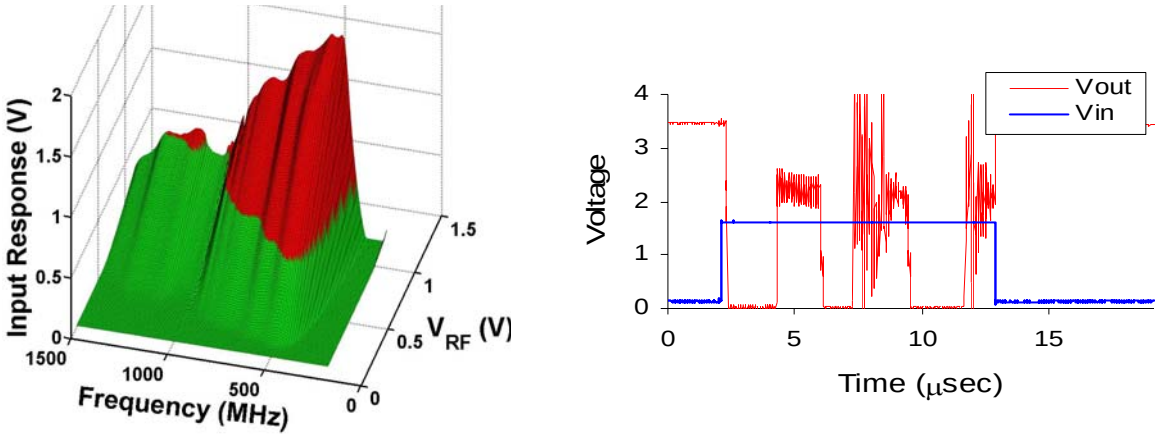
1. Renato Mariz de Moraes and Steven M. Anlage, "Unified Model and Novel Reverse Recovery Nonlinearities of the Driven Diode Resonator," *Phys. Re5. E*, **68**, 026201 (2003).
2. Renato Mariz de Moraes and Steven M. Anlage, "Effect of UHF Stimulus and Negative Feedback on Nonlinear Circuits," *IEEE Trans. Circuits Systems I: Regular Papers*, **51**, 748 (2004).
3. Vassili Demergis, Alexander Glasser, Marshal Miller, Thomas M. Antonsen, Jr., Edward Ott, Steven M. Anlage, "Delayed Feedback and Chaos on the Driven Diode-Terminated Transmission Line," submitted to *Chaos* (2006).

3.2 Microwave Effects on Electronics

(Prof. Neil Goldsman, Prof. Victor Granatstein, Prof. Agis Iliadis, Prof. Bruce Jacob, Prof. Omar Ramahi, Dr. John Rodgers.
Students: Vincent Chan, Cagdas Dirik, Todd Firestone, Kyechong Kim, Laise Parker, Bo Yang)

3.2.1 Microwave Effects in Circuits and Systems

Our previous work focused on RF effects on the integrated circuit level. There is reasonable concern about the threat to electronics imposed by high-power microwave (HPM) sources with complex waveforms. RF effects from microwave pulses whose amplitude is less than the operating voltages in integrated circuits were studied extensively at the University of Maryland [1-2]. This work showed that high-frequency parasitic elements and on-chip ESD protection devices in integrated circuits had resonant frequencies in the microwave regime with quality factors as high as seven. When excited near resonance, these elements produced gate voltages at the input transistor that were higher than the amplitude of the RF pulse. These studies resulted in the development of a new effects model of the high-frequency, nonlinear response of ESD protection devices in integrated circuits. The networks cause upset and instability in circuits when driven by out-of-band carriers with wideband modulation. Figure 1 shows an example of the input and output response in advanced, low-voltage CMOS when excited by microwave pulses with such modulation. The figures show that circuits can exhibit complicated dynamics that may lead to bit errors, oscillation and undefined logic states.



(b)

Fig. 1 Example of the measured response in high-speed CMOS integrated circuit showing (a) voltage gain characteristics due to parasitic resonances, and (b) the instability in the output voltage caused by microwave pulses.

Studies of Systems-Level Microwave Upset

In 2006, research efforts were concentrated on studies of HPM effects in systems. The parasitic inductance-diode-conductance model developed previously proved to be very effective at predicting effects in a wide variety of integrated circuits. However, when many thousands or even millions of these circuits are combined into networks and ultimately into systems, the cascaded interaction between many electronic stages could generate new dynamics and upset mechanisms. Thus, a thorough investigation of system effects was commenced in the later half of 2005 and continued through to the end of the MURI in 2006. In the following, a brief summary of this work is presented.

As a result of the continued decrease in the size of advanced integrated circuits, the margin of error for signal voltages and transient levels have become very small. Consequently, signal integrity and system stability have become critical reliability issues. Circuit controllers and power regulators are often required to provide timing and voltage levels, respectively, with very tight tolerances. In order to achieve a high degree of operating stability, these circuits typically include sensors which feed back status signals to systems regulators. Often, the response of the control loop must be fast (wideband) in order to maintain stability during transient operating conditions. The gain bandwidth of the loop must be restricted (usually with filters) to reject noise and spurious electromagnetic interference (EMI). Furthermore, the parasitic resonances described above are distributed according to the functional hierarchy of the circuit within a given system. Typically, smaller faster devices (e.g. microprocessor) have higher resonant frequencies than larger ones (e.g. input/output). Figure 2 shows the measured distribution of resonances in a typical digital communication system.

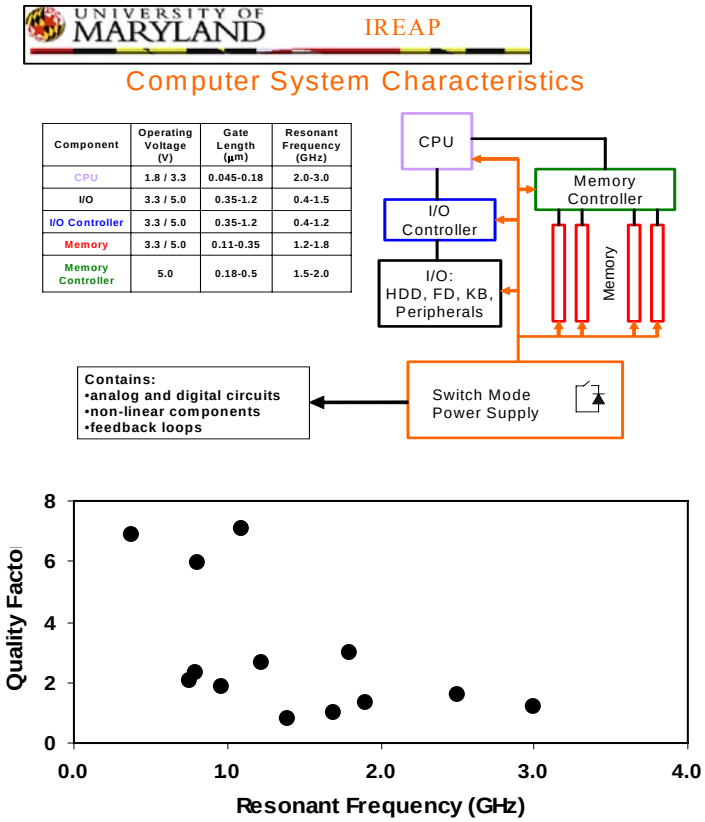


Fig. 2 The hierarchical nature of the devices that comprise a typical digital communications system leads to distributions of parasitic resonances and quality factors leading to HPM susceptibility over a fairly wide frequency band.

In previous work by other research groups, various HPM effects models have been developed wherein semiconductor junctions are considered as simple diodes. This approach gives a fairly good prediction of upset thresholds below VHF frequencies. The data in Fig. 2 demonstrates that an improved treatment was necessary. We solve the time-dependent diffusion equation (1) for ESD junctions. The advantage of this approach is that the parameters in (1) can be directly extracted from the physical layout of the device. This allows the model to be accurately scaled according to the process used to manufacture the circuit.

$$\frac{\partial \Delta p(x,t)}{\partial t} = D_p \frac{\partial^2 \Delta p(x,t)}{\partial x^2} - \frac{\Delta p(x,t)}{\tau} \tag{1}$$

$$I_{diff} = qA \frac{D_p}{L_p} \frac{n^2}{N_D} (e^{\frac{qV_d}{kT}} - 1) \tag{2}$$

$$Y_D = \frac{i_D}{v_D} = G\sqrt{1 + j\omega\tau} \tag{3}$$

In (2) the diffusion current is solved in terms of these scalable device parameters and (3) is the frequency-dependent admittance. Figure 3 shows a comparison of the measured and calculated response of a typical high-speed circuit to microwave pulses.

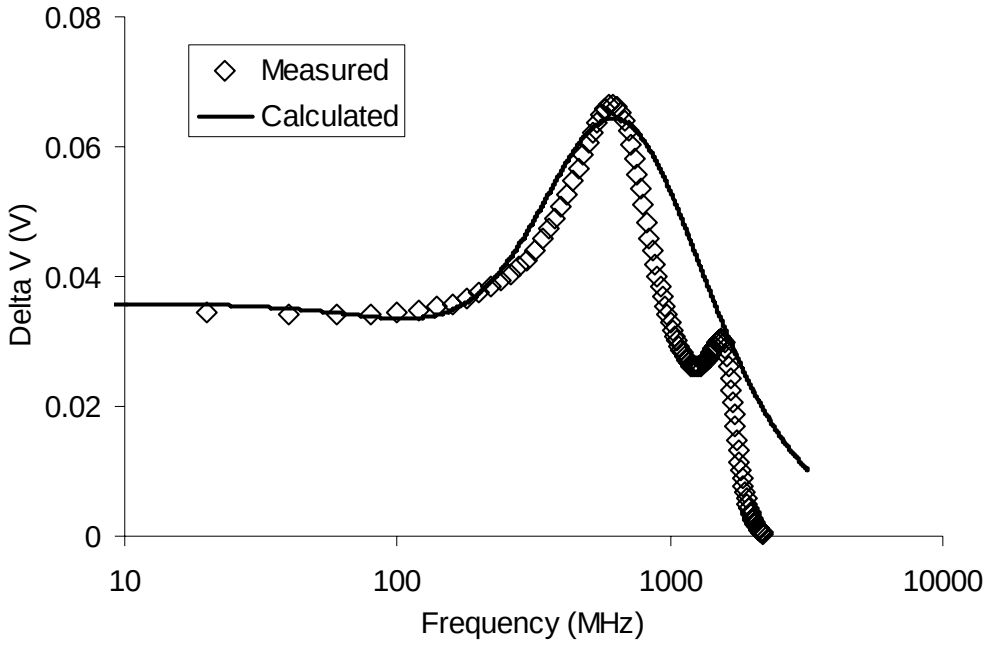


Fig. 3. Comparison of the measured and calculated response vs. the carrier frequency of pulsed microwave excitation of the ESD drain-bulk junction in a high-speed CMOS circuit.

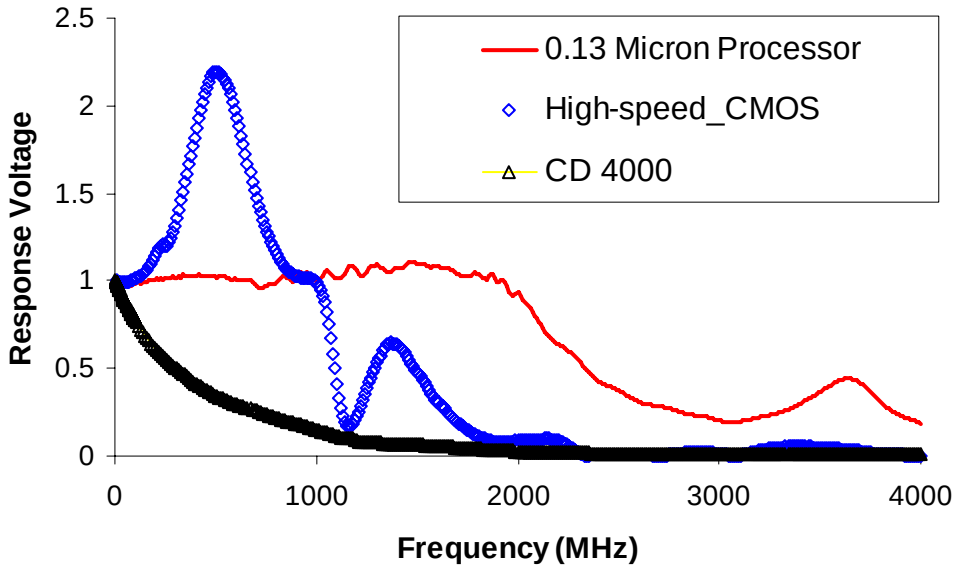


Fig. 4. Comparison of the microwave response of various device families. The CD400 CMOS operated at slower speeds and is based on micron-scale semiconductor processes. Thus, its response to RF pulses falls to negligible levels at frequencies above a few hundred MHz. Advanced devices, however, exhibit significant susceptibility up to several GHz.

Summary of Significant Research Milestones

- The mechanisms that generate HPM upset in electronics have been investigated and characterized in terms of basic circuit parameters.
- How susceptibility scales according to process technology, device function, switching speed and bias voltage has been established.
- A new scalable effects model which accurately predicts upset thresholds has been developed and benchmarked against experimental results with good agreement.
- Initial studies of HPM effects in systems have been completed. Results showed the effectiveness of wideband microwave sources at upsetting electronic systems.

References

1. T.M. Firestone, J. Rodgers and 5.L. Granatstein, "Response of CMOS Logic with Electrostatic Discharge Protection to Pulsed Microwave Excitation Submitted to IEEE Trans. on Circuits and Systems.

2. T. M. Firestone, "RF Induced Nonlinear Effects in High-Speed Electronics" Masters of Science Thesis, University of Maryland, May 2004.

3. J. Rodgers, T. Firestone, 5. L. Granatstein, 5. Dronov, T. M. Antonsen, Jr., and E. Ott, "Study and applications of wideband oscillations in high-power pulsed traveling-wave tubes," Proceedings of the Sixth International Vacuum Electronics Conference IVEC 2005, Noordwijk, The Netherlands, April 2005.

3.2.2 Experimental Studies of High Power Microwave Interference Effects on CMOS ICs.

Summary of Research Highlights

Our project has focused on characterizing and identifying the effects of microwave signals on the fundamental units in integrated circuits (ICs) such as (1) MOSFETs, (2) CMOS inverter gates, and (3) digital automotive control ICs, in order to provide a better understanding of the critical processes and mechanisms for upsets and failures in electronic IC's and systems. MOSFETs: The study showed that injected microwave interference (referred as electromagnetic interference-EMI) significantly affects output current, transconductance, output conductance, and breakdown voltage for power levels above 10 dBm in the frequency range between 1 and 20 GHz. The effects (Fig. 1) result in the devices loosing switch-off capability, saturation and linearity in the amplification region of their output characteristics, developing DC offset currents at zero drain bias, reducing breakdown voltages, and suffering gate oxide breakdown. Most importantly sensitivity to microwave interference was suppressed at frequencies above 4 GHz for these devices, found to be due to the by-pass capacitor effects of the intrinsic capacitors which provide a path to ground for EMI [1].

CMOS inverter gates: Degradation of static operation in CMOS inverters resulted in not only significant increases in static power dissipation but serious static noise margin compression

and loss of regenerative signal properties as well (loss of noise immunity), causing bit-flip errors at inverter clusters (Fig. 2). Measured load-line characteristics showed that the changes in the quiescent point (Q) of operation due to current increase at n and p-MOS in inverters is responsible for the static noise margin compression [2]. EMI disrupted the integrity of dynamic operation by causing substantial changes in propagation delays and output voltage levels, while significant increases in dynamic power dissipation, were observed. An analytical Parameter Extraction Method (PEM) was developed, that allows the prediction of output voltages and currents, propagation delays, and dynamic power dissipation under EMI, from static measurements. Analysis based on this method revealed upsets in the power distribution budget due to substantial increases in short-circuit currents [3]. A new bit-flip error vulnerability while at the threshold voltage (VTHN) (Fig. 3), and critical latch-up events due to parasitic bipolar transistor action with pulsed microwave interference, were identified [4]. Measured current transfer characteristics with pulsed microwave interference also suggested that the observed substantial output current increase is due to charge effects rather than thermal effects (Fig. 4). Digital automotive control ICs (Timers)-collaboration with J. Volakis group: EMI on timer circuits resulted in reduced output pulse width and period, output voltage decrease and saturation to VDD or ground, and irregular timing at the output voltages. These upsets caused critical soft errors due to substantial degradation of the dynamic operation (output voltage swing and propagation delay changes) of the CMOS inverters, and NAND gates that the CLK port of the timer consists of. Analysis using the PEM incorporated with SPICE program showed a good agreement with measurement results [5].

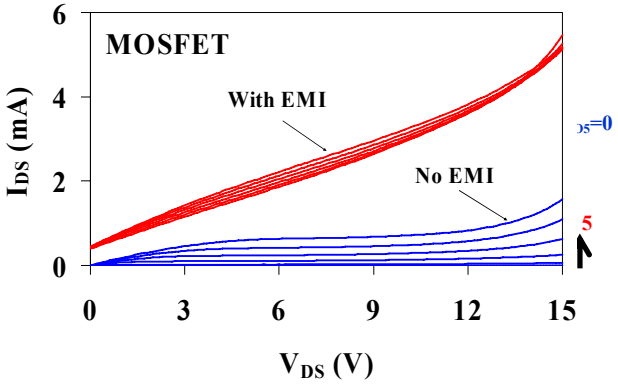


Fig.1. I-V characteristics of an n MOSFET output current with and without EMI.

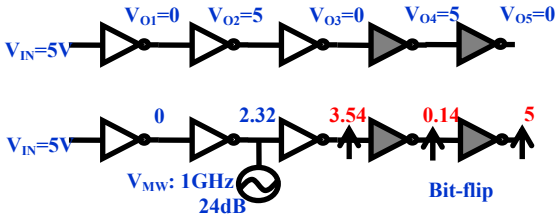


Fig. 2. Inverter clusters**:** ***Bit-flip errors*** due to loss of noise immunity in the digital system.

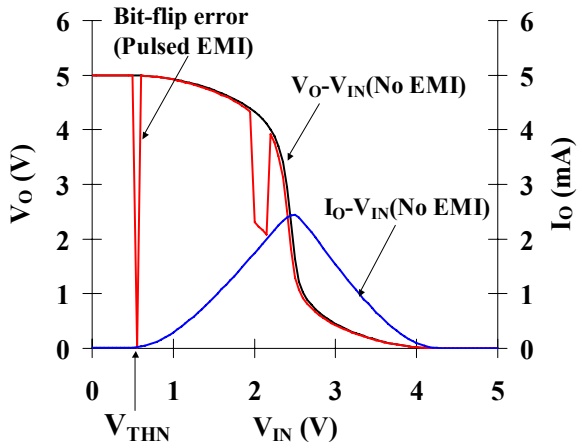


Fig. 3. Bit-flip error at V_{THN} with pulsed microwave interference.

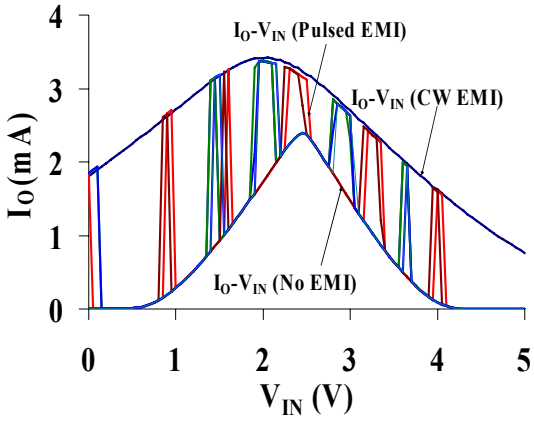


Fig. 4. Microwave pulse, 1.5ms of width, and 200ms of period. No significant changes from CW to pulsed EMI effects. Thus, observed current increases are due to excess charge generation rather than any thermal effects.

Detailed Description of Results Achieved

In this past year, we have developed the Parameter Extraction Method (PEM) which is a methodology allowing us to obtain dynamic characteristics of inverters under EMI using measured static load-line characteristics. Using the PEM, the changes in output voltages and currents, propagation delays, and dynamic power dissipation were obtained. The results showed severely compressed output voltage swings, and significantly changed propagation delays, as well as a large increase in dynamic power dissipation. The substantial changes in the quiescent operating (Q) point under microwave interference were observed to be responsible for the severe compression in the output voltage swing. Such severe compression is expected to result in critical bit errors in digital systems. This degradation in the output voltage together with the decrease in the charging and discharging currents (Fig. 5 and 6), resulted in changes in propagation delays ranging between -22% and 120%. Due to the substantial increase in the short-circuit currents the dynamic power dissipation showed a 95 to 184 % of increase, resulting in elevated currents that stressed the device Ohmic contacts and metal interconnects. As metallizations are rated for substantially lower current densities by design, catastrophic device failure is expected. In addition, such increase in the power dissipation would introduce a system upset by disrupting all power budget distribution, depriving operating currents from other units. Most prominent increase among the short-circuit currents is observed in the IPSC MW (steady), indicating that the p-MOS devices are more vulnerable to EMI. Most importantly, the effects of microwave interference were observed to be severe, as the bias voltage and device size were scaled down [3].

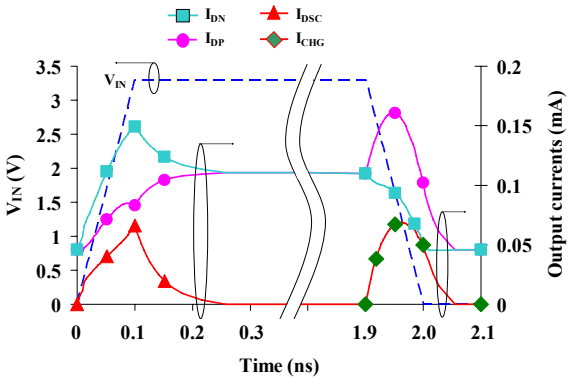


Fig. 5. Input voltage (dashed line) and output currents (color lines) of a 0.6µm inverter at V_{DD}=3.3V with 1GHz, 24dBm interference. Note that $I_{DSC}^{MW}= I_{DN}^{MW}-I_{DP}^{MW}$ and $I_{CHG}^{MW}= I_{DP}^{MW}-I_{DN}^{MW}$. Where I_{DSC}^{MW}, I_{DN}^{MW}, I_{DP}^{MW} and I_{CHG}^{MW} are the currents of discharging, n-MOS drain, p-MOS drain, and charging, respectively.

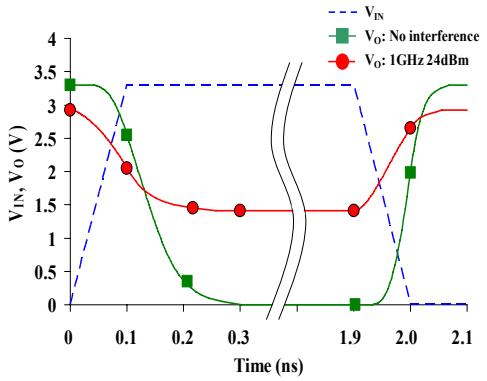


Fig. 6. Input (dashed line) and output voltages (color lines) of a 0.6µm inverter at V_{DD}=3.3V with and without 1GHz, 24dBm. interference.

The impact of disrupted input clock signals by EMI in automotive control ICs such as timers was investigated. For these experiments, Philip 74HC4017 Johnson Decade Counters and timers designed and fabricated with AMI 0.5µm technology were mounted on RT/Duroid 5880 PCB board. EMI and clock signal were combined using a hybrid power combiner and injected into the clock input port (Fig. 7) and the outputs were measured using the Tektronics 450 digital oscilloscope. The timers were biased 2-5V and clock frequencies ranged between 20KHz and 3.4MHz with 50% duty cycle. The timers were designed to operate with negative edge trigger signals. The microwave interference had frequency between 0.8 and 3GHz and power between 0 and 24dBm.

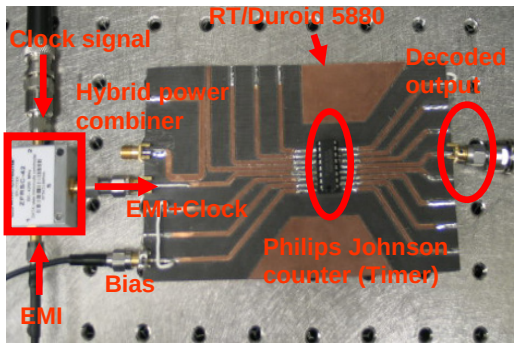


Fig. 7. Timer circuit and measurement setup to examine EMI effects.

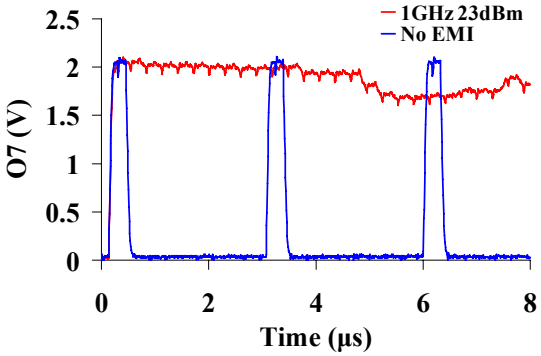


Fig. 8 Output voltage port (O7) of a Johnson timer with and without 1GHz 23dBm interference. Clock signal is 3.4MHz.

At 1GHz 23dBm, the output voltage (O7) saturates to VCC (2V) indicating that the device cannot turn off O7 properly (Fig. 8). The voltage level also changes with respect to time. At 3GHz, the timer showed gradual degradation in output O7. At 20dBm, output O7 drops to 1.14V

sufficient to cause upsets. It is evident that EMI severely degrades the device performance by invalidating the negative edge trigger. The clock input port (where the clock pulse is combined with the EMI signal), is a CMOS inverter. In order to understand the parameters of the upset mechanism, the dynamic characteristics of this inverter under EMI were obtained using the Parameter Extraction Method and modeled as an equivalent clock voltage source (VINV in Fig. 9 (a) and (b)). This equivalent clock voltage source at 1GHz 24dBm with 3.3V bias, is given in Fig. 10 (b). SPICE simulation with the equivalent clock source showed output voltage level (O7) saturation to VCC (3.3V) as shown in Fig. 9 (b). This result shows good agreement with the measurement result shown in Fig. 8. As shown in Fig. 9 (b), the output voltage low (VOL) and high (VOH) are changing from 0V and 3.3V (without EMI) to 1.42V and 2.92V (with 1GHz 24dBm), respectively. In addition, propagation delays increased to 155ps (tPLH) and 257ps (tPHL). This is substantial degradation of clock signal, which invalidates negative edge trigger. Therefore, the timer upsets can be attributed to these severely degraded output voltages (VOL and VOH) and the increased propagation delays in the inverter.

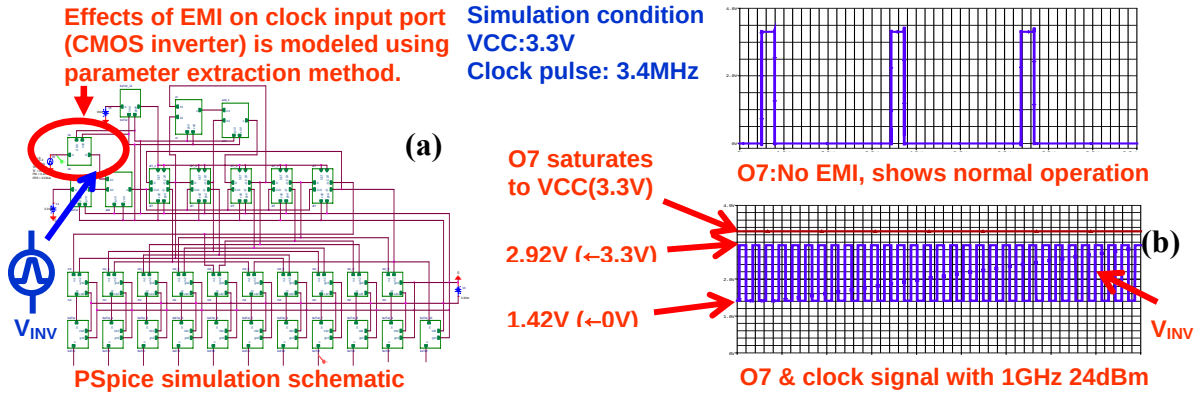


Fig. 9 (a) Schematic for SPICE simulation. (b) O7 and clock (V_{INV}) with 1GHz 24dBm.

The timer circuits designed and fabricated with AMI 0.5µm technology are shown in Fig. 10 and the schematic of the circuit is given in Fig. 11. The timer circuits consist of two edge trigger JK flip-flips and four decoder circuits as shown in Fig. 11. Especially, the clock input ports consist of two NAND gates and an inverter.

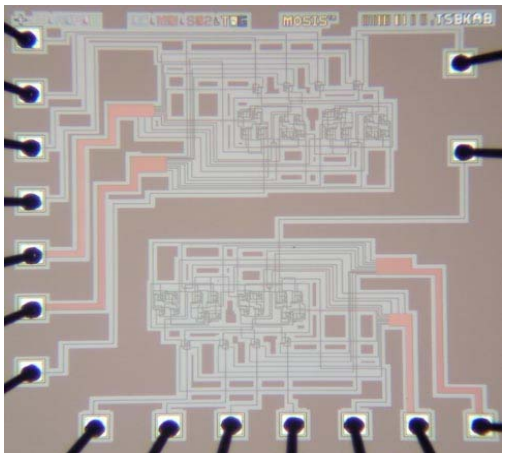


Fig. 10. Photo of timer circuits designed and fabricated with AMI 0.5µm Technology.

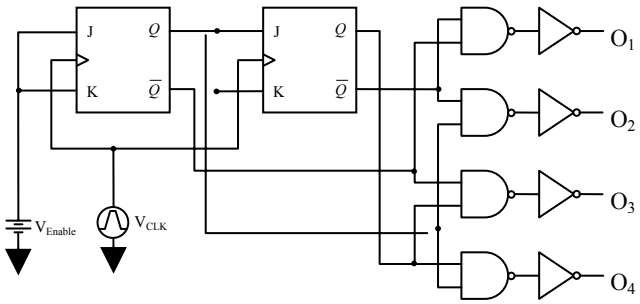


Fig. 11. Schematic of timer circuits. It consists of two JK flip-flops and four decoder circuits.

The output voltage (O1) of the timer with and without 1GHz EMI is shown in Fig. 12. The values of VCC and clock frequency were 3.3V and 100KHz, respectively. The figure shows that the output (O1) of the timer saturates to 0V at 1GHz 15dBm interference, and to VCC (3.3V) at 1GHz 20dBm. Thus, the timer cannot turn off properly. With 20KHz clock pulse, the timer shows an irregular pulse at 1GHz 18dBm. Moreover, at 22dBm, O1 shows not only an irregular pulse, but also a reduced width (from 58µs to 33.6µs) before it saturates to 0V at 23dB (Fig. 13). This results in serious violation of timing sequence for the circuits (O1→ O2→O3 →O4→O1……) and thus, failures in the automotive engine controls. These errors can also be attributed to the same upsets on the CMOS inverters and NAND gates at the clock input. Thus, severe changes in the output voltages (VOH & VOL) and delays in inverters [3], and quiescent point of operation changes in NAND gates are believed to be responsible for the timer upsets.

Threshold power levels causing upsets are given in Table 1. It shows that timers are most susceptible at 1GHz with 100KHz clock and 3.3V bias. As EMI frequency increases, more power is necessary to cause upsets and this is because at higher EMI frequency the intrinsic capacitances of n and p MOSFETs in the timer circuits, act as by-pass capacitors providing a path for EMI to the ground [1]. Thus, devices become less susceptible at higher EMI frequency, higher bias voltage, and lower clock frequencies.

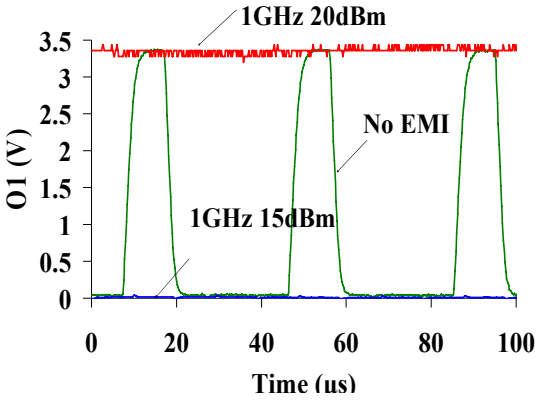


Fig. 12. Output voltage (O1) with and without 1GHz EMI. VCC=3.35. Clock freq: 100KHz.

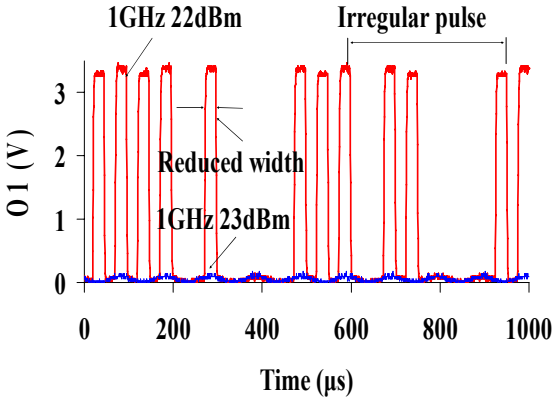


Fig. 13. O1 with 1GHz EMI. VCC=3.35. Clock: 20KHz.

	EMI Freq.	Threshold Power Level Causing Upsets	
		Clock: 100kHz	Clock: 20kHz
3.3V	1 GHz	15 dBm	18 dBm
	2 GHz	17 dBm	21 dBm
	3 GHz	18 dBm	22 dBm
5V	1 GHz	21 dBm	24 dBm
	2 GHz	X (No upsets)	until 24dBm
	3 GHz	X (No upsets)	until 24dBm

Table 1. Threshold power levels causing upsets with respect to EMI power and frequency, clock frequency, and bias.

References

1. K. Kim, A. A. Iliadis, 5. Granatstein, "Effects of Microwave Interference on the Operational Parameters of n-channel Enhancement Mode MOSFET Devices in CMOS Integrated Circuits", *Solid State Electronics*, Vol. 48 Issues 10-11, pp. 1795-1799, 2004.

2. K. Kim and A. A. Iliadis, "Impact of High Power Microwave Interference on Static Operation and Bit-Errors of CMOS Digital Circuits", *IEEE Trans. EMC*, in preparation.

3. K. Kim and A. A. Iliadis, "Impact of Microwave Interference on Dynamic Operation and Power Dissipation of CMOS Inverters", Submitted *IEEE Trans. EMC*, May 2006.

4. K. Kim and A. A. Iliadis, "Operational Degradation and Bit-Errors in CMOS Inverters due to Pulsed Microwave Interference", *IEEE Trans. EMC*, in preparation.

5. Y. Bayram, K. Kim, P. C. Chang, J. L. Volakis, A. A. Iliadis, "High Power EMI on Digital Circuits within Automotive Structures", Submitted in *2006 IEEE International Symposium on EMC,* Jan. 2006.

3.2.3 Impulse-Response/Green's Function Method for Modeling EM Coupling on Integrated Circuits.

We developed a methodology for investigating the response of a complex on-chip interconnect network to external electromagnetic interference or internal noise, modeled by randomly distributed signals induced on the network. Our 3D solver uses the network's impulse responses to characterize the full time and space varying outputs of this system. While we have developed fullwave electromagnetic solutions to model on-chip interconnect networks [1], these are computationally intensive for such structures on a semiconducting substrate. For a problem like determining which points on a chip are particularly vulnerable to EM coupling, being able to

quickly repeat a simulation for many input distributions is advantageous. Our method provides this ability without having to solve for the entire system repeatedly, saving storage and operation counts.

METHODOLOGY

We model on-chip interconnect networks as spatially dependent lumped impedance element networks comprised of unit cells, following a similar approach to our previous work[2]. Since we are dealing largely with the interconnect network, and not transport in the semiconductor, the network is taken to be linear. We then characterize the network using an impulse response-Green's function method[3]. This is achieved by providing a unit signal input at each node of the lumped network. We then solve for the input response in time and space for each input. This provides a total description for the linear system. Once the system is characterized, we can predict its response to an arbitrary input. We achieve this by performing a numerical convolution between the input and the input response-Green's function. This method is especially useful for EM coupling since the input is often random. Therefore, once the system is characterized through the input response, its behavior can be predicted for random EM inputs. Repeating the process for different random input distributions does not require solving for the impulse responses again.

Computational Advantages

This method has several main computational advantages. First, we need to use fullwave solutions only to obtain equivalent circuits for small unit cells. Second, for selected network points of interest (e.g. a particular transistor gate), we only need the impulse responses at these points to have been calculated and stored to get the response to a general input. Especially when exploring effects of random interference, this method has speed and storage advantages over full lumped network solutions.

Repeating the calculation for random inputs does not require solving the entire network again, whereas the standard circuit simulator SPICE needs to solve the entire network matrix equation at each time-step.

IMPLEMENTATION

Our solver allows convenient construction of large interconnect networks from unit cells. The program has two independent modules: Impulse response solver and input signal response calculator. The former sets up and solves KCL equations for our mesh. The latter performs the numerical integration for the convolution.

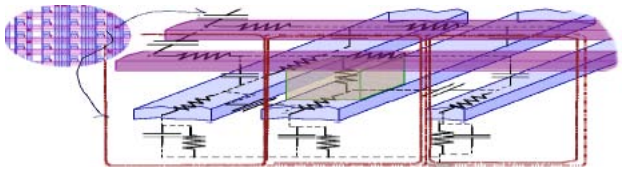


Fig. 1. Two metal network; a simplified equivalent RC network shown. Possible unit cells partitioned.

Unit Cells and the Lumped Element Network

Possible metal segment combinations in a small area define our unit cells. Various equivalent circuit models for coupled interconnect segments have been proposed. They can be derived by parameter extraction from fullwave simulations or S-parameter measurements. Figure 1 shows some possible unit cell definitions in a two-metal technology. Combining unit cells with ground connections and on-chip device loads according to the layout, we obtain a full lumped--element network. We can also define unit cells describing the interaction between stacked (3D) chips' interconnect layers.

Sample Results

We have compared both impulse response and full input response solutions with SPICE results for a 5x5x3 mesh (N =75), in which each node is connected with an R//C to its six nearest neighbors, with bottom layer nodes down-connected to ground and top layer nodes with no up--connections. Fig. 2 demonstrates the agreement between the SPICE results and our solver. For this mesh, SPICE requires 0.24 msec per time-step, while our input response solver takes 0.0124 msec per time-step and output point.

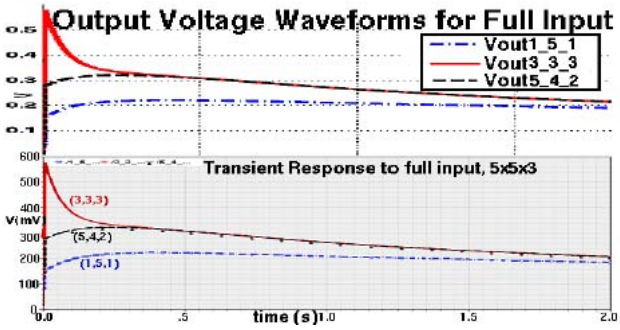


Fig. 2. A 5x5x3 mesh full response simulation. Top: Our solver combines impulse responses at three points using the input data. Bottom: SPICE performs full mesh solution at each timestep for the same input pattern. The solutions match.

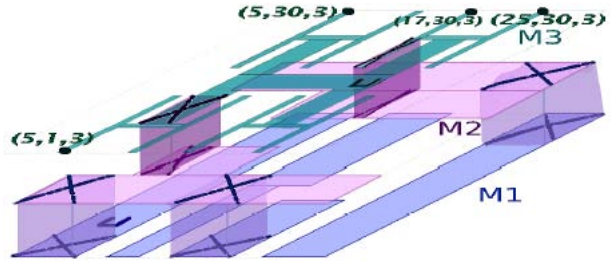


Fig. 3. Three-metal interconnect network. Vias:X. Inputs: .Outputs: •.

Figure 3 shows a more complex 30x30x3 (N =2700) network. The top layer is designed after a typical clock tree. Interlayer, there is resistive coupling due to bias and capacitive coupling at other overlapping areas. Figure 4 shows signals induced by a combination of a ground-level noise spike and a top-level interference pulse at four nodes. Here the top left point (5,30,3) is found to be most sensitive to ground-level pulses and the top right corner points (17,30,3) and (25,30,3) to level 3 noise spikes. The input pulse proximity and the presence of a close resistive path to ground affect output characteristics

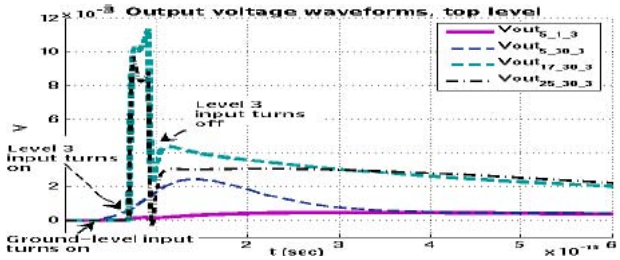


Fig. 4. Responses of the Fig.3 network. A higher signal is induced at (5,30,3) by a groundlevel pulse. Points (17,30,3) and (25,30,3) respond more than the other two to a later pulse injection at level 3. A low overall signal is induced at (5,1,3), with its close path to lower levels.

References

1. X. Shao, N. Goldsman, O. Ramahi, P. Guzdar, *International Conf. on Sim. of Semicond. Proc. and De5. (SISPAD)'03*, pp. 315317.

2. A. Akturk, N. Goldsman, L. Parker, G. Metze, *Solid State Elec*., **49**, pp.11251134, (2005).

3. Z. Dilli, N. Goldsman, A. Akturk, *International Symp. on Semicond. De5. Res. (ISDRS) '05*.

3.3 Design, Fabrication and Testing of On-Chip Microwave Pulse Power Detectors

(Prof. John Melngalis, Dr. John Rodgers;
Students: Todd Firestone, Woochul Jeon)

Building on-chip detectors to measure the microwave power levels in various locations within chips or on various chips within an electronic system is the first step to investigating the vulnerable points in electronic systems and devising protective measures. The most important parameters characterizing microwave pulse detectors in circuits are the pulse response time, operating frequency, and sensitivity. Because Schottky diodes have the fastest response time to a pulse input, Schottky diodes are exclusively used for RF pulse measurements. We have fabricated numerous on-chip Schottky diode RF pulse power detectors by both CMOS processes

and a post-CMOS, focused-ion-beam-based process. Since the standard CMOS process is not specified for the Schottky contact, a modification of a CMOS process was required. As an alternate method, MOSFET diodes with bias circuit can be used for RF power detection for a low frequency range up to 5GHz. And, as a post-CMOS process, the use of FIB for fabricating Schottky diodes at any location of interest on a CMOS-fabricated chip is demonstrated.

CMOS Schottky diode microwave pulse power detectors

In a standard CMOS design, when layouts for contacts to lightly doped substrate, such as N-well or P-well, are drawn, the layout editor automatically generates high impurity diffusion layers at the same locations to prevent Schottky contacts. By modifying the layout file to remove these impurity diffusion layers, Schottky contacts were achieved. Schottky diodes with various contact areas and geometries were fabricated through a 0.35μ 0.5μ 1.5μ CMOS processes and tested. To figure out the relationship between the IV curve and the layout of the contact area and the conduction path, Schottky diodes with various contact areas from 0.6μm x 0.6μm to 50μm x 50μm and different geometries were designed. DC measurements showed that the series resistance of the diode is decided not only by the Schottky contact area but also the geometry of the conduction path. To meet the measured DC voltage IV curve, a SPICE model for a fabricated CMOS Schottky diode was suggested and simulated.

This work has led us into a new project on the design of a charge pump circuit in an RFID chip.

FIB Schottky diode detectors

A post-CMOS process may be used for additional detector fabrication on an existing CMOS chip. FIB milling and ion induced deposition were used as post-fabrication steps to build Schottky diodes in specially designed locations on the CMOS chips fabricated using 0.5μ CMOS process. Reactive Ion Etching (RIE) and chemical etching were used to remove the nitride and oxide layers on a CMOS chip. To make a Schottky contact, platinum was deposited after opening a cut in SiO2 and silicon by FIB ion induced milling. To minimize the pulse response time by minimizing the junction capacitance, we also made undercut triangular bridge shaped Schottky contacts by tilted FIB milling.

MOSFET microwave pulse power detectors

A simple diode connected MOSFET can be used as a rectifier. However, its turn on voltage, usually 1V, is too high for small microwave signal detection and a bias circuit or a dc source is required to improve the sensitivity. By adding a bias circuit, the turn on voltage can be shifted to 05. We have designed a half wave rectifier circuit with 0V turn on voltage and a full wave rectifier circuit.

Measured result

The diode RF power detectors we developed showed various characteristics. CMOS Schottky diodes and FIB Schottky diodes showed a wide dynamic range and a relatively flat

frequency response. However, the output voltage, the frequency response, and the pulse response time strongly depend on the contact area. MOSFET power detectors showed the shortest pulse response time, though their frequency response and dynamic range were worse that that of the Schottky diode power detectors. Figure 1 and Figure 2 shows the measured results for all detectors fabricated and tested. Figure 1 shows the frequency response from 1GHz to 10GHz. Since an RF burst with the frequency range from 1GHz to 5GHz is expected to have the strongest effect on electrical systems, the power detectors were tested up to 10GHz. Figure 2 shows the power sweep from –21dBm to 15dBm. For the better comparison a pn junction diode and a diode connected MOSFET without a bias circuit were also fabricated and tested. Both the diode connected MOSFET and the pn-junction diode showed poor detections in terms of the sensitivity and the frequency response. Table 1 summarized the measured results for all detectors. The pulse response time is the rise time, and it is expressed as the interval between the points of 10% to 90% amplitude of the detected signal. The frequency range of interest in HPM source is from 1GHz to 10GHz and the pulse durations are from 10's to 100ns. The sensitivity in dBm is the input power level to generate 2mV DC output.

Conclusion

CMOS/post-CMOS pulse power detectors were fabricated and compared. Both detectors had relatively flat frequency response up to 15GHz. Large contact area power detectors were the best choice for long and high power pulse detection and small power detectors were good for short and low power pulse detection. FIB Schottky diode achieved 100ns of pulse response time, which is required for HPM pulse detection.

Table 1

	CMOS diode		FIB diode			MOSFET detector		Full wave MOSFET	pn Junction diode
	n-type 92μm2	n-type 1.4μm2	p-type 4μm2	n-type 15μm2	Bridge 1μm2	150kΩ Load	1kΩ Load		
Pulse response time (sec)	820n	776n	192n	6 μ	170n	200n	56n	101n	16μ
Frequency response (Vout at 1GHz / Vout at 10GHz)	4.93	2.05	4.91	3.14	3.97	9.59	4.43	2.44	27.4
Dynamic range (dBm)	> 36	> 34.5	> 16.5	> 25.5	> 26	23	> 25	>25	> 12
Sensitivity (dBm) (smallest possible detection)	-21	-19.5	-1	-20.5	-11	-18	-10	-10	3

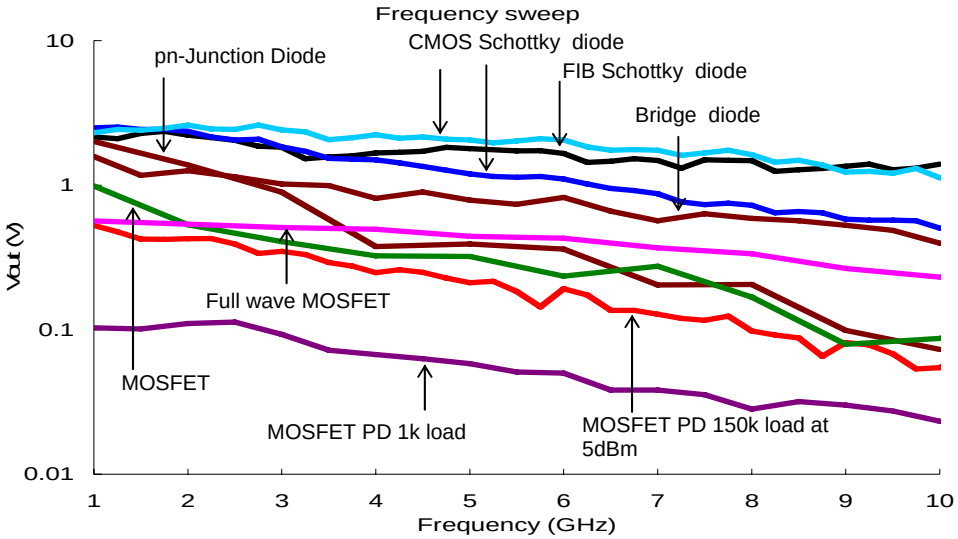


Figure 1 Frequency sweep (1GHz to 10GHz) for fabricated power detectors

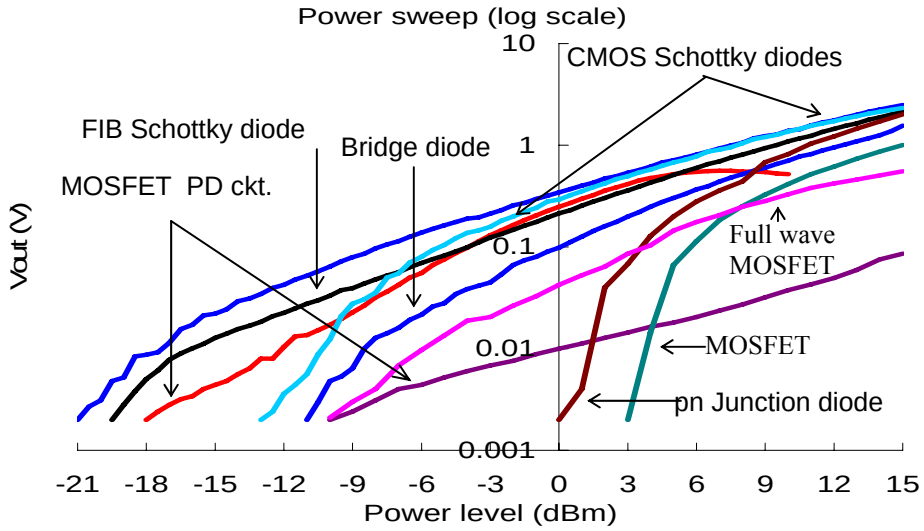


Figure 2 Power sweep (-15dBm to 15dBm) of fabricated power detectors at 1GHz

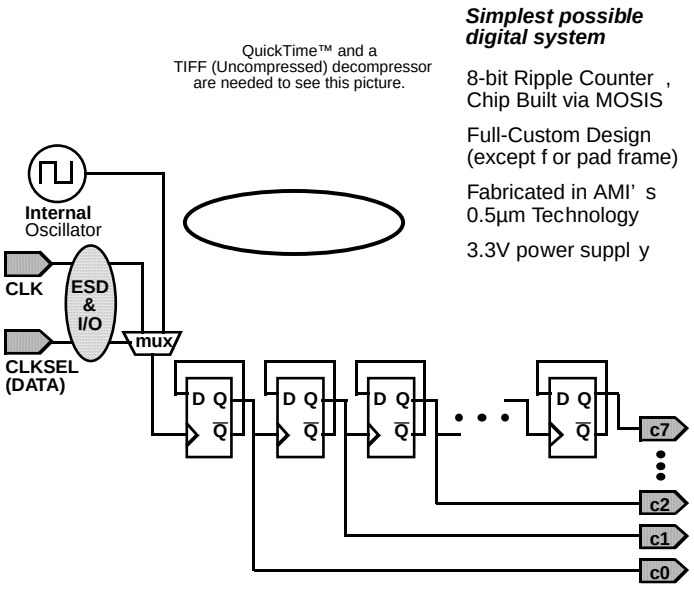
3.4 Studies of Mitigation Techniques

(Prof. Bruce Jacob and Prof. Omar M. Ramahi.
Students: Hongxia Wang, Samuel Rodriguez, Cagdas Dirik, Lin Li, Xin Wu,
Baharak Mohajer-Iravani, Sharooz Shaparia, Mohanmmad Haeri Kermani)

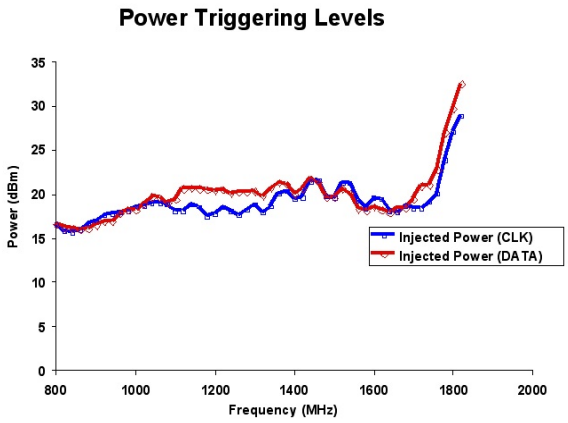
3.4.1 System-Level Vulnerability and Mitigation By Using Robust Architecture

Over the course of the MURI we have investigated three different aspects of the problem of electromagnetic interference and digital systems. We have quantified how easily external signals can enter a typical chip and be interpreted as valid signals; we have quantified how easy it is to perturb the correct functioning of low-leakage SRAMs, the primary circuit used for storing state on a microprocessor; and we have developed and validated a highly robust architecture that enables a microprocessor to survive in the face of even extreme intentional EMI.

The following shows the device under test used to quantify external signals corrupting the input buffers of a chip:

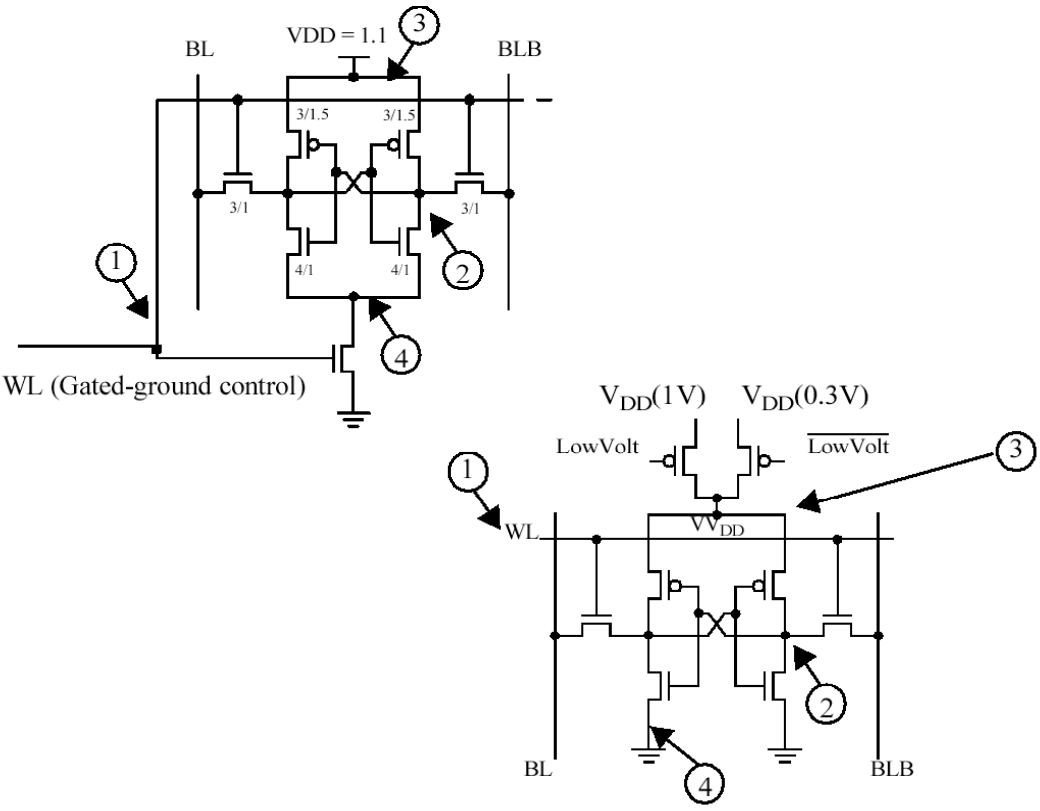


This is a small counter circuit, a series of flip-flops connected to each other. The die photo is the chip that we designed and had manufactured through MOSIS, and the counter circuit is circled. We injected power into both the CLK pin (a clock input) and the CLKSEL pin (a data input). It had been theorized previously that clock inputs would be less easily disrupted than simple data inputs because of the relatively high-capacitance network to which the clock inputs attach (the on-chip clock network tends to be relatively large). The following results demonstrate the similarity of the two inputs:

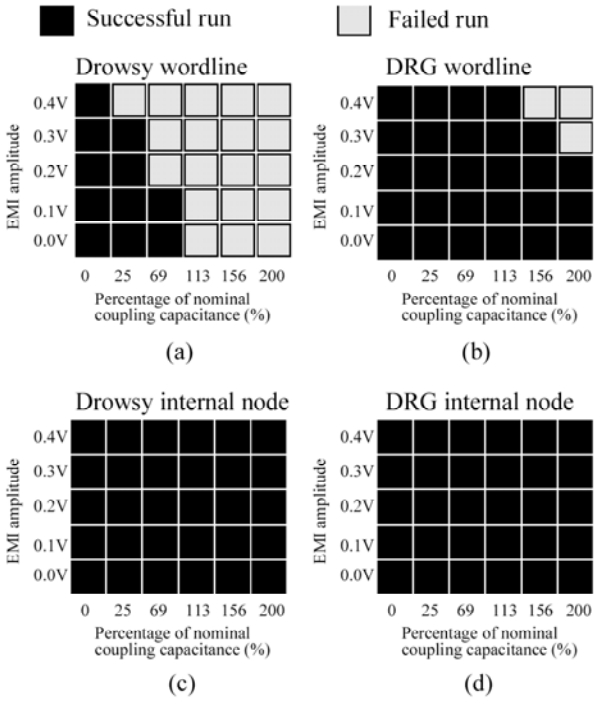


We believe that much of the difference is due to external parasitics on the test board.

Our next series of tests study the leading circuit for on-chip storage: the SRAM. In particular, modern microprocessors are moving to low-leakage SRAM circuits because leakage is the most significant component in power dissipation for cutting-edge circuits, and SRAMs typically represent the largest single component on any microprocessor. We studied two low-leakage circuits: the "Drowsy" SRAM and the data-retentive gated-ground SRAM. The circuits are shown below, with noise-injection sites indicated:



We modeled the circuits in SPICE and injected various types of noise into the injection sites, each corresponding to the appropriate behavior of the circuit. In the simulation, noise is injected into four important internal nodes of a memory cell: (1) the cell's wordline, (2) the cell's internal storage node, (3) the cell's VDD, and (4) the cell's GND, as shown for the DRG cell and drowsy cache cell respectively. The injected noise used in the simulations was a combination of both inherent circuit noise (crosstalk/IR/ground bounce noise) and EMI. IR-drop noise is applied to (1); ground bounce is applied to (2); crosstalk is applied to (3); and induced EMI noise is applied to (4). The following graphs show the results of the study:



These "shmoo" plots denote which combination of EMI and inherent noise coupling result in failure of the memory cell to preserve its internal state. A black square indicates correct functioning of the circuit; a grey square indicates a perturbed circuit. The normal SRAM (not low-leakage) exhibited no failures over the range tested. Among other things, the study shows that low-power SRAM circuits are most susceptible to noise (EMI) through wordline coupling; this is explained by strong differential noise that affects the internal state whenever the wordline has enough strength to turn on the access transistors. For example, when the initial state of an idle or inactive memory cell is "1", and a "0" is being written to a neighboring cell such that the bitline goes low (and the complementary bitline stays high), a voltage difference exists between the internal node and the bitline it is connected to (also true for the complementary side). The access transistors to idle memory cells are ideally turned off to isolate the internal nodes from the bitlines, but any noise present in the wordline will tend to induce currents through the access transistors that produces differential-mode noise across the cross-coupled inverter latch, potentially overwriting it and corrupting its stored state.

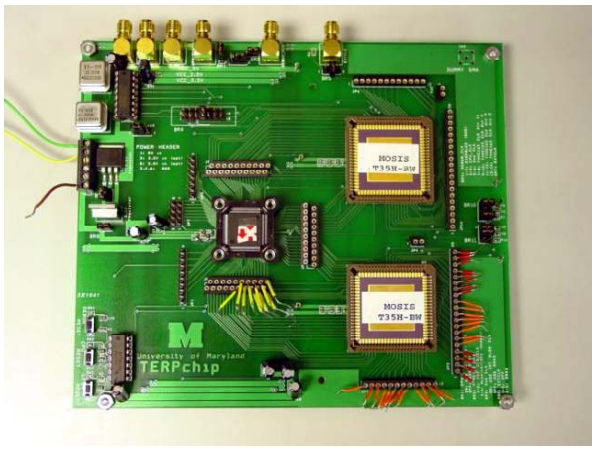
Because MOSFET switching characteristics change with temperature, our future/present work investigates thermal effects.

The results of the previous studies are important: the first study demonstrates that the clock network is as easily upset as data inputs. This is problematic for two reasons: (1) if an error occurs on the clock network, Byzantine failures of the chip result (i.e., the errors are numerous, widespread, and uncorrelated), and (2) while data inputs can be protected via data-integrity measures such as checksums, ECC (error-correcting codes), and other higher-level mechanisms at both the hardware and software levels, the clock network has no such protection measures available to it—the clock is not data and cannot be protected as such.

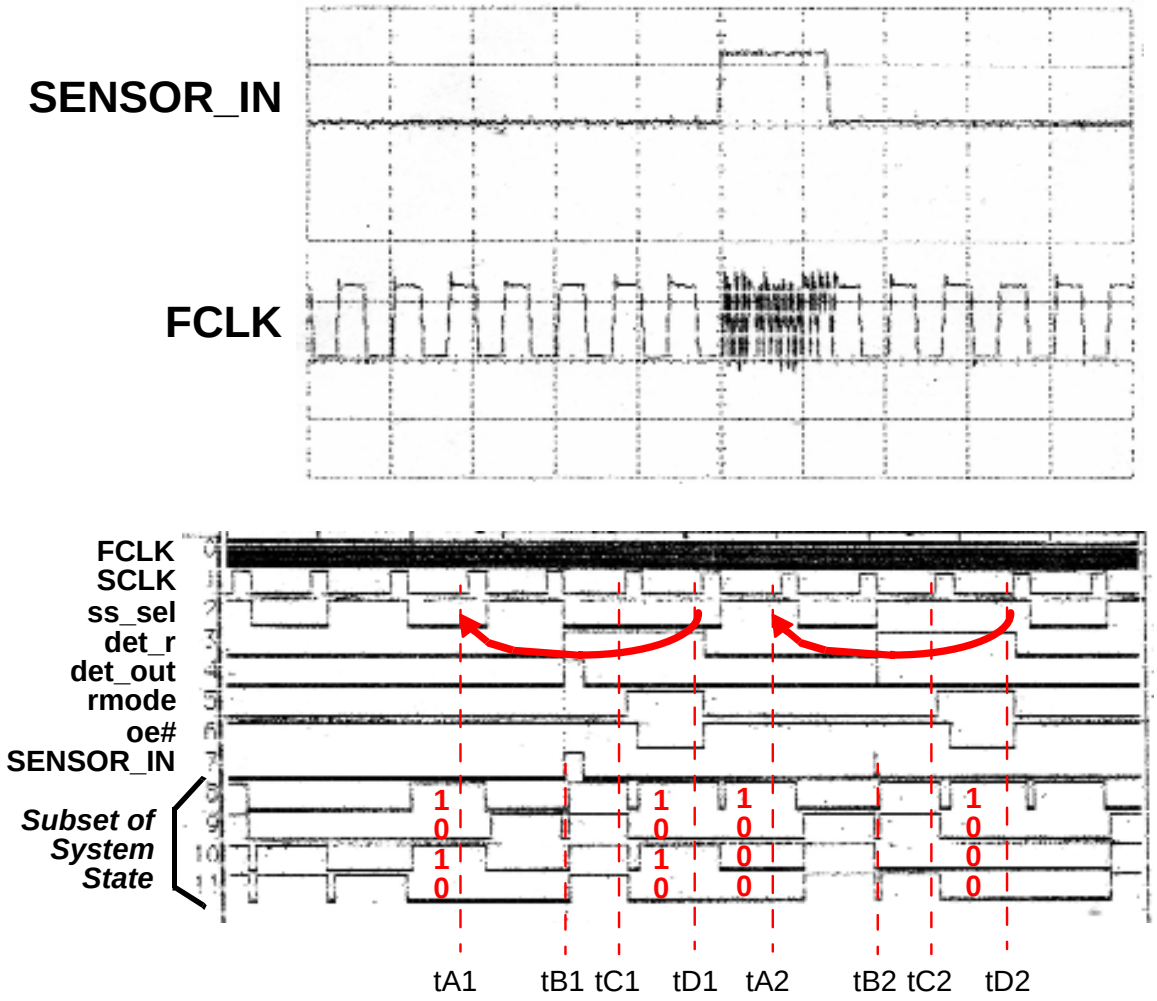
The second study is important because it shows how easily low-leakage SRAMs are perturbed by wordline noise. The main point here is that worldine noise, unlike spurious noise generated by alpha particles (single upset events), will affect every SRAM cell on the same wordline: potentially hundreds of cells, not just one or two cells. Such a large number of potential errors cannot be protected by conventional SRAM-protection means such as ECC. Again, the result is similar to Byzantine failures.

A long-known mechanism for dealing with Byzantine failures is checkpoint/rollback: a scheme in which important state is saved periodically to a known-good location. In the event of an error scenario, the system restores the previously stored state to the computer, thereby "rolling back" to that previous state. Any work performed between the saving of state and rollback is lost, but the work is suspect anyway due to the error scenario, due to which all state of the machine is potentially corrupt.

We developed a novel checkpoint/rollback mechanism that is transparent to software (performed entirely in hardware) and that has a performance overhead that is low enough one can roll back when EMI-upset events are suspected as opposed to detected: this is extremely good news because detecting that an error has occurred is much, much more difficult than detecting the possibility of an error, which only requires detection of significant EMI. Chips were designed by us and fabricated through MOSIS; the following picture shows the test board developed for validation:



The following are screen shots of the logic analyzer used to validate the system:



The top graph shows the superposition of EMI on the CPU's clock input, an event that resulted in the upset of the chip's internal state. The bottom graph shows the response of the system to several such events; in each case, the system successfully rolls back to a previously stored known-good state and continues processing.

3.4.2 Electromagnetic Bandgap Structures for Noise Mitigation

We have pioneered and developed new technology that enables noise mitigation in printed circuit boards and packages. The basic philosophy behind this work is that electromagnetic noise must be transmitted through interconnects and channels in order to cause upset to digital and analogue circuits typically housed in packages. By placing periodic patterns (metallization or inhomogeneous material), frequency bandgaps can be created which will then effectively filter any unwanted electromagnetic energy that falls within this bandgap. The concepts had been tested both numerically and experimentally (see [1-9]). The significance of this approach is that is shifts the chassis shielding efforts, which are typically expensive, difficult

an unpredictable, to a robust technique that eliminates noise propagation at the source, or alternatively (as in the problem of coupling) provides a protection around the target.

The concept of using electromagnetic bandgap (EBG) was applied to three different stages: The chassis, the printed circuit board (PCB) and the package that houses the electronic circuitry.

In the first stage, the chassis, the EBG structure is placed between cavities or openings within the chassis thus effectively attenuating the surface currents that induces the coupling between the source and the victim. In the second and third stage, the PCB and the package, EBG structures are placed within the metal layers [12]. Extensive analysis and design methodologies are reported in. Most recently, we developed planar type EBGs that reduce cost of implementation and add design versatility to complex circuits.

Over the past 18 months, we focused heavily on miniaturization of EBG structures. The primary objective is to reduce the size of the EBG cell to enable insertion in packages and to enable the realization of practical size EBG patches for sub-Giga Hz applications. Using high-k material (er > 100), we were able to show that appreciable miniaturization is possible as summarized in the draft paper [10]. Furthermore, using meander lines as connecting bridges between the EBG patches, both miniaturization and wider frequency bandgaps can be achieved. Upcoming work will focus on experimental realization of such structures.

3.4.3 Development of Alternating-Direction Implicit FDTD (ADI-FDTD) Method

The scientific community has become more dependent on the Finite-Difference Time-Domain (FDTD) method to simulate a wide range of problems form acoustics, electromagnetics to photonics, amongst others. The execution time of a FDTD simulation is inversely proportional to the time-step size. Since the FDTD method is explicit, its time-step size is limited by the well-known Courant-Friedrich-Levy (CFL) stability limit. The CFL stability limit can render the simulation inefficient for very fine structures such as small apertures and transmission lines (small in comparison to the size of the entire structure that is being modeled). The Alternating Direction Implicit FDTD (ADI-FDTD) method has been introduced as an unconditionally stable implicit method. Numerous works have shown that the ADI-FDTD method is stable even when the CFL stability limit is exceeded. Therefore, ADI-FDTD can be considered an efficient method for special classes of problems with very fine structures or high gradient fields.

Whenever the ADI-FDTD method is used to simulate open-region radiation or scattering problems, the implementation of a mesh-truncation scheme or absorbing boundary condition becomes an integral part of the simulation. These truncation techniques represent, in essence, differential operators that are discretized using a distinct differencing scheme which can potentially affect the stability of the scheme used for the interior region. In our work, we showed that the ADI-FDTD method can be rendered unstable when higher-order mesh truncation techniques, such as Higdon's Absorbing Boundary Condition (ABC) or Complementary Derivatives Method (COM), are used. When having large fields gradients within a limited volume, a non-uniform grid can reduce the computational domain and, therefore, decrease the computational cost of finite-difference time-domain method. However, for high-accuracy

problems, different grid sizes increases the truncation error at the boundary of domains having different grid sizes. To address this problem, we have introduced the Complementary Derivatives Method (CDM), a second-order accurate interpolation scheme. The detailed implementation of the CDM method can be found in [11].

3.4.4 Novel Techniques for Reducing EM Coupling into Enclosures and Cavities

Metallic enclosures are commonly used to reduce emission from electronic devices and boards, and to improve the immunity of the same electronic equipment to external interference and threats. In cases where the frequency is high enough such that the skin depth is less than the thickness of the shield, the overall shielding effectiveness will not be determined by the shield material properties but by the apertures in the shield or chassis. These apertures may be introduced intentionally, as would be the case when airflow is needed for cooling, or unintentionally as the inevitable joint seams of shields or small openings in doors with imperfect gaskets. The leakage of electromagnetic waves through apertures in enclosures is critical at frequencies where the wavelength approaches the dimension of the aperture.

In our work, we focused on the problem of radiation through an aperture present in an infinite large conducting plane, thus ignoring any effects induced by the enclosure such as the resonance of the enclosure and complex field interaction with internal structures. This initial focus is intended to develop an understanding for the electric current density distribution in the immediate vicinity of the aperture. To improve shielding effectiveness due to the presence of an aperture in an infinite metallic screen, we introduce a novel technique that is based on the application of resistive sheets (coating) to the area immediately surrounding the aperture. The primary objective in our technique is to lower the radiation through the aperture while maintaining constant aperture size in order not to affect airflow and heat transfer which is a major consideration for enclosures containing high-speed electronics. Numerical validation and experimental verification of our coating technique was demonstrated and fully documented in [12].

3.4.5. Quasi-Analytic Solution for Finding the Eigenvalues in a Class of Chaotic Cavities

As a complementary effort to other MURI researchers, we addressed the problem of bowtie cavity. We constructed the solution to the bowtie cavity problem by realizing that the bowtie cavity can be formed by circles with varying radii. The circles are simultaneously non-intersecting and tangent to each other. Through this realization, it is possible to construct an analytic solution to the field distribution within such cavities and furthermore to obtain the statistical distribution of the Eigenvalues. Using the technique developed [14], it is possible to analytically study a wide-class of cavities and understand the effect of adding inclusions within the cavity on the statistical distribution of the Eigenvalues. The analytical approach introduced in our work is highly advantageous in terms of computation efficiency and robustness in comparison to three-dimensional full-wave Maxwell equations solvers that carry significant computational overhead and code acquisition costs.

References

1. J. Qin and O. M. Ramahi, "Ultra-wideband mitigation of simultaneous switching noise using novel planar electromagnetic bandgap structures," accepted for publication in *IEEE Microwave and Wireless Component Letters.*

2. S. Shahparnia and O. M. Ramahi, "Design, implementation and testing of miniaturized electromagnetic bandgap structures for broadband switching noise mitigation in high-speed PCBs," accepted for publication in *IEEE Transactions on Advanced Packaging*.

3. Mohajer-Iravani, S. Shahparnia and O. M. Ramahi, "Coupling reduction in enclosures and cavities using electromagnetic band gap structures," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 48, No. 2, pp. 292-303, May 2006.

4. T. Kamgaing and O. M. Ramahi, "Design and modeling of high-impedance electromagnetic surfaces for switching noise suppression in power planes," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 47, No. 3, pp. 479-489, Aug. 2005.

5. S. Shahparnia and O. M. Ramahi, "A simple and effective model for electromagnetic bandgap structures embedded in printed circuit boards," *IEEE Microwave and Wireless Components Letters,* Vol. 15, No. 10, pp. 621-623, Oct. 2005.

6. S. Shahparnia and O. M. Ramahi, "Miniaturized Electromagnetic Bandgap Structures for Broadband Switching Noise Suppression in PCBs," *Electronics Letters*, Vol. 41, No. 9, pp. 519-520, April 2005.

7. S. Shahparnia and O. M. Ramahi, "Electromagnetic interference (EMI) reduction from printed circuit boards (PCB) using electromagnetic bandgap structures," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 46, No. 4, pp. 580-587, No5. 2004.

8. S. Shahparnia and O. M. Ramahi, "Simultaneous switching noise mitigation in printed circuit boards using cascaded high-impedance surface," *Electronics Letters*, Vol. 40, No. 2, pp. 98-99, Jan. 2004.

9. T. Kamgaing and O. M. Ramahi, "A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface," *IEEE Microwave and Wireless Components Letters*, Vol. 13, No. 1, pp. 21-23, Jan. 2003.

10. B. Mohajer-Iravani and O. M. Ramahi, "Miniaturized Electromagnetic Bandgap Structures for Switching Noise and EMI Mitigation in Packages," to be submitted to *IEEE Transactions on Advanced Packaging*.

11. M. H. Kermani and O. M. Ramahi, "The complementary derivatives method: A second-order accurate interpolation scheme for non-uniform grid in FDTD simulation," *IEEE Microwave and Wireless Components Letters*, Vol. 16, No. 2, pp. 60-62, Feb. 2006.

12. O. M. Ramahi and L. Li, "Analysis and reduction of electromagnetic field leakage through loaded apertures: A numerical study," *Electromagnetics Journal*, Vol. 25, No. 7-8, pp. 679-693, October-December 2005.

13. L. Li, J. Xie, O. M. Ramahi, M. Pecht, and B. J. Donham, "Airborne operation of portable electronic devices," *IEEE Antennas and Propagation Magazine*, Vol. 44, No. 4, pp. 30-39, Aug 2002.

14. F. Seydou, O. M. Ramahi, and T. SeppÄanen, A Quasi-Analytical Approach for Finding the Helmholtz Eigenvalues in a Class of Chaotic Cavities, to be submitted to *Physical Review E.*

4. PERSONNEL SUPPORTED

4.1 Academic Faculty

Prof. Steven Anlage, Physics
Prof. Thomas M. Antonsen, Jr., Physics and Electrical Engineering
Prof. Neil Goldsman, Electrical Engineering
Prof. Agis Iliadis, Electrical Engineering
Prof. Bruce Jacob, Computer Engineering
Prof. John Melngalis, Electrical Engineering
Prof. Edward Ott, Physics and Electrical Engineering
Prof. Omar Ramahi, Mechanical Engineering
(now affiliated with the University of Waterloo, Waterloo, Ontario, Canada)

4.2 Research Faculty

Dr. Yuval Carmel, Inst. for Research in Electronics & Applied Physics (IREAP)
Dr. John Rodgers, IREAP

4.3 Graduate Students

Vincent Chan
Cagdas Dirik
Todd Firestone (Ph.D. expected 2007)
James Hart (Ph.D. expected 2007)
Sameer Hemmady (graduated, Ph.D.)
Woochul Jeon (graduated, Ph.D.)
Mohammad Haeri Kermani
Kyechong Kim
Lin Li (graduated, Ph.D.)
Baharak Mohajer-Iravani (graduated, M.S.)
Latise Parker
Shahrooz Shaparnia
Xin Wu (graduated, Ph.D.)
Bo Yang
X. (Henry) Zheng (graduated, Ph.D.)
Christopher Bertrand (Ph.D. expected 2008)

5. PUBLICATIONS AND PATENTS

5.1 Refereed Journal Papers During the Reporting Period

1. Sameer Hemmady, Xing Zheng, Edward Ott, Thomas M. Antonsen, and Steven M. Anlage, "Universal Impedance Fluctuations in Wave Chaotic Systems," Phys. Re5. Lett. 94, 014102 (2005).

2. Sameer Hemmady, Xing Zheng, Thomas M. Antonsen, Edward Ott, and Steven M. Anlage, "Universal Statistics of the Scattering Coefficient of Chaotic Microwave Cavities," Phys. Re5. E 71, 056215 (2005).

3. Xing Zheng, Thomas M. Antonsen Jr., and Edward Ott, "Statistics of Impedance and Scattering Matrices in Chaotic Microwave Cavities: Single Channel Case, " Electromagnetics 26, 3 (2006).

4. Xing Zheng, Thomas M. Antonsen Jr., and Edward Ott, "Statistics of Impedance and Scattering Matrices of Chaotic Microwave Cavities with Multiple Ports," Electromagnetics 26, 37 (2006).

5. Xing Zheng, Sameer Hemmady, Thomas M. Antonsen Jr., Steven M. Anlage, and Edward Ott, "Chracterization of Fluctuations of Impedance and Scattering Matrices in Wave Chaotic Scattering," Phys. Re5. E 73, 046208 (2006).

6. Sameer Hemmady, Xing Zheng, Thomas M. Antonsen Jr., Edward Ott and Steven M. Anlage, "Aspects of the Scattering and Impedance Properties of Chaotic Microwave Cavities," Acta Physica Polonica A 109, 65 (2006) pdf nlin.CD/0506025.

7. Sameer Hemmady, James Hart, Xing Zheng, Thomas M. Antonsen Jr., Edward Ott, and Steven M. Anlage, "Experimental Test of Universal Conductance Fluctuations by Means of Wave-Chaotic Microwave Cavities," submitted to Phys. Re5. B (Rapid Communications), June 2006. cond-mat/0606650.

8. W. Jeon, T. Firestone, J. Rodgers, J. Melngailis, "On-chip RF pulse power detector using FIB as a post-CMOS fabrication process", Journal of Electromagnetics, in-press

9. W. Jeon and J. Melngailis, "CMOS and post-CMOS on-chip microwave pulse power detectors", Solid state electronics, Vol. 50, Iss. 6, pp. 951-958, June 2006

10. S. Shahparnia and O. M. Ramahi, "A simple and effective model for electromagnetic bandgap structures embedded in printed circuit boards," IEEE Microwave and Wireless Components Letters, Vol. 15, No. 10, pp. 621-623, Oct. 2005.

11. X. Wu and O. M. Ramahi, "Application of C-COM to the Absorption of Evanescent Waves in Waveguides," IEEE Microwave and Wireless Components Letters, 2005.

12. T. Kamgaing and O. M. Ramahi, "Design and modeling of high-impedance electromagnetic surfaces for switching noise suppression in power planes,"IEEE Transactions on Electromagnetic Compatibility, 2005,

13. J. Qin and O. M. Ramahi, "Ultra-wideband mitigation of simultaneous switching noise using novel planar electromagnetic bandgap structures," accepted for publication in IEEE Microwave and Wireless Component Letters.

14. S. Shahparnia and O. M. Ramahi, "Design, implementation and testing of miniaturized electromagnetic bandgap structures for broadband switching noise mitigation in high-speed PCBs," accepted for publication in IEEE Transactions on Advanced Packaging.

15. Mohajer-Iravani, S. Shahparnia and O. M. Ramahi, "Coupling reduction in enclosures and cavities using electromagnetic band gap structures," IEEE Transactions on Electromagnetic Compatibility, Vol. 48, No. 2, pp. 292-303, May 2006.

16. M. H. Kermani and O. M. Ramahi, "The complementary derivatives method: A second-order accurate interpolation scheme for non-uniform grid in FDTD simulation," IEEE Microwave and Wireless Components Letters, Vol. 16, No. 2, pp. 60-62, Feb. 2006.

17. O. M. Ramahi and L. Li, "Analysis and reduction of electromagnetic field leakage through loaded apertures: A numerical study," Electromagnetics Journal, Vol. 25, No. 7-8, pp. 679-693, October-December 2005.

5.2 Papers Submitted to Refereed Journals

1. Xing Zheng, Sameer Hemmady, Thomas M. Antonsen Jr., Steven M. Anlage, and Edward Ott, "Characterization of Fluctuations of Impedance and Scattering Matrices in Wave Chaotic Scattering," submitted to Phys. Re5. E. cond-mat/0504196.

2. Sameer Hemmady, Xing Zheng, Thomas M. Antonsen Jr., Edward Ott and Steven M. Anlage, "Aspects of the Scattering and Impedance Properties of Chaotic Microwave Cavities," submitted to Acta Physica Polonica A (2006). nlin.CD/0506025.

3. B. Mohajer-Iravani, S. Shahparnia, and O. M. Ramahi, "Coupling Reduction in Enclosures and Cavities using Electromagnetic Band Gap Structures", submitted to IEEE Transaction in Electromagnetic Compatibility. Revised Sept. 2005.

4. T.M. Firestone, J. Rodgers and 5.L. Granatstein, "Investigation of the Radio Frequency Characteristics of CMOS Electrostatic Discharge Protection Devices", Submitted to IEEE Trans. on Circuits and Systems.

5. K. Kim, A. A. Iliadis, 5. Granatstein, "Operational Degradation and Bit-Flip Errors in CMOS Inverters due to Microwave Interference", IEEE Trans EMC, submitted (July, 2005)

6. W. Jeon, T. Firestone, J. Rodgers, J. Melngailis, “CMOS/Post-CMOS fabrication of on-chip Schottky diode microwave pulse power detectors”, Journal of Directed Energy, under review

7. K. Kim and A. A. Iliadis, “Impact of Microwave Interference on Dynamic Operation and Power Dissipation of CMOS Inverters”, Submitted IEEE Trans. EMC, May 2006.

8. F. Seydou, O. M. Ramahi, and T. SeppÄanen, A Quasi-Analytical Approach for Finding the Helmholtz Eigenvalues in a Class of Chaotic Cavities, to be submitted to Physical Review E.

9. T.M. Firestone, J. Rodgers and 5.L. Granatstein, “Response of CMOS Logic with Electrostatic Discharge Protection to Pulsed Microwave Excitation Submitted to IEEE Trans. on Circuits and Systems.

10. S. Hemmady, X. Zheng, T.M. Antonsen, E. Ott, and S.M. Anlage, “Universal Properties of 2-port Scattering, Impedance and Admittance Matrices of Wave Chaotic Systems,” submitted to Phys. Re5. E.

11. Sameer Hemmady, James Hart, Xing Zheng, Thomas M. Antonsen Jr., Edward Ott, and Steven M. Anlage, “Experimental Test of Universal Conductance Fluctuations by Means of Wave-Chaotic Microwave Cavities,” submitted to Phys. Re5. B (Rapid Communications), June 2006. cond-mat/0606650.

5.3 Papers Published in Conference Proceedings

1. W. Jeon and J. Melngailis, “CMOS&post CMOS on-chip microwave pulse power detectors” Proc., 2005 ISDRS, Washington DC, Dec. 2005

2. W. Jeon, J. Melngailis, and R. W. Newcomb, “CMOS Schottky diode microwave power detector fabrication, Spice modeling, and application”, IEEE Intl. Work. Electronic Design, Test, & Applications (DELTA 2006), pp 17-22, Kuala Lumpur, Malaysia, Jan. 2006

3. W. Jeon and J. Melngailis, “On-chip CMOS microwave pulse power detectors”, 2006 IEEE Power Modulator Conference abstracts, pp 64-65, Washington DC, May 2006

4. W. Jeon, J. Melngailis, and R.W. Newcomb, “Disposable CMOS passive RFID transponder for patient monitoring”, IEEE ISCAS, pp 5071-5074, Island of Kos, Greece, May 2006

5. W. Jeon, J. Melngailis, and R. W. Newcomb, “CMOS Schottky diode microwave power detector fabrication, Spice modeling, and application”, IEEE Intl. Work. Electronic Design, Test, & Applications (DELTA 2006), pp 17-22, Kuala Lumpur, Malaysia, Jan. 2006

6. O. M. Ramahi, and S. Shahparnia "Miniaturized Electromagnetic Bandgap Structures for Noise Suppression," in proceedings, the 9th International Conference on Electromagnetics in Advanced Applications (ICEAA '05) and the 11th European Electromagnetic Structures Conference (EESC'05), Turin, Italy, pp. 379-381, Sept. 12-16, 2005. (invited paper)

7. K. Kim, A. A. Iliadis, "Degradation of Characteristics and Critical Bit-Flip Errors in Cascaded 3-Stage CMOS Inverters due to RF Interference", Proc. 2005 International Semiconductor Device Research Symposium, Washington D. C., pp 5-6 Dec. 2005.

8. Y. Bayram, K. Kim, P. C. Chang, J. L. Volakis, A. A. Iliadis, "High Power EMI on Digital Circuits within Automotive Structures", 2006 IEEE International Symposium on EMC, Jan. 2006.

5.4 Talks

1. Steven Anlage, "Chaos in Electromagnetism and Quantum Mechanics," Physics Colloquium, University of Erlangen-Nürnberg, Germany, 29 May, 2006, 60 minutes.

2. Steven Anlage, "Experimental Investigation of Universal Fluctuations in Quantum/Wave Chaotic Scattering Systems," NIST Quantum Information Bose Einstein Condensation (QIBEC) seminar, Gaithersburg, MD, 11 January, 2006, 60 minutes.

3. Steven Anlage, "Universal Scattering Properties of 2-Port Wave Chaotic Systems," invited talk, Centro Internacional de Ciencias Gathering on Chaotic and Random Wave Scattering in Quantum Mechanics and Acoustics, Cuernavaca, Mexico, 4 October, 2005. 2.25 hours.

4. Sameer Hemmady, "Universal Fluctuations in Scattering, Impedance and Admittance Matrices of Quantum Chaotic Systems"- Presented at the Annual March meeting of the American Physical Society, Baltimore MD. (2006). Invited Talk (12 mins). Awarded the Graduate Student Speaker Award by the Group on Statistical and Non-linear Physics (GSNP).

5. Sameer Hemmady, "Exploring Mesoscopic Fluctuations through Universal Scattering Fluctuations in Chaotic Microwave Cavities."- Presented at the Annual March meeting of the American Physical Society, Baltimore MD. (2006). Contributed Talk (12 mins).

6. Sameer Hemmady, " The Random Coupling Model – a priori prediction of field distributions inside complicated enclosures"- Presented at the Institute for Infrastructure Surety (IFIS) workshop on High-Power Microwave (HPM) weapons attack, Un4. of New Mexico, Albuquerque, NM.(2005). Invited Talk (35 mins).

7. W. Jeon, J. Melngailis, "CMOS passive RFID transponder with read-only memory for low cost fabrication," IEEE SOCC 2005, Washington, DC, September 2005.

8. W. Jeon, J. Melngailis, and R. W. Newcomb, “CMOS Schottky diode microwave power detector fabrication, Spice modeling, and application”, IEEE Intl. Work. Electronic Design, Test, & Applications (DELTA 2006), pp 17-22, Kuala Lumpur, Malaysia, Jan. 2006

9. W. Jeon, J. Melngailis, "CMOS passive RFID transponder with read-only memory for low cost fabrication", IEEE SOCC 2005, Washingtond DC, September 2005

10. M. Moskowitz and W. Jeon, “Design of Portable integrated Diode-Based Biosensor for diabetic diagnoses”, World Congress on Medical physics and Biomedical engineering, Seoul, Aug. 2006.

11. W. Jeon and J. Melngailis, “CMOS Schottky diode for photo-detector and thermal detector applications”, IEEE sensors, Oct 2006.

5.5 Patents

1. A. A. Iliadis “Sense and Protect Circuit”: US Patent #6,968,157.

6 Interactions / Transitions

Outreach activities:

Substantial interactions on wave chaos group with the ONERA group in Toulouse, France. Collaboration with this group is planned.

Collaboration was established between the research group led by Professor A. Iliadis at the University of Maryland and the research group led by Professor J.L.Volakis at Ohio State University.

The Random Coupling Model code for calculating the PDF of microwave field strength on electronic components inside enclosures. Has been transferred to a number of DOD laboratories and DOD contractors.

7 Honors /Awards

Sameer Hemmady won the “GSNP Student Speaker Award” for his wave chaos presentation at the March 2006 meeting of the American Physical Society.

APPENDIX

Boise State University MURI Update: (September 1, 2005- July 31, 2006)

Concise summary of research highlights over the 5 year span of the MURI 2001 program

Focus of MURI Research

One of the primary areas in the MURI '01 proposal was to characterize, evaluate, model and simulate degradation and operational errors in devices and circuit building blocks (see section A.4.). We have focused all of our MURI-based research in this. In particular, for ultrathin gate dielectrics in devices and circuits, we sought to answer the question, "When devices in a circuit experience specific degradation that can be induced by electromagnetic coupling (EMC), how will: 1) the devices respond, and 2) the circuit respond?" Hence, our area of focus was gate dielectric/oxide (SiO2) degradation by EM and EM-like radiation in metal-oxide-semiconductor field effect transistors (MOSFETs) and effects on ICs. Below is a concise list summarizing our accomplishments:

- Determined degradation mechanisms in gate oxide dielectric of MOSFETs due to EM radiation of various thickness (tox):
  - nm
  - 2nm
- Mimicked EM radiation-induced degradation in gate oxides using DC techniques for all gate oxide thicknesses
- Determined how gate oxide degradation mechanisms affect simple integrated circuit building blocks (SICBBs) including:
  - Inverters
  - Transmission gates
  - Logic gates:
  - NAND
  - NOR

To do this, we developed two test and measurement techniques

- Multi-Waveform Pulse Voltage Stressing (MWPVS) [1-5]
- Switch Matrix Technique [6-19]

Both of these techniques are highlighted below.

MWPVS technique:[1-5]

Continued size reduction in ICs, leads to:
Very close interconnect proximity
EM radiation will capacitive couple to interconnects
Cause noise spiking from EM pulses
Leads to an increase voltage:
From: Vcarrier
To: Vcarrier + VEM = Vnoise

MWPVS Results:

Pre- and post- MWPVS gate leakage current as a function of gate voltage were examined for gate oxide degradation mechanisms. The degradation mechanisms observed included:

- SILC (Stress Induced Leakage Current)
- SBD and Softer SBD (Soft Breakdown)
- LHBD (Limited Hard Breakdown)
- HBD (Hard Breakdown)

Established a preliminary MOSFET lifetime noise model for MWPVS:

Initial data indicates that increasing the noise signal decreases device lifetime exponentially

$$\frac{1}{t_{bd,noise}} \approx d \cdot e^{c|V|} + d' \cdot e^{c(|V|+|dV|)}$$

where:

$$\Delta t_{bd} = \frac{t_{bd} - t_{bd,noise}}{t_{bd,noise}}$$

$$t_{bd} = T \cdot DC_{BASE} \cdot P_{bd}$$

and:

- tbd, time to breakdown without EM noise
- DCbase, duty cycle of base voltage
- tbd,noise, time to breakdown due to EM noise
- d, constant proportional to DCBASE of carrier signal
- d', constant proportional to DCSPIKE of noise signal
- c, voltage accelerator factor
- dV, noise amplitude
- T, frequency
- Pbd, pulses to breakdown

Conclusions:

Degradation mechanisms induced by either EM-like pulse voltage stressing or constant voltage stressing (CVS), a DC stressing technique.

Device lifetime decreases by over 3 orders of magnitude following MWPVS when compared to lifetime obtained using constant voltage stressing (CVS).

Designed a MWPVS technique to simulate effects of EM radiation on MOSFETs

MWPVS is due to constructive interference - occurs due superposition of waveforms

Electromagnetic radiation

Capacitive Coupling

Mixed Signals

Data corresponds to the noise model: Device lifetime exponentially decreases with increase in noise voltage

Switch Matrix Technique:[6-19]

Motivation:

Reliability studies - focus mainly on MOSFETS and large-scale ICs.
Some studies on inverters and SRAM cells, but do not study time domain nor do or can they directly correlated degradation effects in MOSFETs to gate oxide degradation in ICs

Question:

An IC is a monolithic circuit composed of devices. Thus, how can simple ICs and the devices that form the IC be examined separately?

Answer: We developed a method that can isolate MOSFET from IC to:
examine EM-radiation-like oxide degradation in individual MOSFETs
induce EM-radiation-like oxide degradation in individual MOSFETs or circuit

Method:

Switch Matrix Technique (SMT) enables reliability studies at the simple integrated circuit building block (SICBB) level.
Using SMT, reliability studies have focused on the following SICBBs:
- Inverter (tox: 3.2 and 2 nm)
- Transmission Gate (TG not shown)
- NAND (tox: 2 nm)
- NOR (tox: 2 nm)

Results:
- Limited hard breakdown in both nMOSFET and pMOSFET caused
- Inverter (tox: 3.2) and Transmission Gate
- Both DC and time domain circuit response degraded
- Low level degradation in pMOSFET caused severe degradation in:
  - NAND (tox: 2 nm)
  - NOR (tox: 2 nm)

Conclusions:

Switch Matrix Technique – viable technique
Determine degradation in individual devices
Ability to connect device degradation to circuit degradation
Gate Oxides: 2.0 nm more susceptible than 3.2 nm to EM-radiation-like degradation
SICBB failure may result at a fairly low level degradation
Voltage Transfer Characteristics (VTC) of SICCBs may show negligible inverter degradation
Suggests Oxide degradation effects in SICBBs are not a reliability issue
Decrease in logic gate performance, particularly in time domain, directly related to the change in drive current which is related to the change in channel resistance:

$$\Delta I_{drive} \rightarrow \Delta I_{drive} \propto \frac{1}{\Delta R_{channel}} \rightarrow \Delta t_r \propto \Delta R_{channel}$$

Observed degradation in Δtr of the NOR gate is about half of that observed in NAND gates

Graduate Students

Betsy Cheek (graduated, MS ECE, May 2006)
Thesis: Development and Implementation of the Circuit-Level Oxide Reliability Switch Matrix Technique for Evaluation of CMOS DC and AC Circuit Performance Characteristics
Present Employment: Freescale Semiconductor (formerly Motorola)
Mike Ogas (MS ECE – expected December 2006)
Present Employment: Micron Technology Inc.
Richard Southwick III (MS ECE – expected December 2006, Ph.D. – expected 2009)
Krishna Duvvada (gradiated, MS ECE, 2006)
Present Employment: Micron Technology, Inc.
Bhavana Kollimarla (gradauted, MS ECE, 2005)
Present Employment: Intel, Inc.
Sue Fern Ng (graduated, MS ECE , 2006)
Present Employment: Micron Technology, Inc.

Publications in journals and conference proceedings, patents and talks:

(*: denotes student author)

Journal Articles and Conference Proceedings:

1. Southwick III*, Richard G. and William B. Knowlton, Stacked Dual Oxide MOS Energy Band Diagram Visual Representation Program, IEEE Transactions on Device and Materials Reliability, (2006) - accepted for publication.
2. Duvvada, K., Saxena, 5., and Baker, R. J., (2006) High Speed Digital Input Buffer Circuits, proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), pp. 11-12, April, 2006.
3. T. L. Gorseth*, D. Estrada*, J. Kiepert*, M. L. Ogas*, B. J. Cheek*, P.M. Price, R. J. Baker, G. Bersuker, W.B. Knowlton, Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation, presented at the Workshop on Microelectronic Devices (Boise, Idaho; April 14, 2006)
4. M. L. Ogas*, P. M. Price*, J. Kiepert*, R. J. Baker, G. Bersuker, and W. B. Knowlton, Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, (October 2005) p. 63-66.
5. Ogas* M. L., R. G. Southwick III* B. J. Cheek* R. J. Baker, G. Bersuker, W. B. Knowlton, Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices, in proceedings of the 2004 IEEE International Integrated Reliability Workshop, (Oct. 2004), pp. 32-36.
6. Cheek* Betsy J., Stutzke* Nate, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton, Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, in proceedings of the 2004 IEEE International Reliability Physics Symposium (April, 25-29, 2004) pp. 110-116.

7. Kumar, Santosh, William B. Knowlton, Sridhar Kasichainula and Cesar Payan, SRAM Subthreshold Current Recovery after unipolar AC stressing, in proceedings of the 2004 IEEE International Reliability Physics Symposium (April, 25-29, 2004) pp. 46-48.
8. Stutzke*, N., B.J. Cheek*, S. Kumar, R.J. Baker, A.J. Moll and W.B. Knowlton, Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics, in proceedings 2003 IEEE International Integrated Reliability Workshop, (Oct, 20-23, 2003) pp. 71-79.
9. Payan, C., S. Kumar, A. Thupil, S. Kasichainula and W.B. Knowlton, Leakage Current Recovery in SRAM after AC stressing, in proceedings 2003 IEEE International Integrated Reliability Workshop, (Oct, 20-23, 2003) pp. 67-70.
10. Lawrence*, C.E., B.J. Cheek*, T.E. Lawrence*, Santosh Kumar, A. Haggag, R.J. Baker, and W.B. Knowlton, Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach, in Proceedings of the 15th Biennial IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003, pp.263-266.
11. Kumar, Santosh and William B. Knowlton, Alternate method of TDDB study for aluminum oxide using magneto-resistance. in IEEE International Integrated Reliability Workshop, (2002) pp. 180-183.
12. Knowlton, W.B., T. Caldwell*, J.J. Gomez*, and S. Kumar. On the nature of ultrathin gate oxide degradation during pulse stressing of nMOSCAPs in accumulation. in IEEE International Integrated Reliability Workshop, (2001) pp. 87-88.
13. Patents and Talks:
14. Butler, D.L, and R.J. Baker, (2005) Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes, 2005 Midwest Symposium on Circuits and Systems.
15. Richard Southwick III*, Michael Ogas* and William B. Knowlton, Interactive dual oxide MOS energy band diagram program, poster presentation at the 2005 IEEE International Integrated Reliability Workshop, (October 2005).
16. Richard G. Southwick III*, Vaughn Johnson*, Joe Lindsey*, Tim Lawrence*, Jim Jozwiak, Amy Moll, William B. Knowlton, Through Wafer Interconnects: Preliminary Investigation Of Plasma Induced Damage In pMOSFETs By BOSCH DRIE, poster presentation at 2004 IEEE International Integrated Reliability Workshop, (Oct. 2004).
17. Ogas*, Michael, Richard Southwick III*, Betsy Cheek*, Carrie Lawrence*, BSU, Santosh Kumar, Amr Haggag, Jacob Baker, and William Knowlton, Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra Thin Oxides, poster presentation at Workshop on Microelectronics and Electron Devices, (Boise, Idaho, April 16, 2004).
18. Ogas, Michael*, Dorian Kiri*, Ouahid Salhi*, Richard Southwick III*, Betsy Cheek*, William B. Knowlton, Investigation of Ultra Thin Gate Oxide Reliability in MOS Devices and Simple ICs, poster presentation at Workshop on Microelectronics and Electron Devices, (Boise, Idaho, April 16, 2004) and at 2004 IEEE International Integrated Reliability Workshop, (Oct. 2004).
19. Ogas*, M. L., R. G. Southwick III, B. J. Cheek*, C. E. Lawrence*, S. Kumar, A. Haggag, R. J. Baker, W. B. Knowlton, Investigation of Multiple waveform pulse voltage stress (MWPVS) technique in ultrathin oxides, poster presentation at the 2003 IEEE International Integrated Reliability Workshop (Oct, 20-23, 2003).

20. Stutzke*, Nate, Betsy J. Cheek*, and William B. Knowlton, Circuit-level stress and gate dielectric degradation in MOSFETs, oral presentation and poster at the 2003 Micron Foundation Summer Technical Conference, Boise, ID (August 8, 2003). [Awarded Best Poster Award]
21. Southwick III, R.G. *, Betsy Cheek* and William B. Knowlton, Charge pumping techniques for MOS devices, oral presentation and poster at the 2003 Micron Foundation Summer Technical Conference, Boise, ID (August 8, 2003).
22. Cheek, Betsy*, Carrie Lawrence*, Tim Lawrence*, Jose Gomez*, Theodora Caldwell*, Dorian Kiri*, Santosh Kumar, Jake Baker, Amy J. Moll and William B. Knowlton, Gate dielectric degradation effects on nMOS devices and simple IC building blocks (SICBBs), extended abstract accepted for poster session at IEEE/EDS Workshop on Microelectronics and Electron Devices, (October 25, 2002).
23. Lawrence*, C., B. Cheek*, T. Caldwell*, T. Lawrence*, D. Kiri*, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at the IEEE International Integrated Reliability Workshop, (October 21-24, 2002).
24. Cheek*, B., C. Lawrence, T. Lawrence*, T. Caldwell*, D. Kiri*, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at the IEEE International Integrated Reliability Workshop, (October 21-24, 2002).
25. Knowlton, William B., Research efforts in materials science related areas at Boise State University, invited talk at Idaho State University-Idaho Accelerator Center Workshop on "Application of Novel X-ray sources to Biological and Materials Science" (September 5 & 6, 2002).
26. Rivera B., Baker R. J., Melngailis J., (2001) "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.

Awards:

Jake Baker:

President's Research and Scholarship Award, Boise State University - 2005

Bill Knowlton:

Nominated – College of Engineering for Professor of the Year (2006)
Nominated - University Foundation Scholars Award for Research and Creative Activity (2006)
Nominated - University Foundation Scholars Award for Service (2006)
Faculty Research Associate – Office of Research Administration (2005-2006)
Nominated - University Foundation Scholars Award for Teaching (2005)

Significant Contacts with Other Organizations:

Cypress Semiconductor
Motorola/Freescale Semiconductor
SEMATECH
Micron Technology

Annual Summary of Results: August 1, 2005 to July 31, 2006

Over the past year, there was a continued emphasis to answer the question, "When devices in a circuit experience specific degradation that can be induced by electromagnetic coupling (EMC), how will: 1) the devices respond, and 2) the circuit respond?" Two simple integrated circuit building blocks (SICBBs) were studied. The NAND gate and the NOR gate with the latter being a preliminary study. One of the goals of the MURI proposal was to study future device technologies. Hence, a preliminary study of MOSFETs with high dielectric constant (k) material was initiated. The high K material in this case is HfO2 with an interfacial layer of SiO2 that is approximately 1nm in thickness. In the following separate sections, the results of the NAND and NOR studies will be reviewed followed by the high K MOSFET studies.

NAND Gate Reliability (IRW 2005)[20]

We have studied the effects of dielectric degradation or wearout in a single pMOSFET (fig.1) on NAND gate performance. Our switch matrix technique (SMT) measurements [10, 13, 16] provide conclusive evidence that NAND gate performance is deteriorated in both the DC domain (fig. 2) and particularly in the time-domain (fig. 3). Time-domain measurements show that wearout substantially increases the rise time (tr) of a NAND circuit. Our analysis establishes a direct correlation between the degradation of pMOSFET parameters and the NAND circuit rise time, tr. Consequently, small increases in the channel resistance, RCH, of a single pMOSFET acts to increase the NAND tr and thus limit the speed of the circuit operation. Increases in delay, or decreases in speed, may result in circuit logic errors or bit errors. For instance, data may be expected 500 ps after some event, but arrives 750 ps after the event. The data may be mistaken for not having arrived at all and thus lost. This failure may cause the digital system to request the data again or the circuit to become confused and fail. Therefore, the relevance of tr to digital circuits cannot be understated.

NOR Gate Reliability (WMED 2006)[19]

The preliminary results reported for dielectric degradation or wearout in one pMOSFET of a NOR gate circuit indicate a substantial increase in the rise time (tr) attributed to an increase in channel resistance. The voltage-time (Vt) characteristics for the NOR circuit in configuration 2 are shown in Fig. 4. It was observed that tr of the circuit increases by 27 % ±5 % for configuration 2. Rise time is defined as the time it takes for the output signal to increase from 10% to 90% of the final voltage, as indicated in Fig. 4. This preliminary study suggests that the NOR gate is less sensitive to single pMOSFET wearout than the NAND gate circuit, potentially due to the stacking effect in digital circuits. Future goals include investigation of the stacking effect in digital circuits relative to the wearout regime, as well as examination of correlations between increased tr and variations in threshold voltage.

High K reliability (IRW 2005 & IRW 2006)[21, 22]

In state of the art MOSFETs, the SiO2 thickness is sub-2 nm and is at a fundamental limit because of excessive quantum mechanical tunneling (high leakage current) and the loss of bulk

properties (e.g., decreased band gap). Novel materials are being examined to replace SiO2 such as HfO2. However, HfO2 is thermodynamically unstable resulting in a ~1 nm thick interlayer (IL) of SiO2 between the HfO2 and the Si substrate thereby forming a dual gate oxide stack. The complexity of a dual gate oxide stack relative to energy band diagrams increases with variation in many parameters including, dielectric band offsets, dielectric constants, thicknesses, electric fields, and multiple tunneling mechanisms. Because of these complexities, an energy band diagram program has been developed utilizing basic analytical equations to visualize the energy band diagrams of various dual oxide MOS structures. The program is freely available to the scientific community.1 This program facilitates the creation and exploration of arbitrary stacked dual oxide MOS structures providing students, engineers, and scientists a tool for visualizing energy band diagrams. Energy bands are available for SiO2, HfO2/SiO2, BaTiO3/SiO2, Al2O3/SiO2, and ZrO2/SiO2 MOS stacks to demonstrate the usefulness and range of the program. Using the graphics produced within the program, many applications were presented which include: 1) operation from depletion to strong inversion of a HfO2/SiO2 nMOS device (Fig. 5), 2) direct tunneling (DT) and Fowler-Nordheim tunneling (FNT) mechanisms were easily recognized for BaTiO3/SiO2 (Fig. 6) and ZrO2/SiO2 (Fig. 7) studies, and 3) quantum wells were identified in Al2O3/SiO2 under negative biases (Fig. 8).

The program calculates several parameters (table I). Using the output parameters accessible from the program, trends in the electric field and voltage drop across the interfacial layer present in numerous high-k stacks were investigated. It was shown that the electric field in the interfacial layer is independent of the high-k material and interfacial layer thickness for a constant equivalent oxide thickness (EOT). It was also determined that the electric field, in the interfacial oxide, increases as EOT decreases. In addition, various stress conditions observed in high-k gate stack interfacial layers were plotted as a function of EOT and gate voltage. Electron transport mechanisms as a function of interfacial and high-k thickness and interfacial oxide electric field in the form of transport maps were investigated and the transport mechanisms for various published high-k reliability studies were determined. Through these numerous applications, the program has proven to be a useful tool in exploring the energy band diagrams of stacked dual oxide MOS structures and several reliability scenarios.

TABLE I: PARAMETERS EXTRACTED BY THE PROGRAM

voltage drop across oxide stack	FNT distance
voltage drop across 1st dielectric	EOT
voltage drop across 2nd dielectric	maximum space charge width
electric field across oxide stack	threshold hold voltage
electric field across 1st dielectric	flatband voltage
electric field across 2nd dielectric	metal semiconductor work function difference
capacitance of oxide stack	surface potential
capacitance of 1st dielectric	gate charge
capacitance of 2nd dielectric	

[1] Download program at: http://coen.boisestate.edu/bknowlton/Research/dualBandDiagramProgram.htm

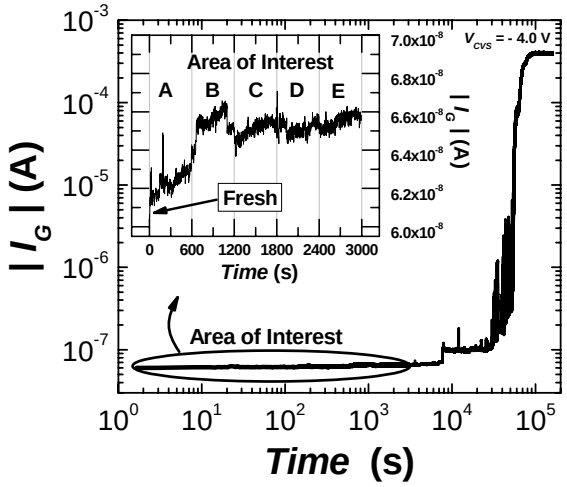


Fig. 1. CVS technique showing gate current versus time of a pMOSFET with stress voltage, VCVS = -4.0 5. Wearout is in the low-leakage regime encircled and marked by the Area of Interest, isolated from the later breakdown events. The pMOSFETs used in this study were not stressed beyond the Area of Interest. An expanded view of the Area of Interest shown in the inset defines the five 600s stress periods A through E, in which the CVS measurement was stopped and circuit and device characteristics were obtained.

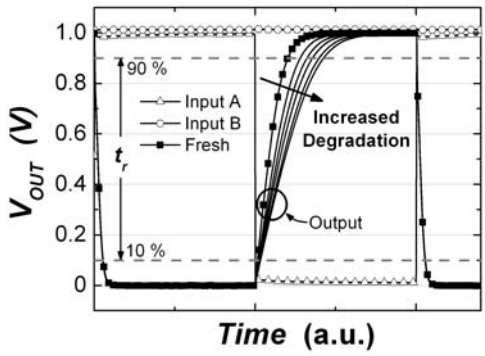
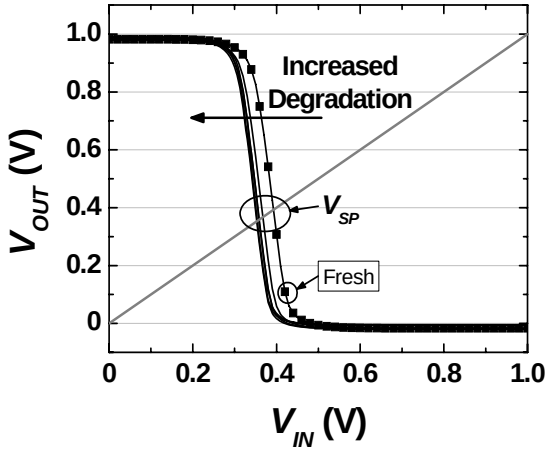


Fig. 2. Voltage time-domain (V-t) results for the NAND circuit using the SMT method. Wearout in one pMOSFET significantly affects the rise time (tr) as shown from Fresh to degradation E.



a.

Fig. 3. Voltage transfer characteristics (VTC) results for the NAND circuit using the SMT method. Wearout in one pMOSFET is shown. A shift to the left in the voltage switching point (VSP) is observed from Fresh to degradation E. VSP is defined as the switching point voltage when VOUT = VIN. intersects the data.

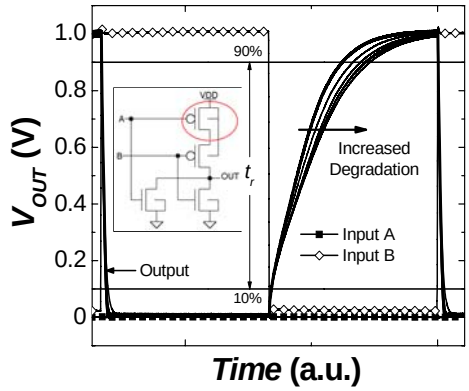


Fig. 4. NOR Voltage-Time measurement with Input A held at ground and Input B swept from 0V to 1V (configuration 2). Inset: NOR circuit with degraded pMOSFET circled.

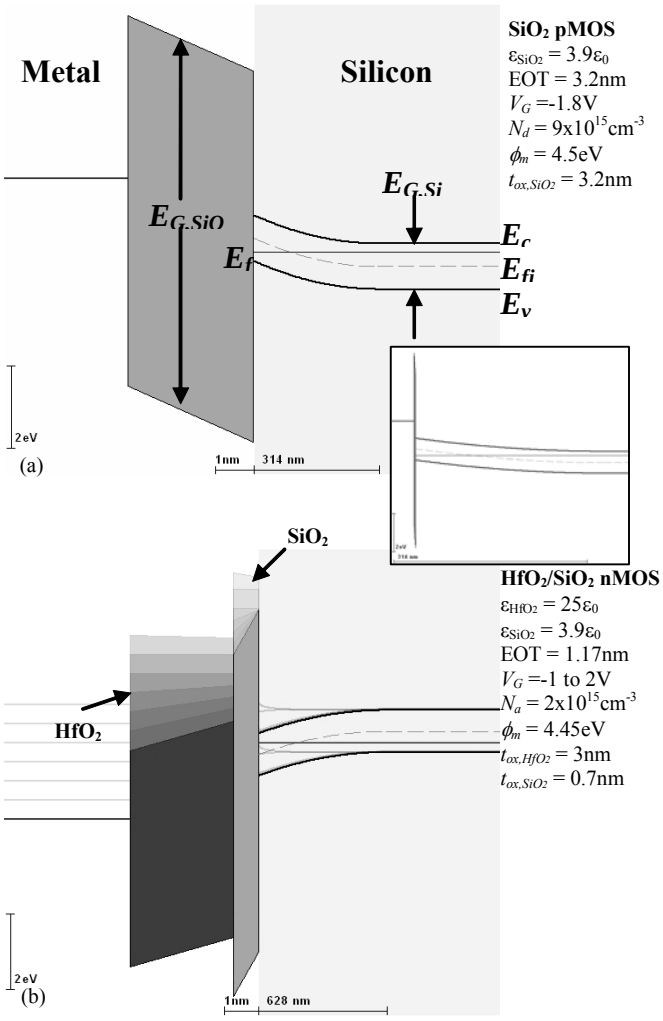


Fig. 5. Part (a) shows a simple SiO2 pMOS energy band structure bias in strong inversion. Inset shows the same band diagram drawn on the same distance scale. Part (b) depicts a more complex HfO2/SiO2 nMOS energy band structure swept from accumulation to strong inversion.

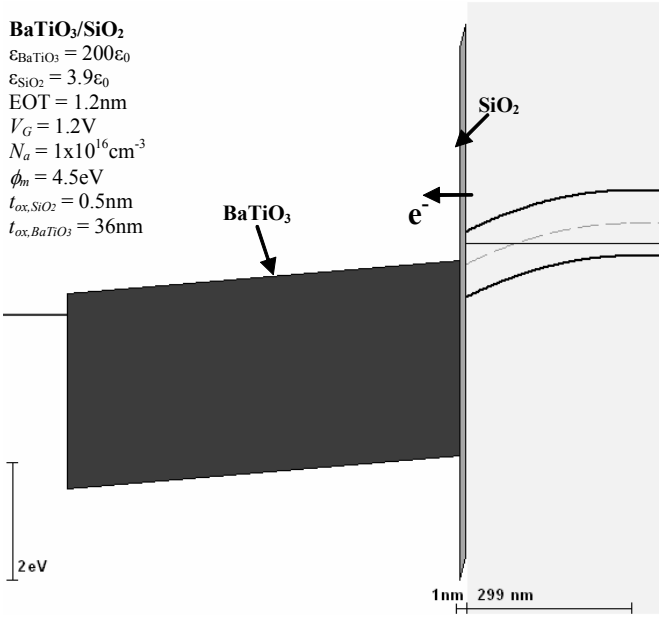


Fig. 6. Energy band diagram for an nMOS containing BaTiO3 with a SiO2 interfacial layer. Shows DT through the SiO2 into the conduction band of BaTiO3.

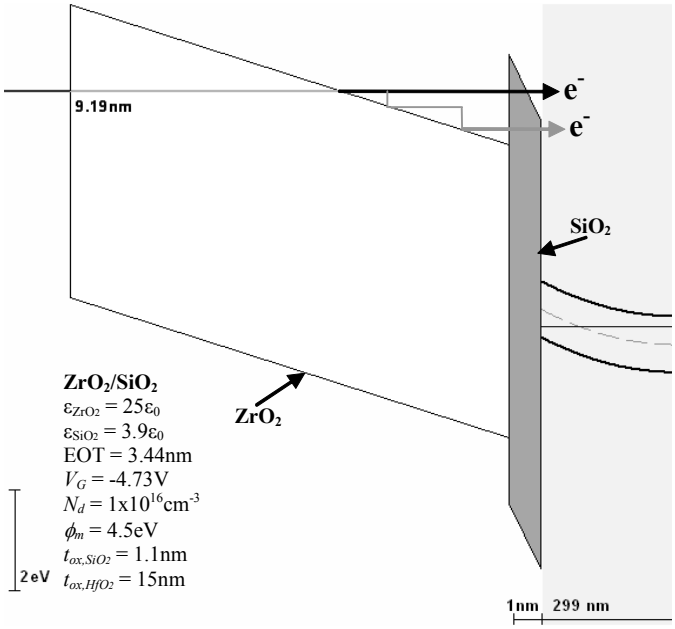


Fig. 7. Band diagram for ZrO2/SiO2 biased under the same electric field conditions as Fig. 4. FNT is seen through the ZrO2 oxide while both FNT and DT are shown in the SiO2 oxide. The calculated FNT distance is also shown for an electron tunneling through the ZrO2 to be 9.19nm.

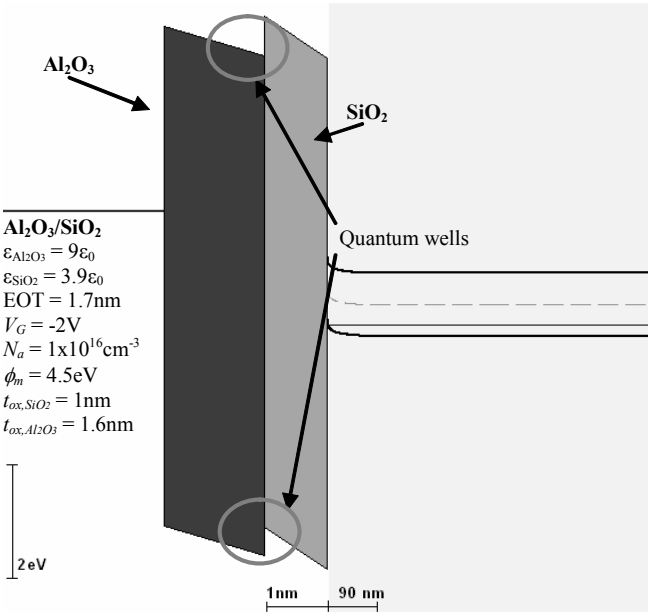


Fig. 8. Energy band diagram for an nMOS with an Al2O3 with a SiO2 interfacial layer. Quantum wells can be seen in both the conduction and valence oxide bands.

References:

[1] W. B. Knowlton, T. Caldwell*, J. J. Gomez*, S. Kumar, and B. Cheek, "On the nature of ultrathin gate oxide degradation during pulse stressing of nMOSCAPs in accumulation," in the proceedings of the IEEE International Integrated Reliability Workshop, pp. 87-88, 2001.

[2] C. Lawrence*, B. Cheek*, T. Caldwell*, T. Lawrence*, D. Kiri*, S. Kumar, J. Baker, A. J. Moll, and W. B. Knowlton, "Pulse voltage stressing of ultrathin gate oxides in NMOS devices," poster presentation at IEEE International Integrated Reliability Workshop, Fallen Leaf Lake, CA, (O. 21-24, 2002).

[3] C. E. Lawrence*, B. J. Cheek*, T. E. Lawrence*, S. Kumar, A. Haggag, R. J. Baker, and W. B. Knowlton, "Gate dielectric degradation effects on nMOS devices using a noise model approach," in the proceedings of the IEEE University Government Industry Microelectronics Symposium, pp. 263-266, 2003.

[4] M. L. Ogas*, R. G. Southwick III*, B. J. Cheek*, C. E. Lawrence*, S. Kumar, A. Haggag, R. J. Baker, and W. B. Knowlton, "Investigation of multiple waveform pulse voltage stress (MWPVS) technique in ultra-thin oxides," poster presentation at 2003 IEEE International Integrated Reliability Workshop, (O. 20-23, 2003).

[5] M. Ogas*, R. Southwick III*, B. Cheek*, C. Lawrence*, S. Kumar, A. Haggag, J. Baker, and W. Knowlton, "Multiple waveform pulse voltage stress technique for modeling noise in ultrathin oxides," poster presentation at IEEE International Integrated Reliability Workshop, (O. 18-21, 2004).

[6] B. Cheek*, C. Lawrence*, T. Lawrence*, T. Caldwell*, D. Kiri*, S. Kumar, J. Baker, A. J. Moll, and W. B. Knowlton, "Circuit level reliability of ultrathin gate oxide for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an

inverter," poster presentation at IEEE International Integrated Reliability Workshop, (O. 21-24, 2002).

[7] B. Cheek*, C. Lawrence*, T. Lawrence*, J. J. Gomez*, T. Caldwell*, D. Kiri*, S. Kumar, J. Baker, and A. J. Moll, "Gate dielectric degradation effects on nMOS devices and simple IC building blocks (SICBBs)," poster presentation at IEEE/EDS Workshop on Microelectronis and Electron Devices, (O. 25, 2002).

[8] C. Payan, S. Kumar, A. Thupil, S. Kasichainula, and W. B. Knowlton, "Leakage current recovery in SRAM after AC stressing," in the proceedings of the IEEE International Integrated Reliability Workshop, pp. 67-70, 2003.

[9] R. G. Southwick III*, B. Cheek*, and W. B. Knowlton, "Charge Pumping Techniques for MOS Devices," poster presentation at Micron Foundation Summer Technical Conference, (A. 8, 2003).

[10] N. Stutzke*, B. J. Cheek*, S. Kumar, R. J. Baker, A. J. Moll, and W. B. Knowlton, "Effects of circuit-level stress on inverter performance and MOSFET characteristics," in the proceedings of the IEEE International Integrated Reliability Workshop, pp. 71-79, 2003.

[11] N. Stuzke*, B. Cheek*, and W. B. Knowlton, "Circuit-Level Stress and Gate Dielectric Degradation in MOSFETs," poster presentation at Micron Foundation Summer Technical Conference, (A. 8, 2003).

[12] B. J. Cheek*, R. G. Southwick III*, M. L. Ogas*, P. E. Nagler*, D. Whelchel*, S. Kumar, R. J. Baker, and W. B. Knowlton, "Preliminary soft breakdown (SBD) effects In CMOS building block circuits," poster presentation at IEEE International Integrated Reliability Workshop, (O. 18-21, 2004).

[13] B. J. Cheek*, N. Stutzke*, S. Kumar, R. J. Baker, A. J. Moll, and W. B. Knowlton, "Investigation of circuit-level oxide degradation and its effect on CMOS inverter operation and MOSFET characteristics," in the proceedings of the IEEE International Reliability Physics Symposium, pp. 110-116, 2004.

[14] S. Kumar, W. B. Knowlton, S. Kasichainula, and C. Payan, "SRAM subthreshold current recovery after unipolar AC stressing," in the proceedings of the IEEE International Reliability Physics Symposium, pp. 46-48, 2004.

[15] M. Ogas*, D. Kiri*, O. Salhi*, R. Southwick III*, B. Cheek*, and W. B. Knowlton, "Investigation of ultrathin gate oxide reliability in MOS devices and simple ICs," poster presentation at Workshop on Microelectronics and Electron Devices, (A. 16, 2004).

[16] M. L. Ogas*, R. G. Southwick III*, B. J. Cheek*, G. Bersuker, and W. B. Knowlton, "Survey of oxide degradation in inverter circuits using 2.0 nm MOS devices," in the proceedings of the IEEE International Integrated Reliability Workshop, pp. 32-36, 2004.

[17] B. J. Cheek*, "Development and Implementation of the Circuit-Level Oxide Reliability Switch Matrix Technique for Evaluation of CMOS DC and AC Circuit Performance Characteristics," in Electrical and Computer Engineering, vol. Master of Science, June, Ed. Boise: Boise State University, 2006, pp. 150.

[18] D. Estrada*, M. Ogas, and W. B. Knowlton, "Investigation of the effects of single pMOSFET ultrathin oxide degradation on NOR logic ciruciut operability," poster presentation at IEEE International Integrated Reliability Workshop, Fallen Leaf Lake, CA, (October, 2006).

[19] T. L. Gorseth*, D. Estrada*, J. Kiepert*, M. L. Ogas*, B. J. Cheek*, P. M. Price*, R. J. Baker, G. Bersuker, and W. B. Knowlton, "Preliminary study of NOR digital response to

single pMOSFET dielectric degradation," in the proceedings of the Workshop on Microelectronic Devices pp. 31-32, 2006.

[20] M. L. Ogas*, P. M. Price*, J. Kiepert*, R. J. Baker, G. Bersuker, and W. B. Knowlton, "Degradation of rise time in NAND gates using 2.0 nm gate dielectrics," in the proceedings of the IEEE International Integrated Reliability Workshop, pp. 63-66, 2005.

[21] R. Southwick III*, M. Ogas*, and W. B. Knowlton, "Interactive dual oxide MOS energy band diagram program," poster presentation at IEEE International Integrated Reliability Workshop, Fallen Leaf Lake, CA, (October, 2005).

[22] R. G. Southwick III* and W. B. Knowlton, "Stacked dual oxide MOS energy band diagram visual representation program," IEEE Transactions on Device and Materials Reliability, vol. to be published, 2006.