EM Effects on Semiconductor Devices, Gates and Integrated Circuit Interconnects

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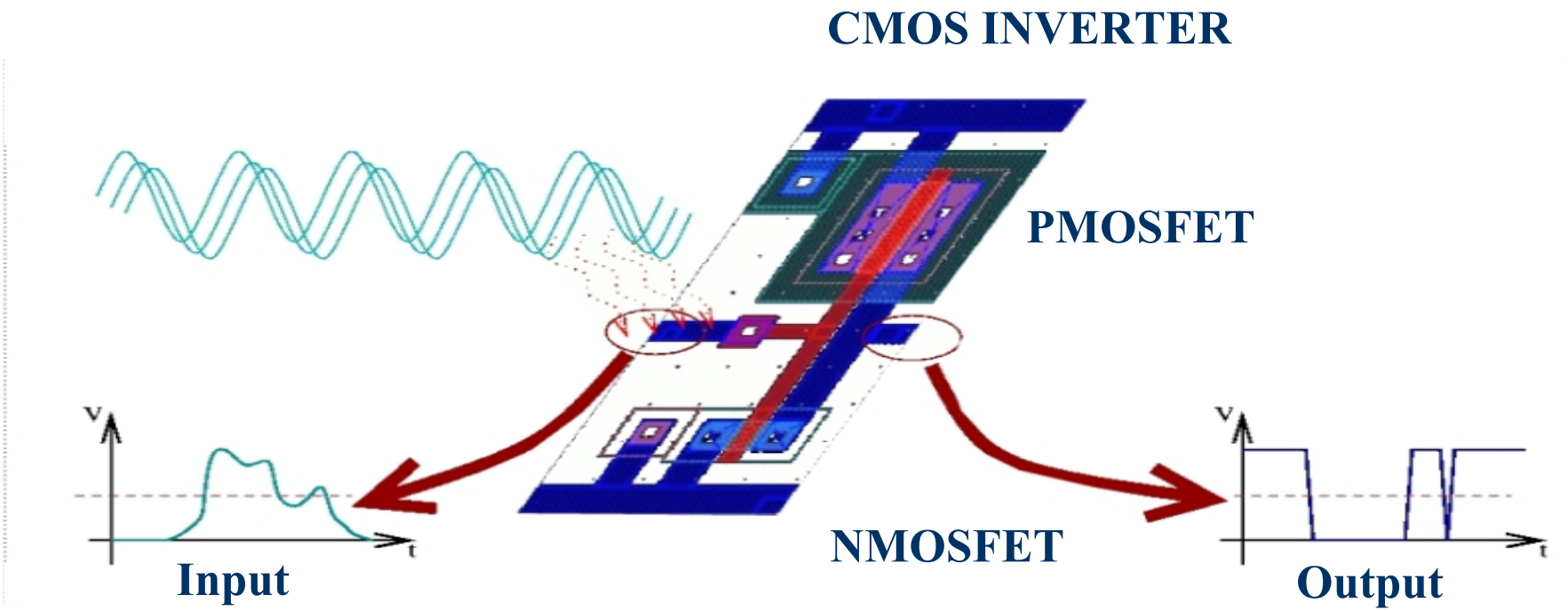
Outline

EM Coupling: Levels Investigated

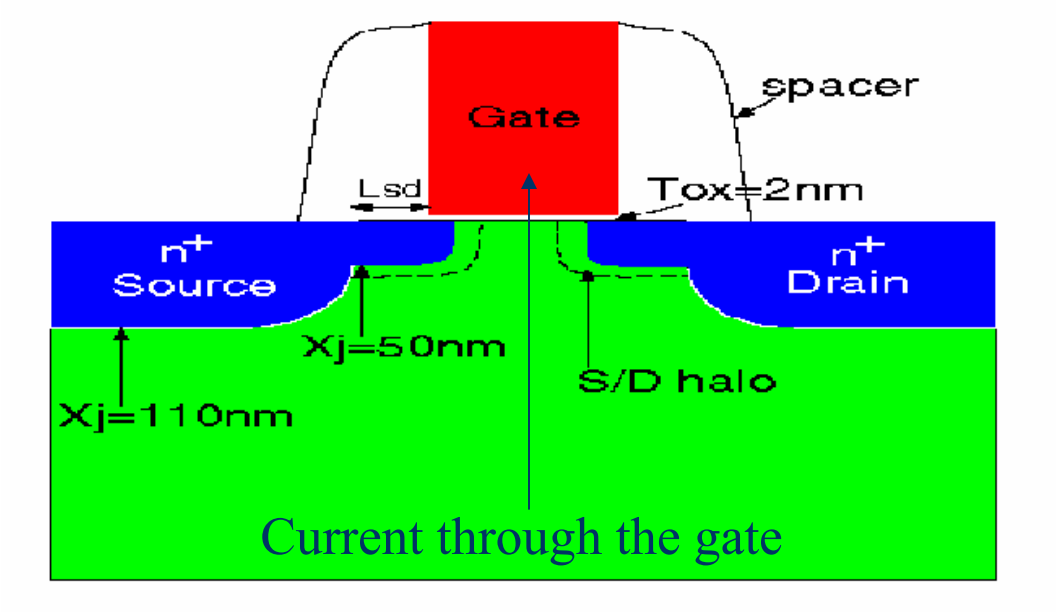
Task 1: Device Level

Task 2: Gate Level (Inverters)

Task 3: Interconnects and Passive Elements



MOSFET Cross-Section and Illustration of Vulnerabilities: Oxide and Avalanche Breakdown

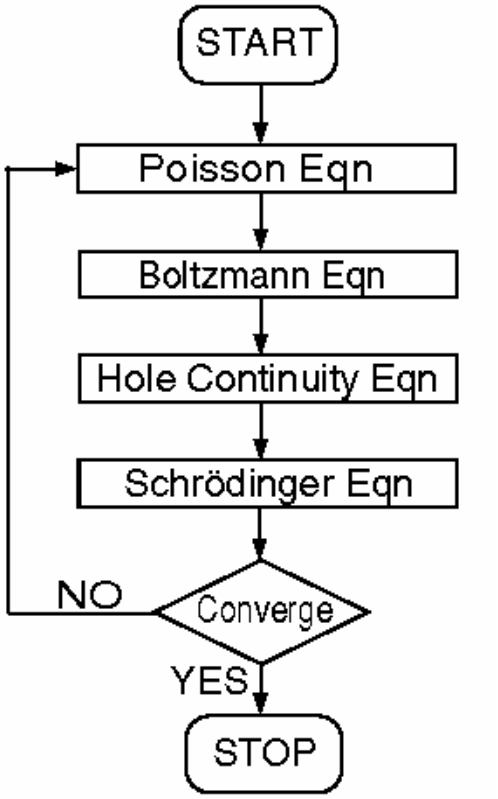


Problems:

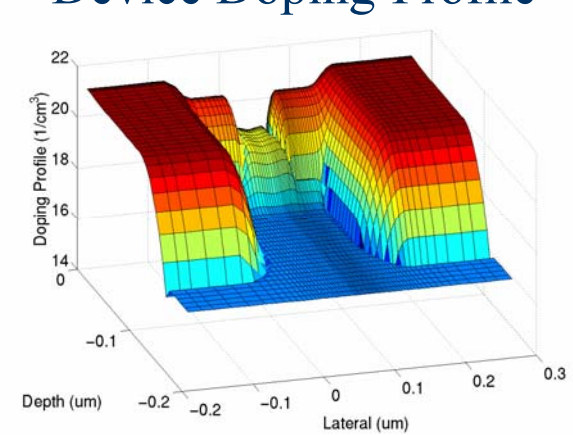
-Scaling to the nanometer gate length requires oxides less than 20Angstroms.
-Such thin oxides give rise to such large gate current that devices will not function.
-Large internal fields cause impact ionization, avalanching and damaging filaments
-Problems especially important for EM coupling, which can induce large voltages to Gate and Drain Electrodes!

Developed Quantum Device Simulator to Investigate Internal MOSFET Subject to Large Coupled EM Terminal Voltages

Solve QM Device Equations Numerically.
Inputs are device structure, doping profile & basic physics.



Device Doping Profile

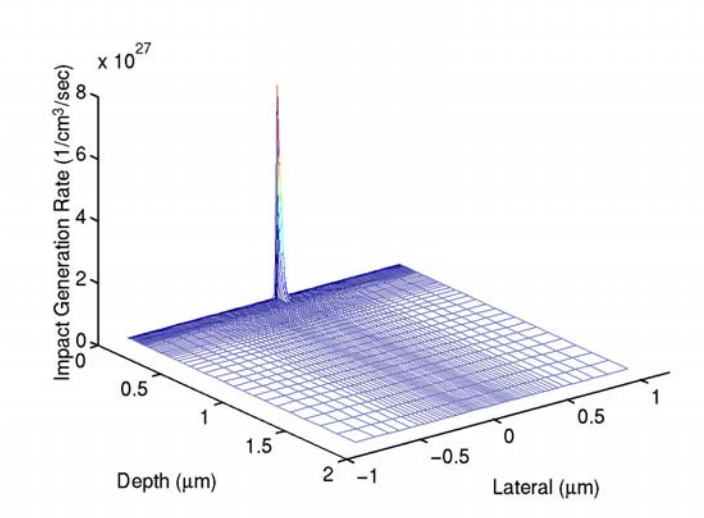


Electron Transport Physics Include:

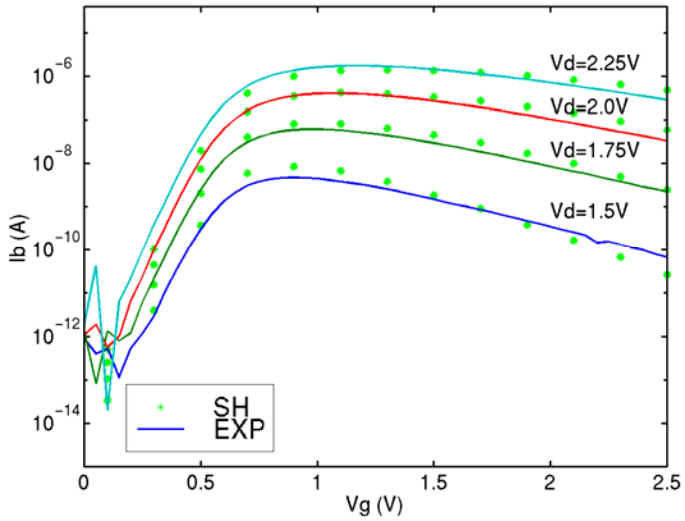
-Acoustic & Optical Phonons
-Band Structure
-Ionized Impurities
-Impact Ionization & Breakdown
-Surface Roughness
-Gate Current and Oxide Breakdown

Quantum Device Modeling Gives Internal Fields, Currents and Problem Spots:

Internal MOSFET Avalanche Rate



Resulting Parasitic Substrate Current



Using the new simulator to model EM induced avalanche breakdown

-Results indicate 2V on drain of 0.1μm causes excessive electron-hole pair generation peak in channel.

-Simulations agree with experiment on resulting substrate current

-Excessive substrate current causes permanent filament damage

Gate Current: Mathematical Model

The final gate leakage current will be the summation of the tunneling and thermionic current

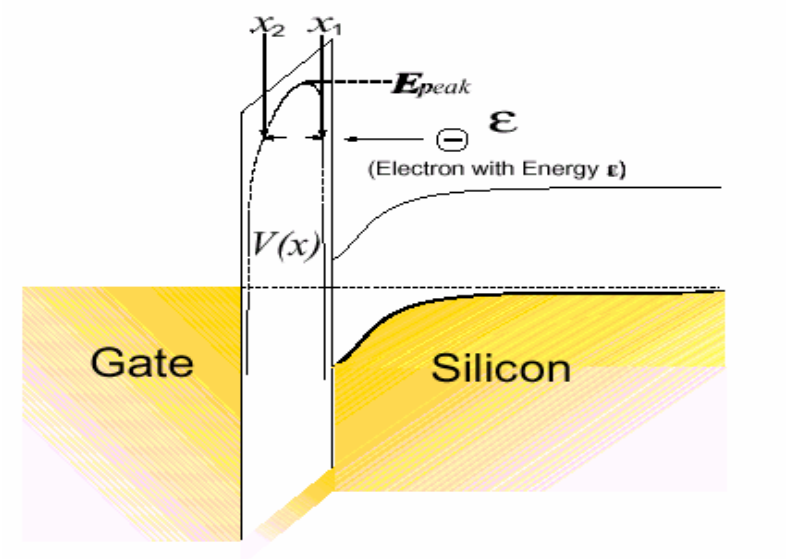
$$J_{gate}(x) = J_{tu}(x) + J_{th}(x)$$

Where tunneling current

$$J_{tu}(x) = \int_0^{E_{peak}} f(\xi, x)\, g(\xi)\, v_{\perp}(\xi)\, T_{tun}(\xi, x)\, d\xi$$

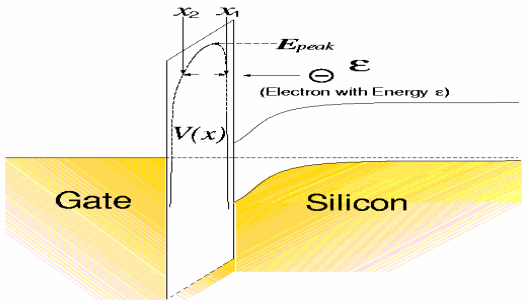
And thermionic current

$$J_{ther}(x) = \int_{E_{peak}}^{\infty} f(\xi, x)\, g(\xi)\, v_{\perp}(\xi)\, T_{ther}(\xi, x)\, d\xi$$

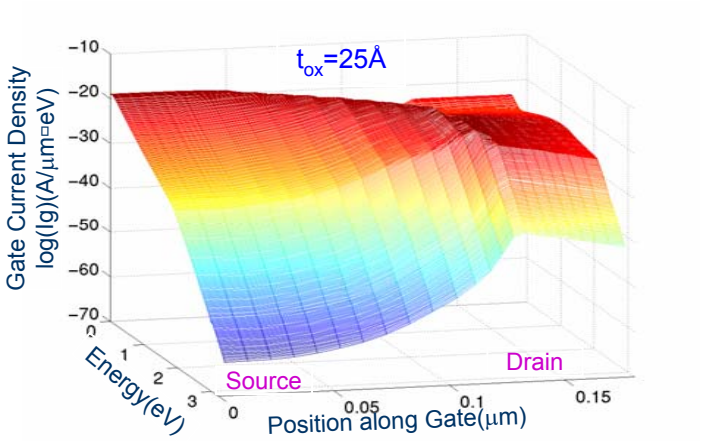


J_{gate} = Gate Current Density
f = Distribution Function
g = Density of States
T_{tu} = Tunneling Probability
T_{ther} = Thermionic Probability

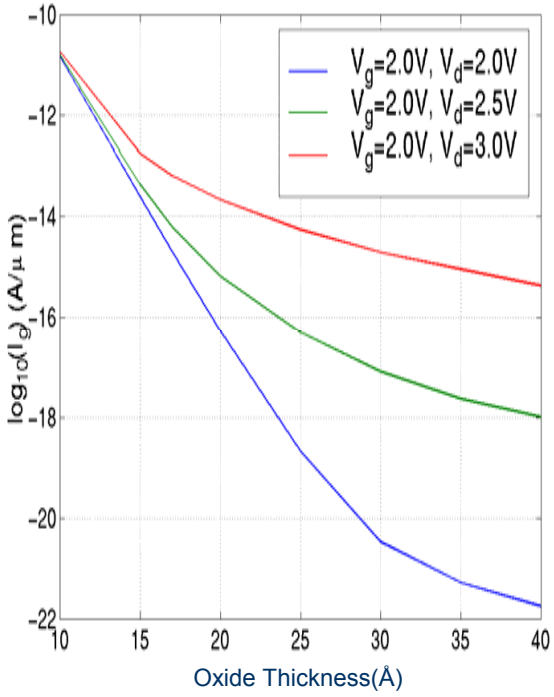
Boltzmann-Schrodinger/Spherical Harmonic Device CAD Results: Gate Current (WKB Method): Degrades Device



I_g vs V_g, V_d

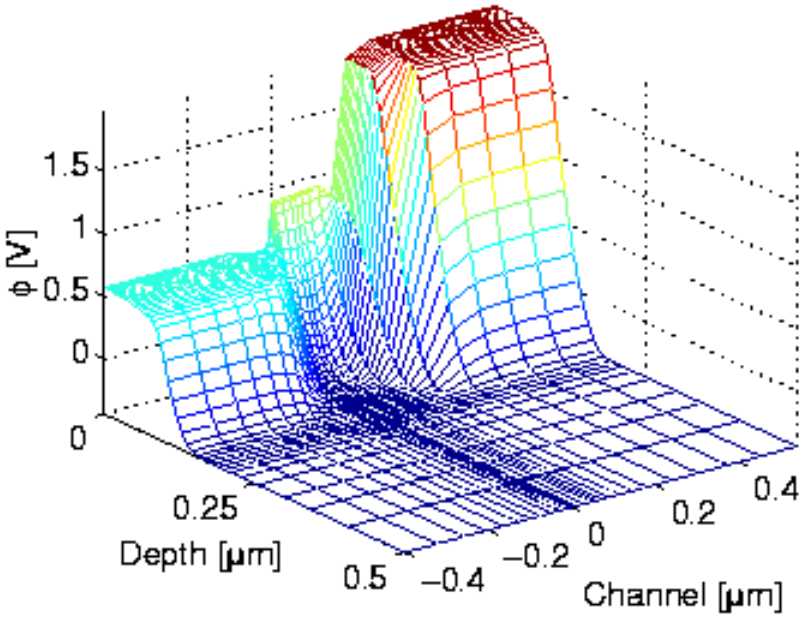


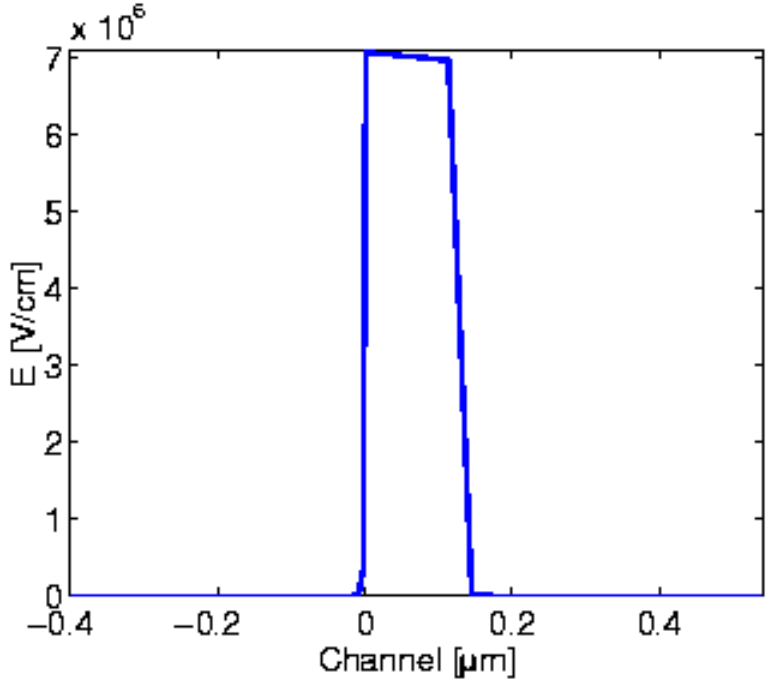
I_g vs Position and Energy



I_g vs Oxide Thickness

Resulting Electrostatic Potential inside 0.14μm MOSFET: Bias Conditions for Oxide Breakdown





V_G=2.8V V_D=1.4V V_S=V_B=0V

If $|E_y|$ > 7MV/cm => Oxide Breakdown

Device Simulations predicts induced gate voltage of 2X supply causes MOSFET oxide damage

Task 2. EM Effects on Gates

Differential equation based modeling of EM effects on inverter circuits

- Stage 1: Develop simulation tool.
- Stage 2: Use tool to analyze distributed effects of EM GHz range coupling on fundamental computer chip circuit elements.

Developed Distributed Circuit Simulator Applied to Inverters

DD Equations

$$\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}}(p - n + D)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . \overrightarrow{J_n} - R_n + G_n$$

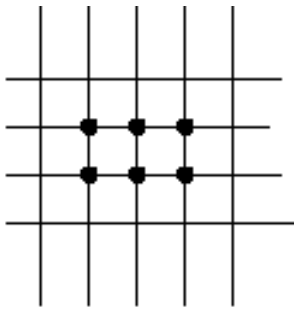
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . \overrightarrow{J_p} - R_p + G_p$$

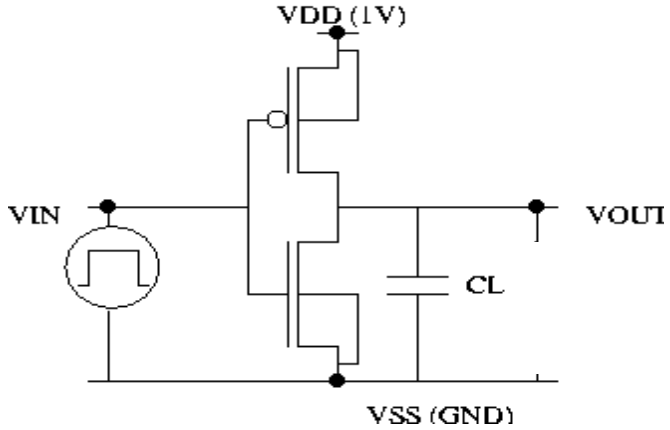
Supplementary DD Equations

$$\overrightarrow{J_n} = -q\mu_n n\overrightarrow{\nabla\Phi} + q\mu_n V_T \overrightarrow{\nabla n}$$

$$\overrightarrow{J_p} = -q\mu_p p\overrightarrow{\nabla\Phi} - q\mu_p V_T \overrightarrow{\nabla p}$$

Coupled Discretized DD Equations are solved at each mesh point





CMOS Inverter (CMI)

Lumped KCL equation check at the output node and using the KCL equation, the output guess is updated for the next iteration, V_O^{i+1}:

$$I_{DN} - I_{DP} + I_{R_L} + I_{C_L} = 0$$

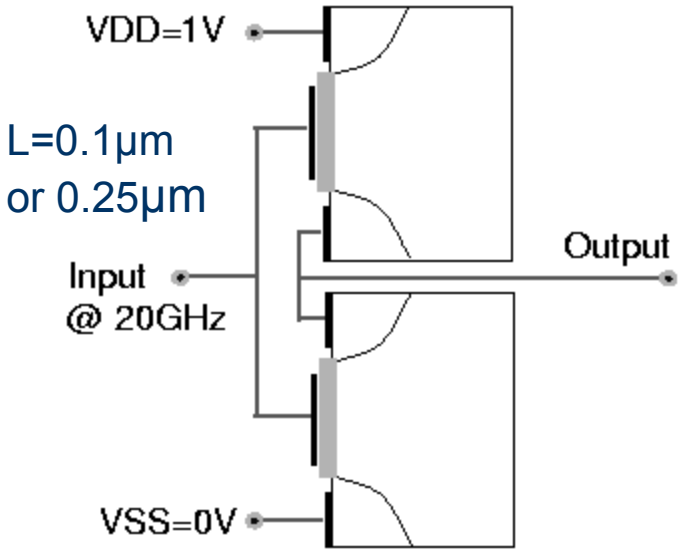
$$A_N + B_N V_o^{i+1} + A_P + B_P V_o^{i+1} + \frac{V_o^{i+1} - V_{SS}}{R_L} + C_L \frac{V_o^{i+1} - V_o^i}{\Delta t} = 0$$

$$V_o^{i+1} = \frac{V_{SS} + V_o^i \frac{R_L C_L}{\Delta t} - (A_N + A_P)R_L}{1 + \frac{R_L C_L}{\Delta t} + (B_N + B_P)R_L}$$

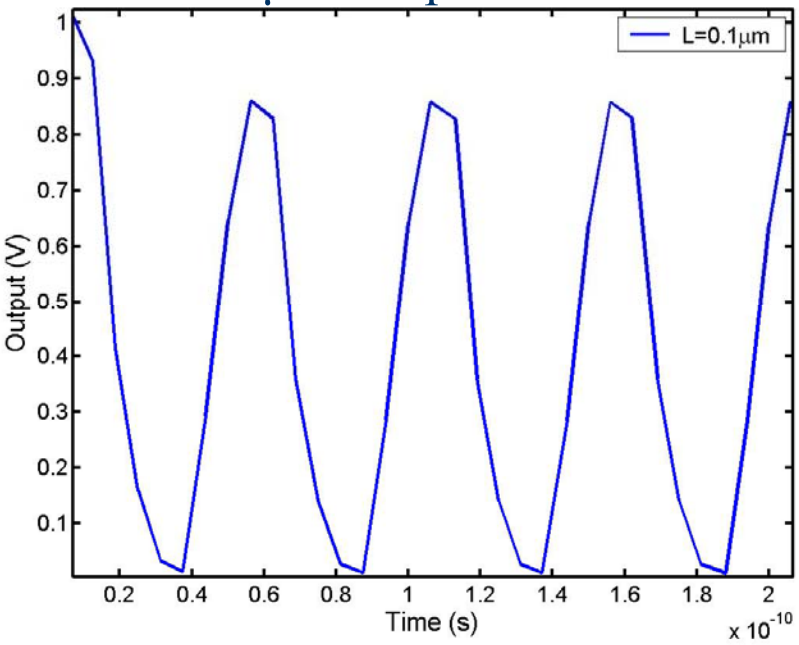
Modeling 20GHz, 1V Coupled to 0.1μm & 0.25μm Inverters

-Output follows input but with reduced amplitude in 0.25

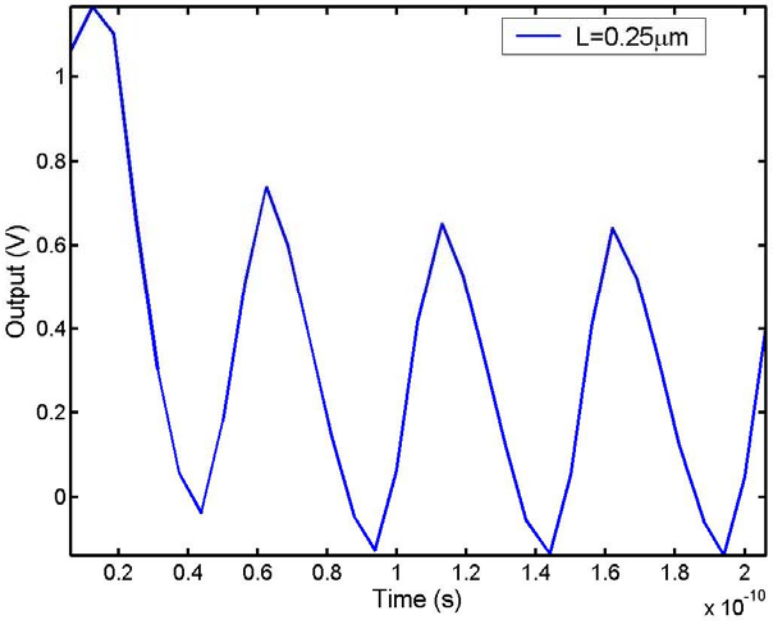
-Bit errors can still occur in larger device but may be less likely



0.1μm Output



0.25μm Output



An Impulse-Response Based Methodology for Modeling Complex On-Chip Interconnect Networks: Random or Deterministic Inputs

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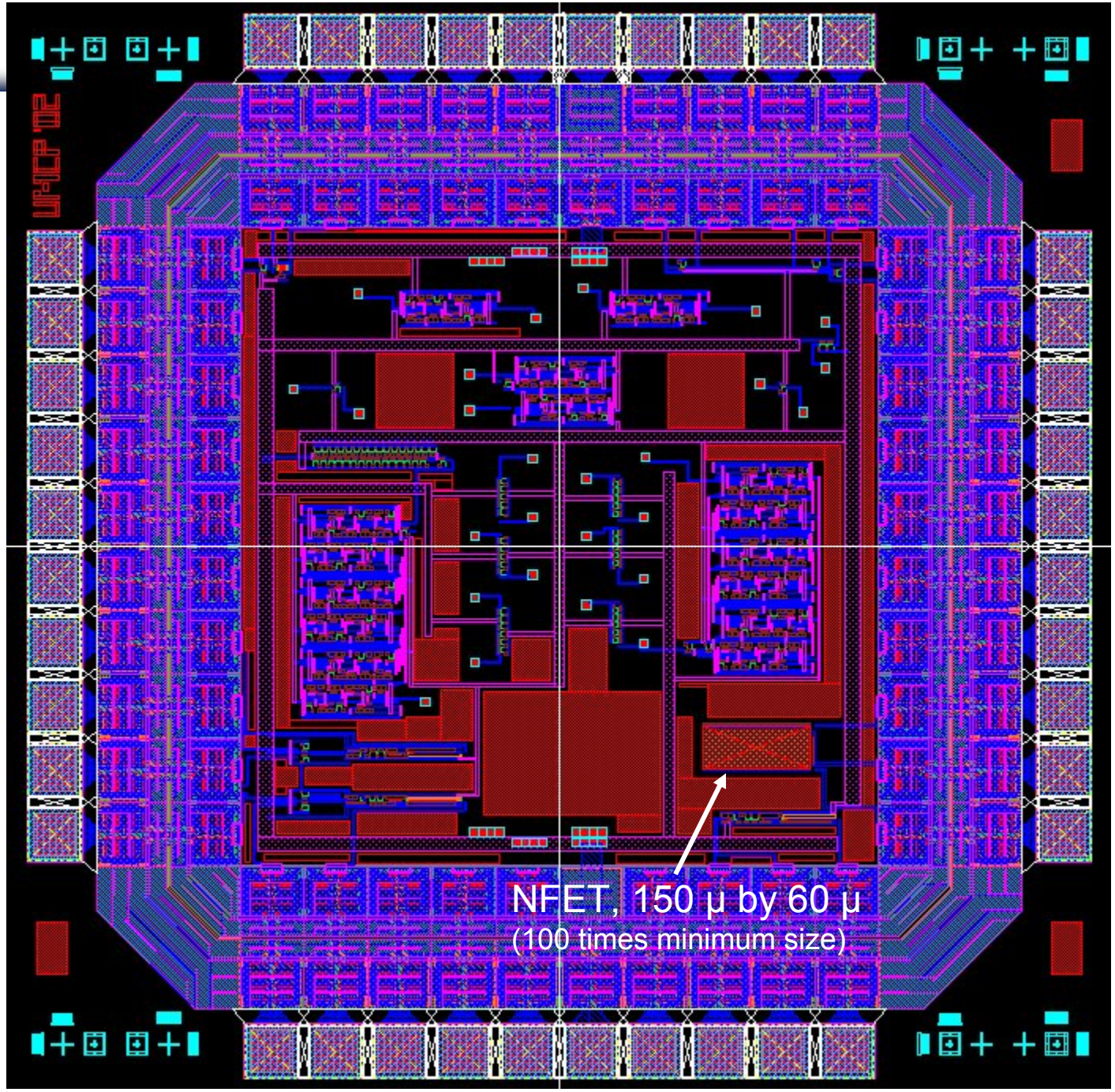
Experimental Chip for EM Coupling and Gate Current Measurements.

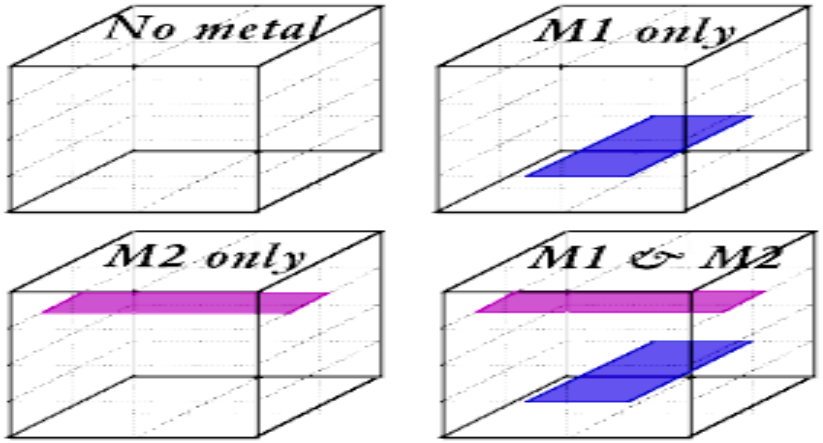
Designed at UMD Fabricated by MOSIS

Thousands of Metal Interconnect lines



Interconnect Network Modeling

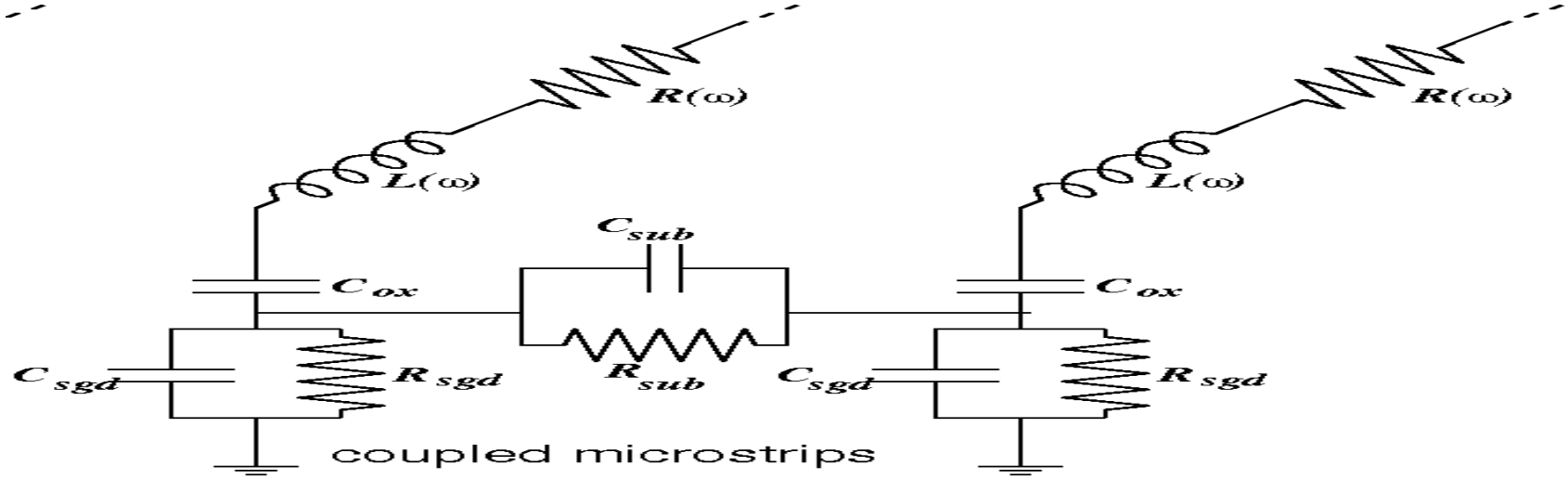
- *Objective:* Investigate the response of a complex on-chip interconnect network to external RF interference or internal coupling between different chip regions
- Full-chip electromagnetic simulation: Too computationally-intensive
- Full-wave simulation possible for small "unit cell"s: Simple seed structures of single and coupled interconnects, combined to form the network.
- We have developed a methodology to solve for the response of such a network composed of unit cells with random inputs.



Sample unit cells for a two-metal process

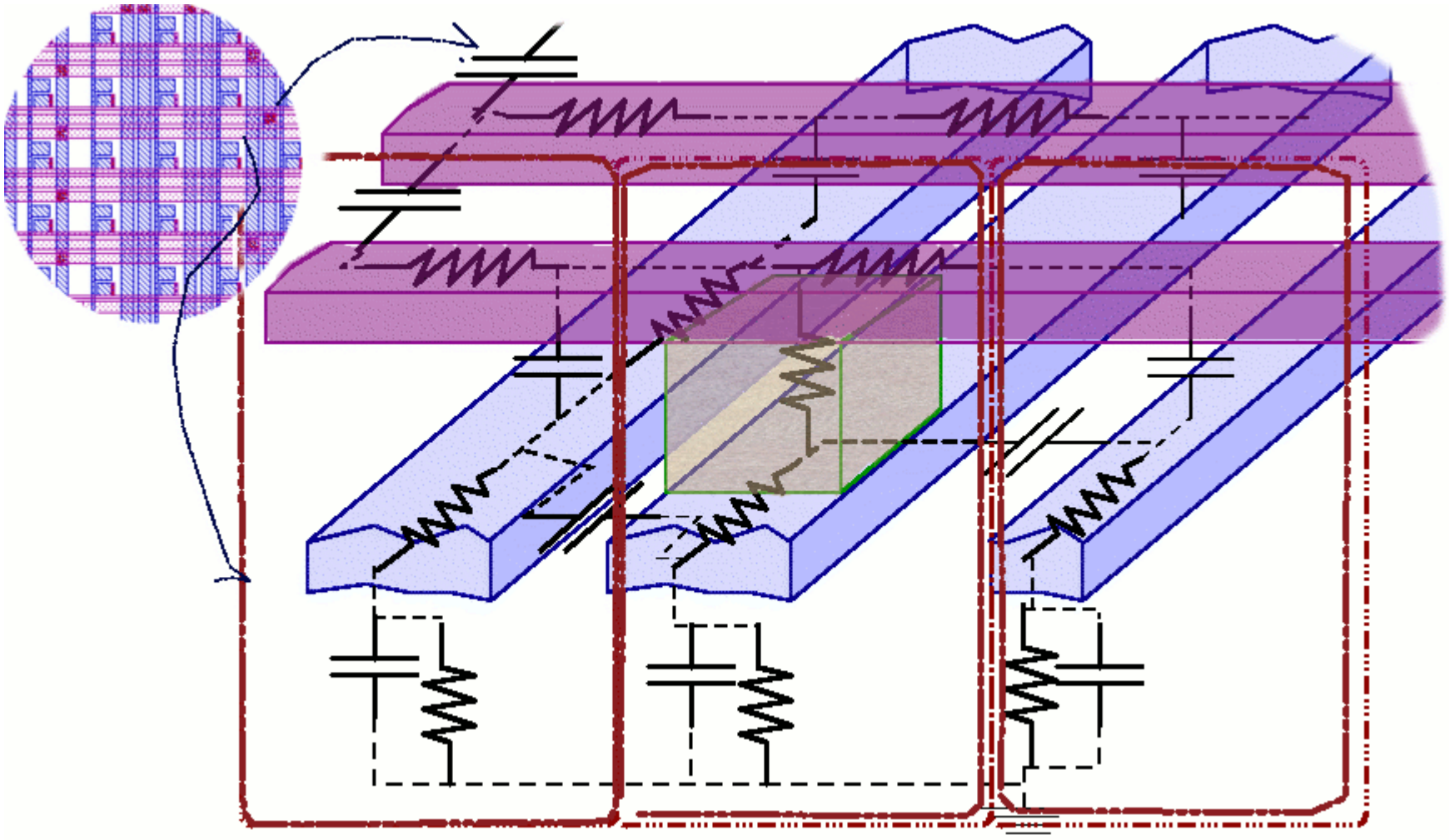
Interconnect Network Modeling

- On-chip interconnects on lossy substrates: capacitively and inductively coupled to each other
  - Characterized with S-parameter measurements
  - Equivalent circuit models found by parameter-fitting
- For small interconnect unit cells, create an equivalent circuit model from EM simulation results/S-parameters.



Interconnect Network Modeling

- Lumped element model: Uses resistors and capacitors (Unit cells marked with red boxes in the figure).



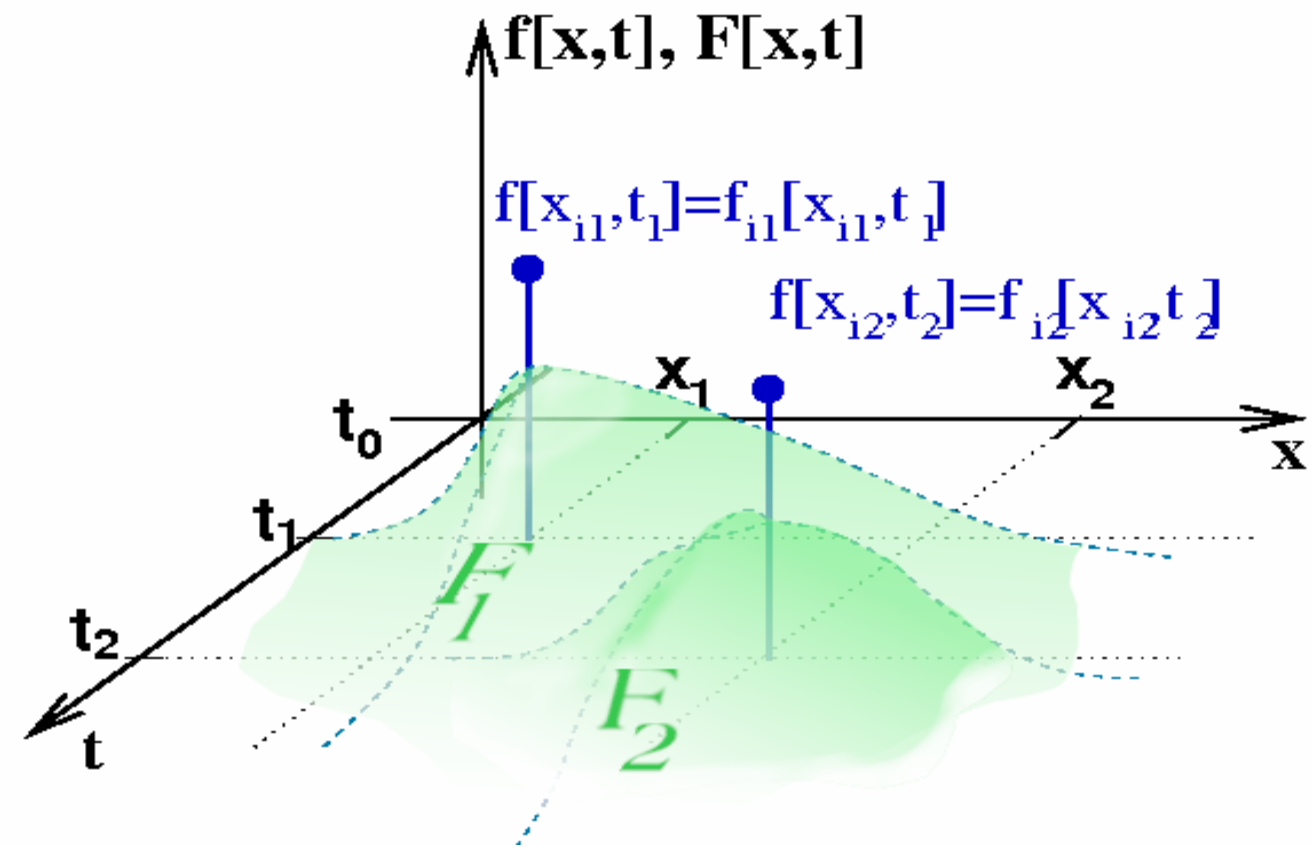
Interconnect Network Modeling

- The interconnect network is a linear time invariant system: It is possible to calculate the output to any input distribution in space and time from the impulse responses.

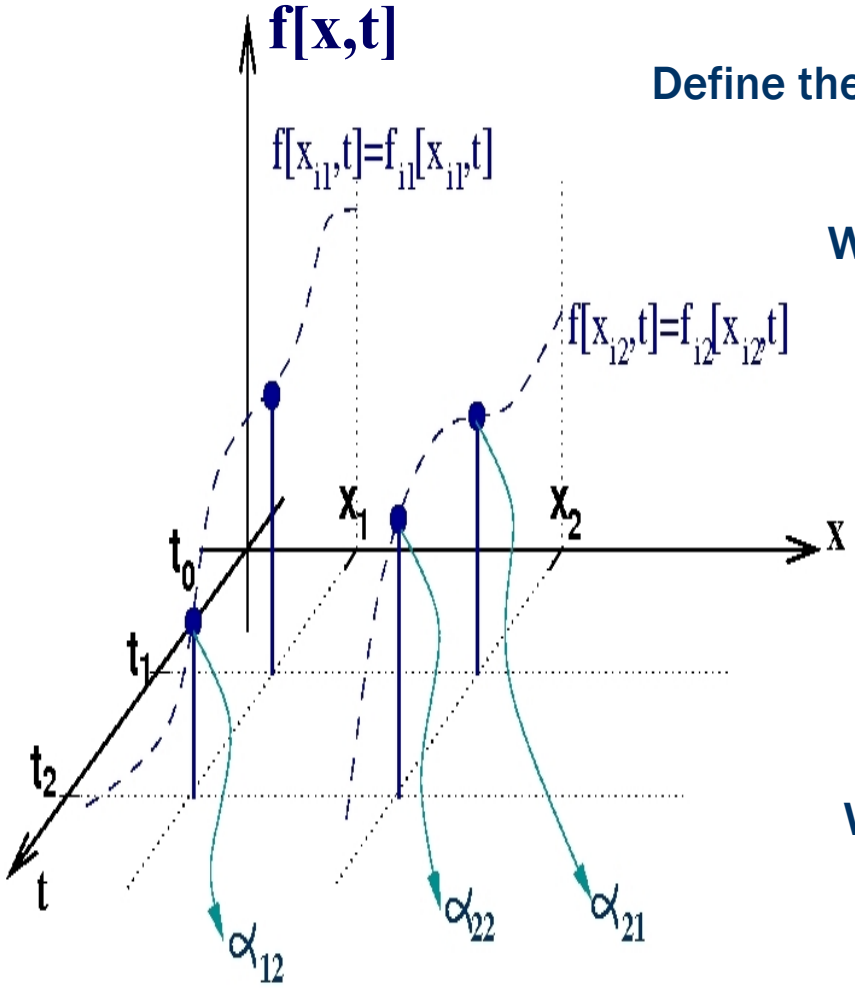
Characterize System by Response to Impulses

$$f[x,t] = \sum f_i[t] \Rightarrow F[x,t] = \sum F_i[t]$$

$$\Rightarrow F[x,t] = \sum_i \sum_j f_i[t_j] h_i[x, t - t_j]$$



Response to a General Input from Impulse Responses



Define the *unit impulse* at point x_i: $\delta[x-x_i]=\begin{cases}1, & x=x_i\\ 0, & \text{else}\end{cases}$

We calculate the *system's impulse response*:

$\delta[x-x_i]\delta[t-0]$ → $h_i[x,t]$

Let an input f[x,t] be applied to the system. This input can be written as the superposition of time-varying input components $f_i[t]=f[x_i,t]$ applied to each point x_i:

$$f[x,t]=\sum_i f_i[t]$$

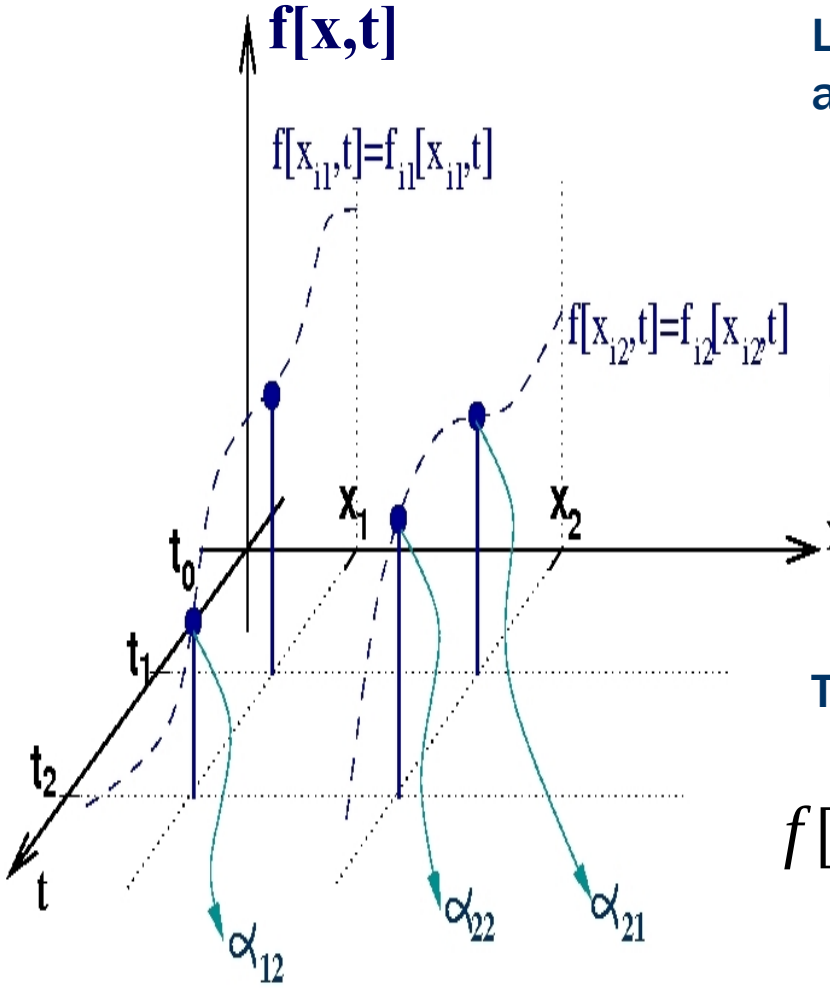
We can write these input components $f_i[t]$ as

$$f_i[t]=f[x,t]\delta[x-x_i]$$

Writing $f_i[t]$ as the sum of a series of time-impulses marching in time:

$$f_i[t]=\sum_j f[x,t\ ]\delta[x-x_i]\delta[t-t_j]$$

Response to a General Input from Impulse Responses



Let $F_i[x,t]$ be the system's response to this input applied to x_i:

$$f_i[t] \rightarrow \boxed{} \rightarrow F_i[x,t]$$

For a time-invariant system we can use the impulse response to find $F_i[x,t]$:

$$F_i[x,t] = \sum_j f_i[t_j] h_i[x, t - t_j]$$

Then, since

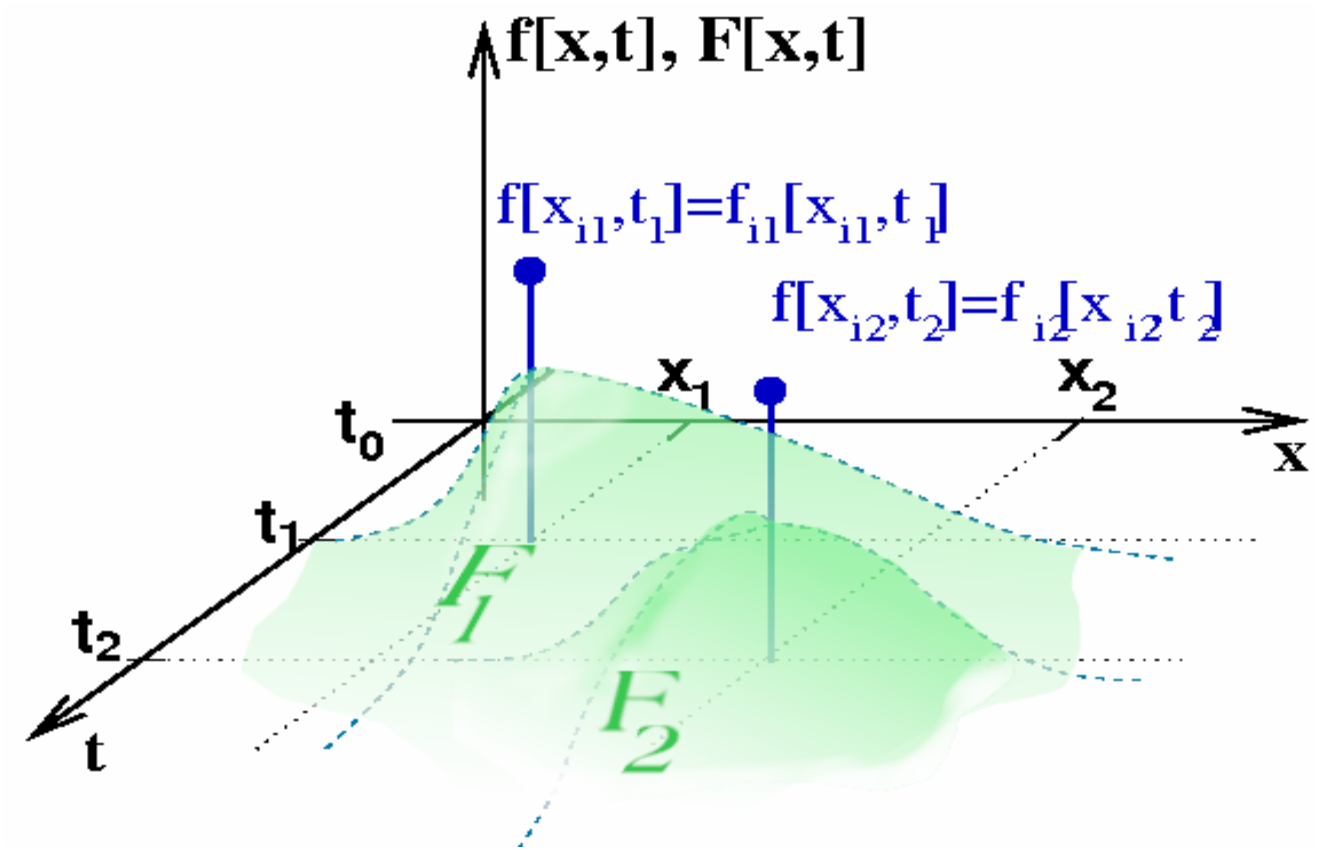
$$f[x,t] = \sum_i f_i[t] \Rightarrow F[x,t] = \sum_i F_i[x,t]$$

$$\Rightarrow F[x,t] = \sum_i \sum_j f_i[t_j] h_i[x, t - t_j]$$

Response to a General Input from Impulse Responses

$$f[t] = \sum f_i[t] \Rightarrow F[t] = \sum F_i[t]$$

$$\Rightarrow F[x,t] = \sum_i \sum_j f_i[t_j] h_i[x, t - t_j]$$



Characterize Impulse Response of Entire Chip

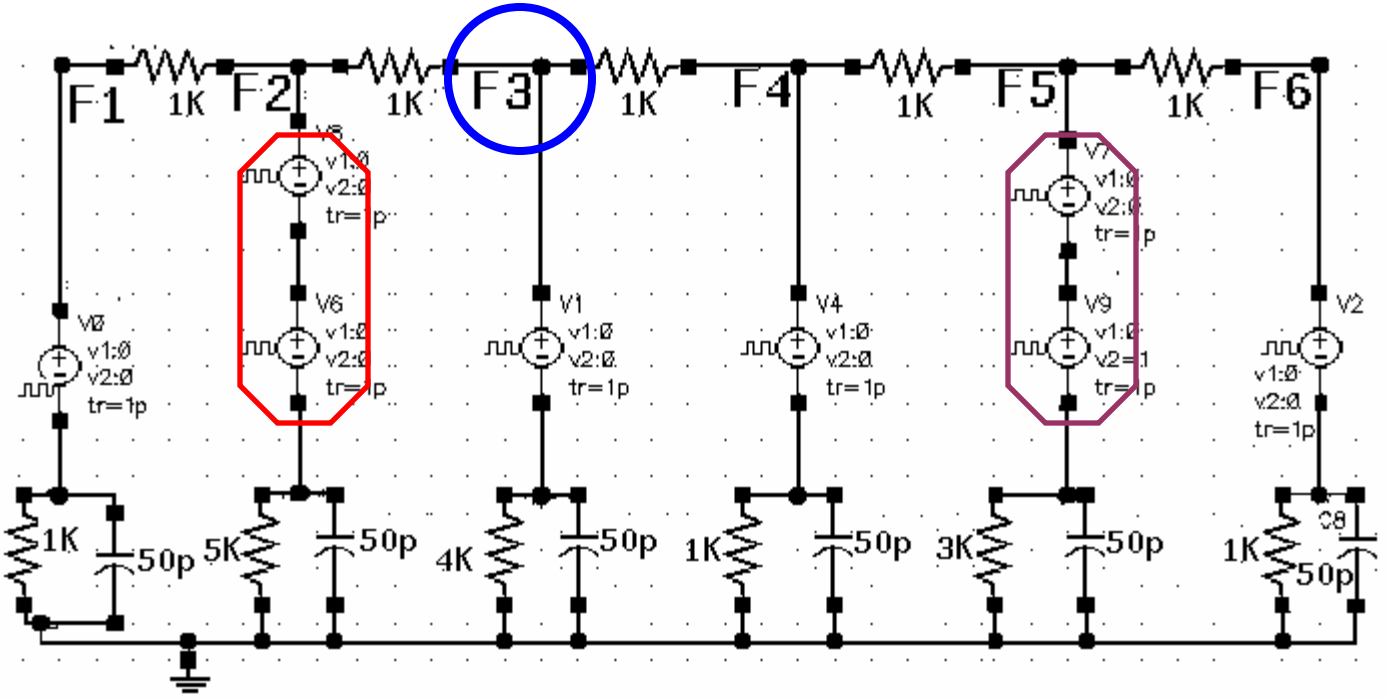
- Choose a spatial mesh and a time period
- Calculate the impulse response over all the period to impulse inputs at possible input nodes (might be all of them)
- The input values at discrete points in space and time can be selected randomly, depending on the characteristics of the interconnect network (coupling, etc.) and of the interference. Let

$$\alpha_{ij} := f[x_i, t_j]$$

$$\Rightarrow F[t] = \sum_i \sum_j \alpha_{ij} h_i[x, t - t_j]$$

- Then we can calculate the response to any such random input distribution α_{ij} by only summation and time shifting
- We can explore different random input distributions easily, more flexible than experimentation

A Demonstration using SPICE



- *Goal:* Simulate response at Point F3 to a discrete-time input given by the sum of two impulses at Point 2 and two at Point 5:

$$2\delta(x-x_2,t)+3\delta(x-x_2,t-200ns)$$

$$+3\delta(x-x_5,t-100ns)+\delta(x-x_5,t-400ns)$$

A Demonstration using SPICE

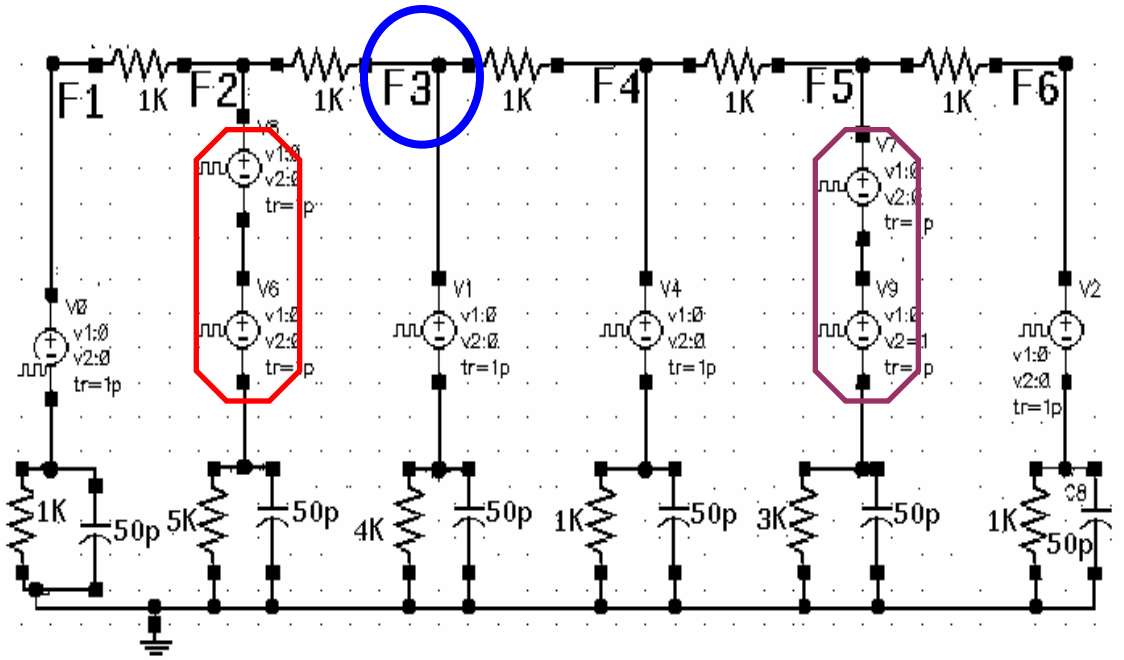
- Theoretically, the response at point F3 to this input

$$2\delta(x-x_2,t)+3\delta(x-x_2,t-200ns)$$

$$+3\delta(x-x_5,t-100ns)+\delta(x-x_5,t-400ns)$$

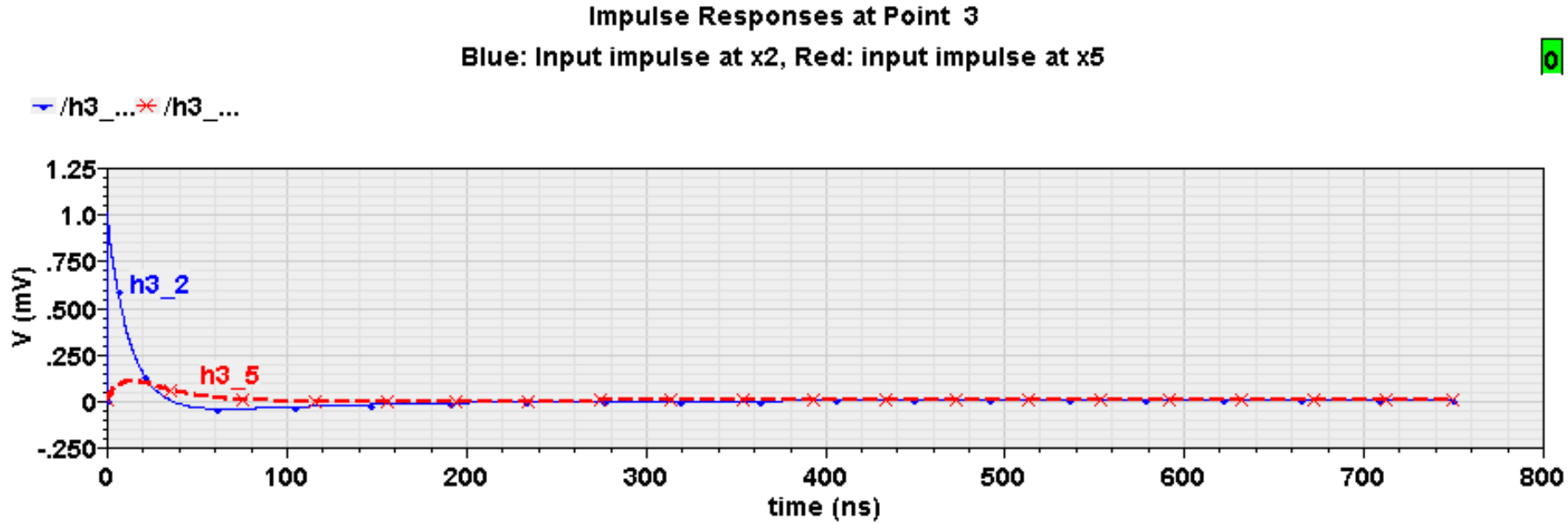
is obtainable by the time-shifted sum of scaled impulse responses:

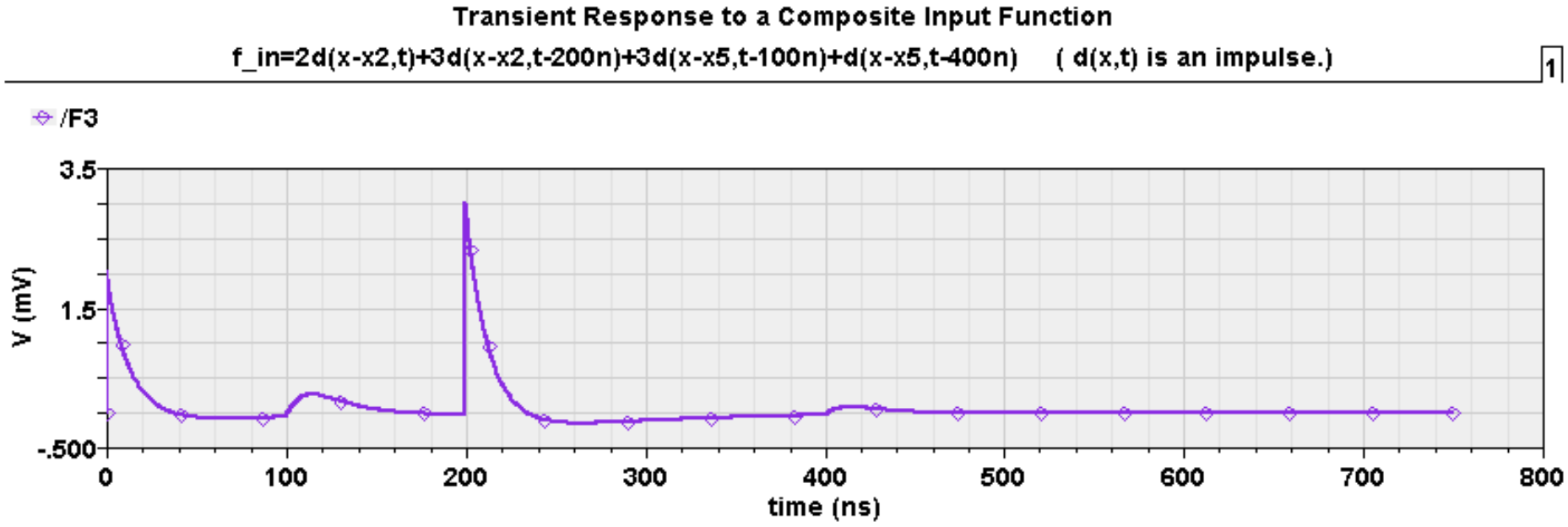
$$2h_{3\_2}(t)+3h_{3\_2}(t-200ns)+3h_{3\_5}(t-100ns)+h_{3\_5}(t-400ns)$$



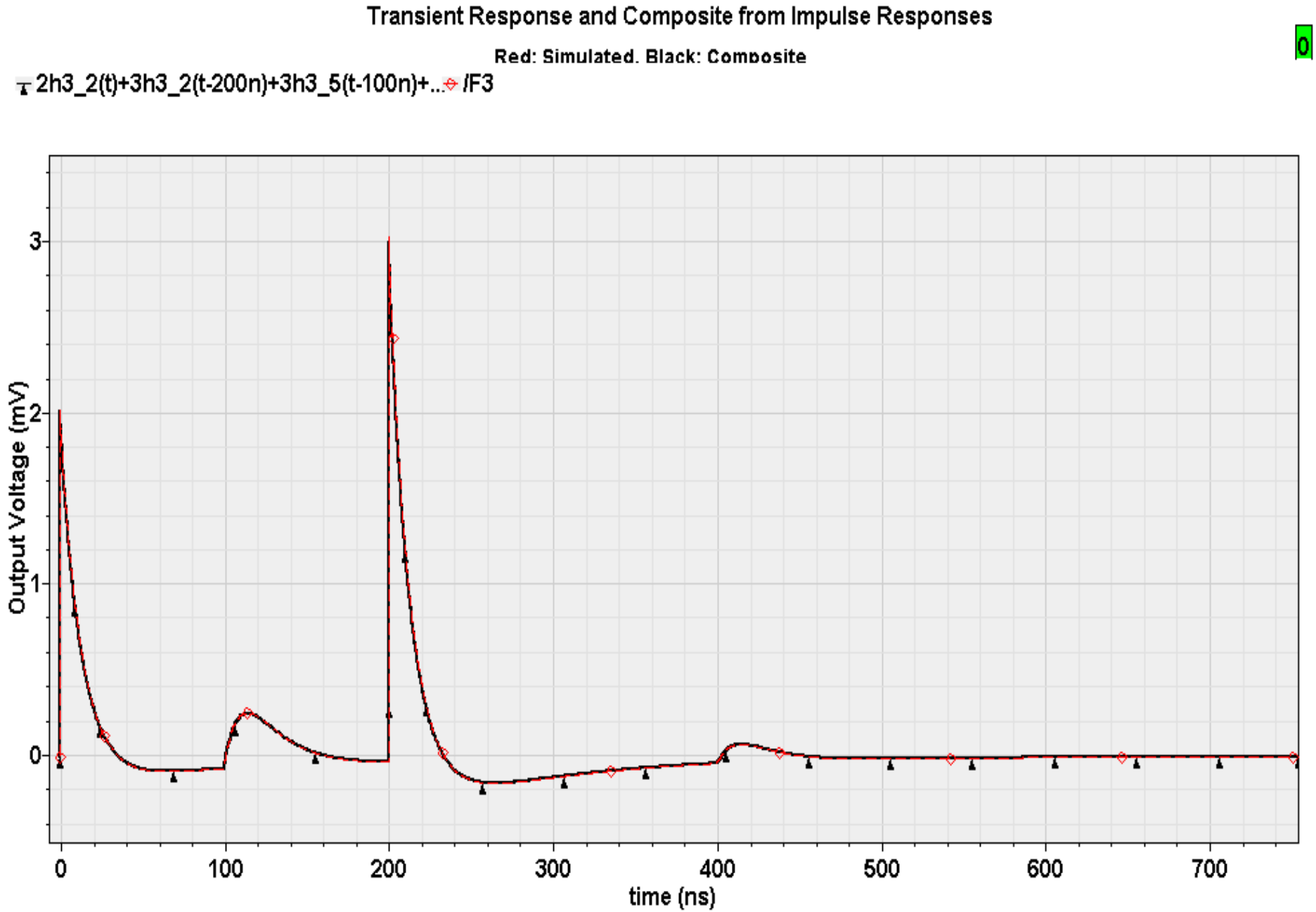
- Calculate this analytically from the simulated impulse responses and compare with simulation result

A Demonstration using SPICE





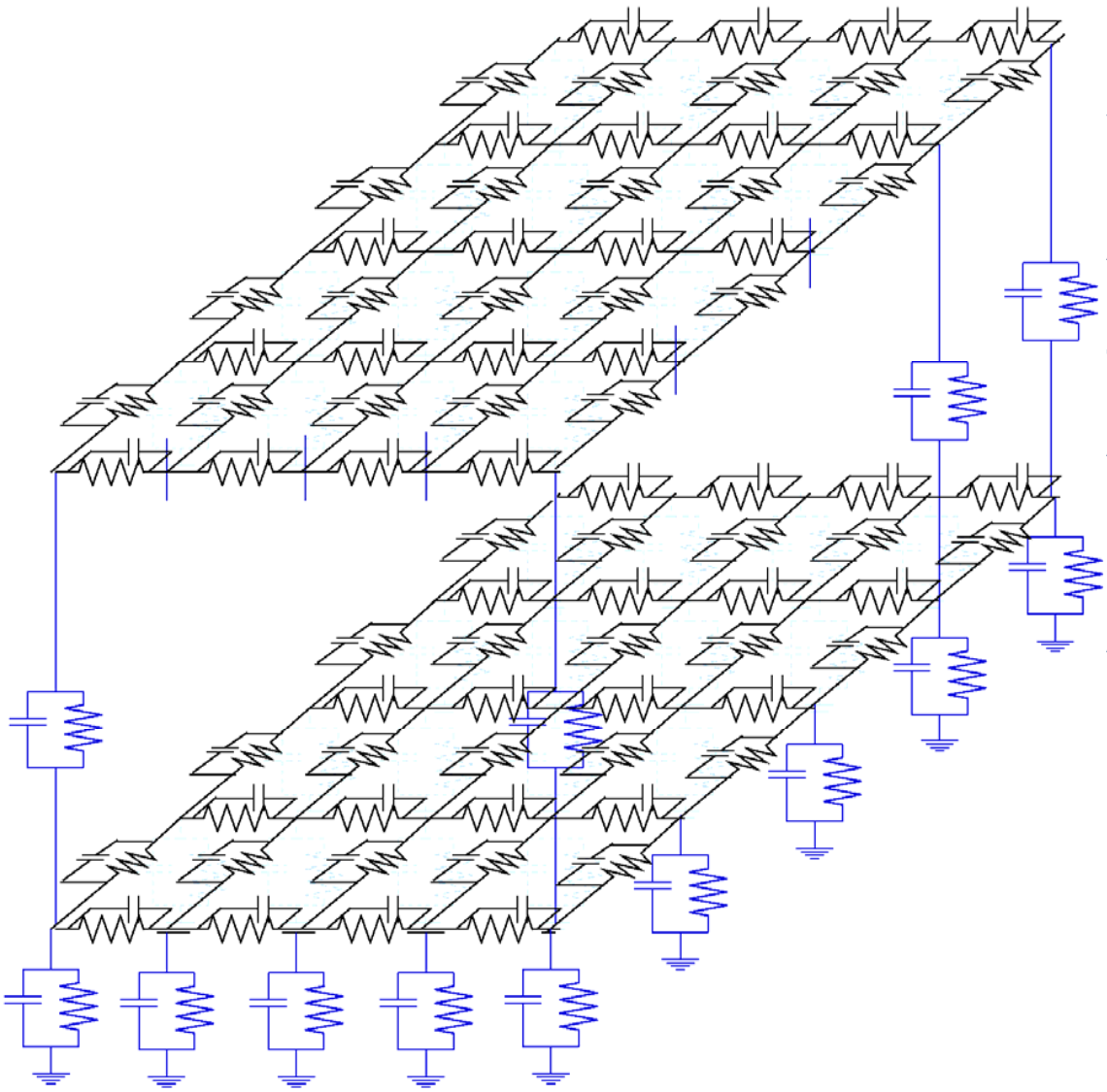
Impulse Response and SPICE Agree



Interconnect Network Solver Outline

- Developed an in-house network solver. Preliminary results presented at ISDRS'05, December 2005. More results to be presented in SISPAD 2006.
- *Inputs:* A 2-D or 3-D lumped network; input waveforms with the input locations indicated; locations that the user wishes to observe responses at.
- *Outputs:* Impulse responses at given output locations to impulses at given input locations; the composite output at given output locations to the input waveforms provided.
- *Algorithm:*
  1. Read in network mesh structure, the input impulse locations, the output locations
  2. Set up the KCL-based system of difference equations for the mesh
  3. For each impulse location, stimulate the system with a unit impulse
     1. Solve for the time evolution of the voltage profile across the network
     2. Record the values at the set output points, creating impulse responses vs. time
  4. Use the full input waveforms together with calculated impulse responses to compose the full output at the requested output locations.
- *Computational advantages*:
  - Impulse responses calculated once used for system response to many inputs;
  - Impulse responses at only the desired points in the system need to be stored to calculate the output at those points for any input waveform.

Sample 3-D Network



Only 5x5x2 mesh shown for simplicity. Not all vertical connections shown.

All nodes on the same level connected with an R//C to their neighbors.

All nodes on lowest level are connected with an R//C to ground.

All nodes in intermediary levels are connected with an R//C to neighbors above and below.

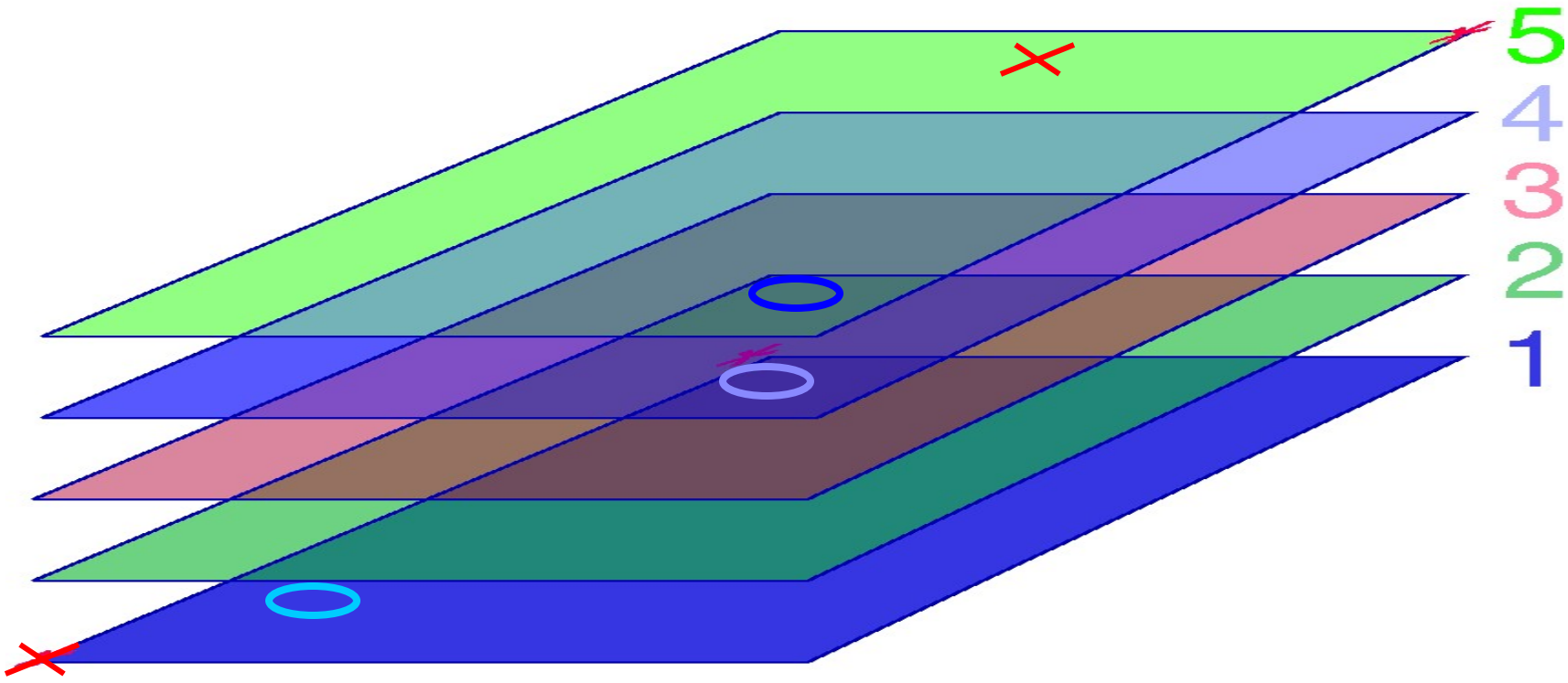
Impulse Response Solver Results: 11x11x5 Mesh

Solves for the response over the mesh using a system of differential equations derived from KCL equations.

Given here: Results for a 11x11x5 mesh.

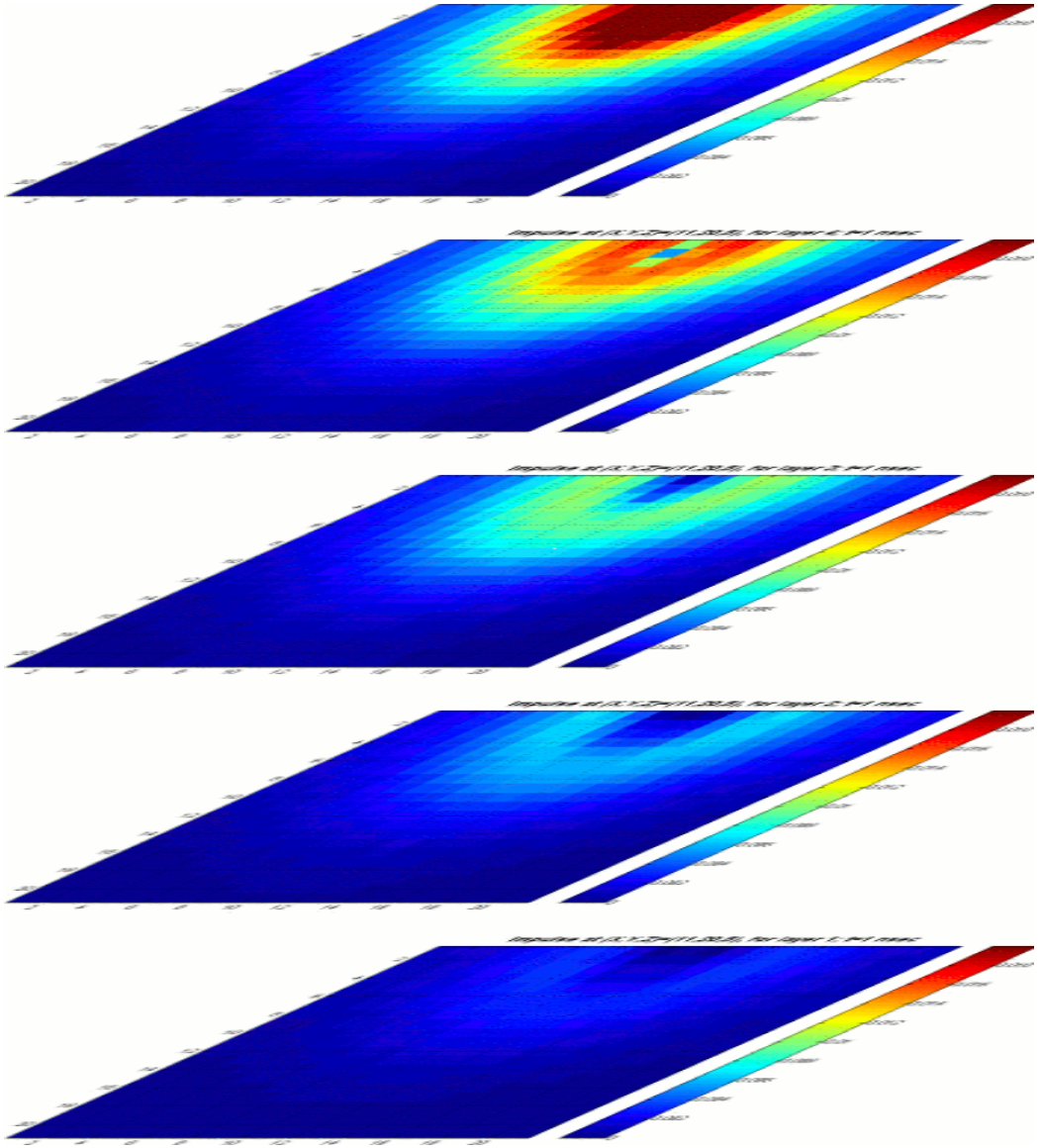
Input points: **(1,1,1)** (bottom layer, southwest corner), **(11,20,5)** (near north edge center, topmost layer).

Sample output points **(5,5,1)** (bottom layer, southwest of center); **(11,11,3)** (center layer, exact center); **(20,2,5)** (top layer, southeast of center).



Impulse Response Solver Results: : 11x11x5 Mesh

Sample impulse response over all five layers:



Unit impulse at point (11,20,5).

The animation shows the impulse response until t=6 nsec with 1 nsec increments.

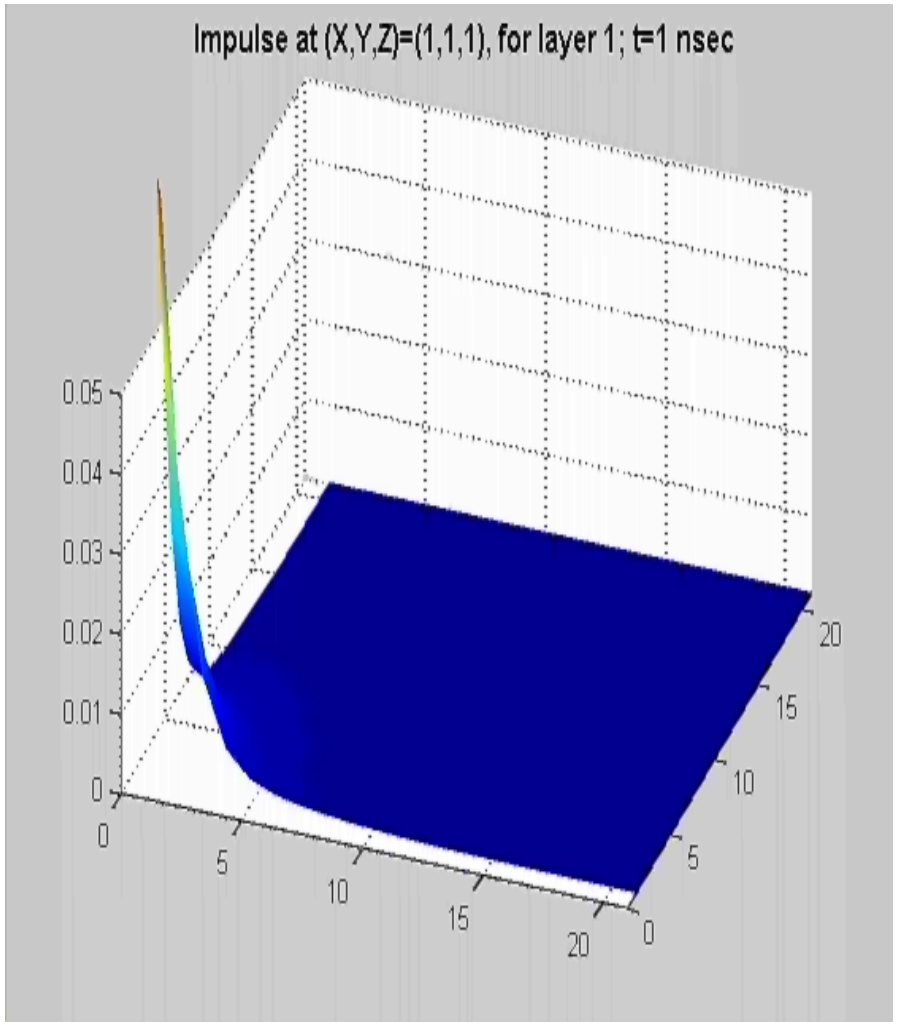
Note that this result is from a network with all horizontal connections resistive only.

Impulse Response Solver Results : 11x11x5 Mesh

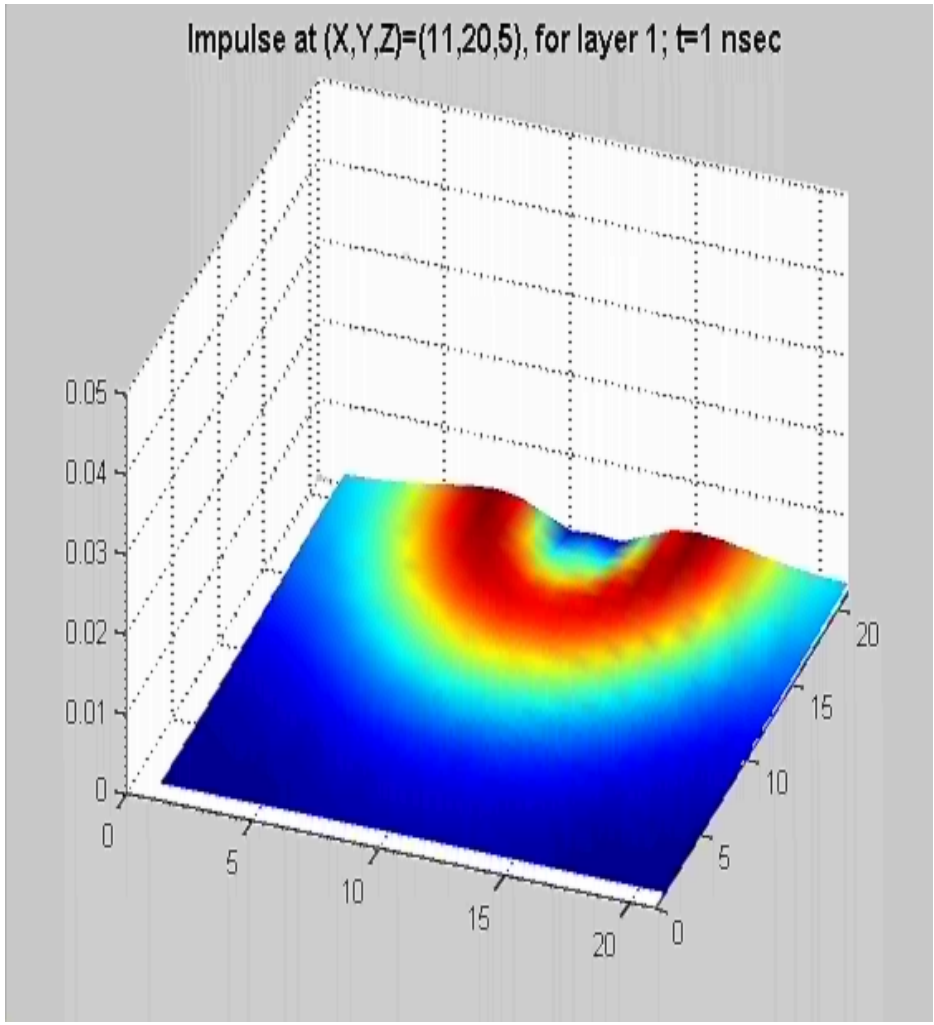
Sample impulse responses shown one layer at a time (click to play; horizontal connections resistive only.):

Layer 1

Impulse at (1,1,1)



Impulse at (11,20,5)

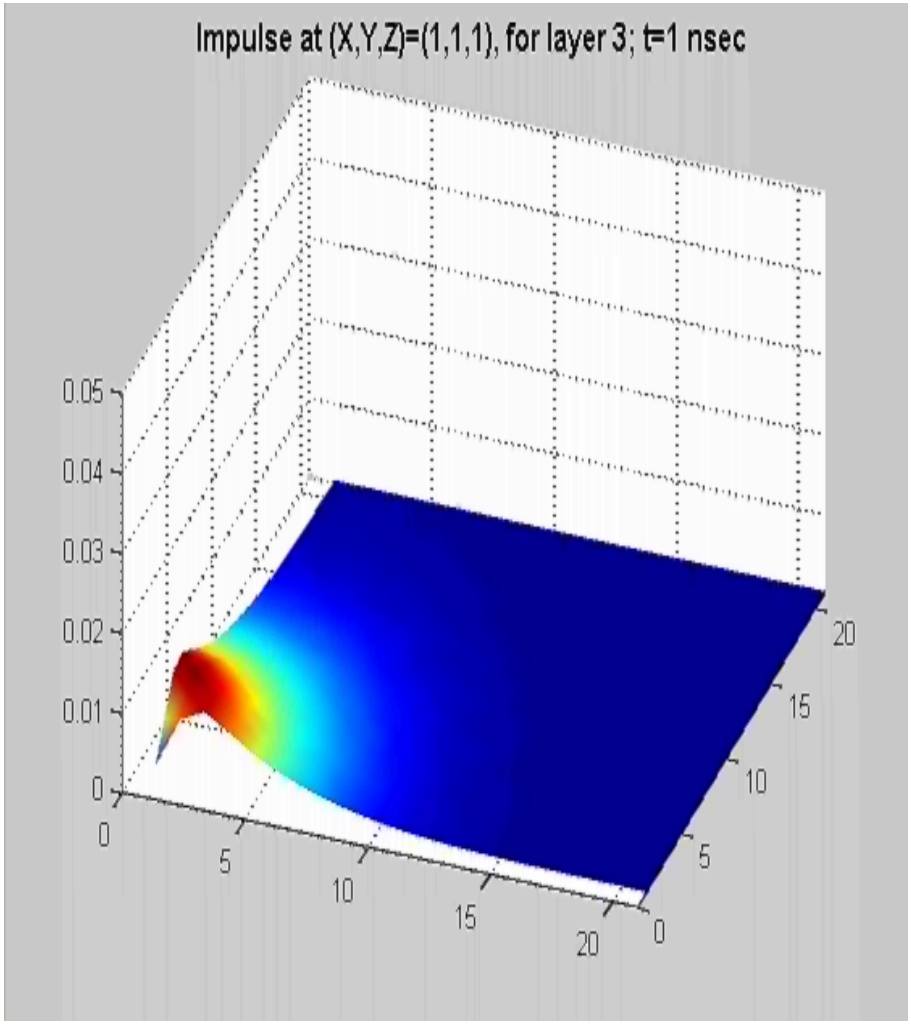


Impulse Response Solver Results : 11x11x5 Mesh

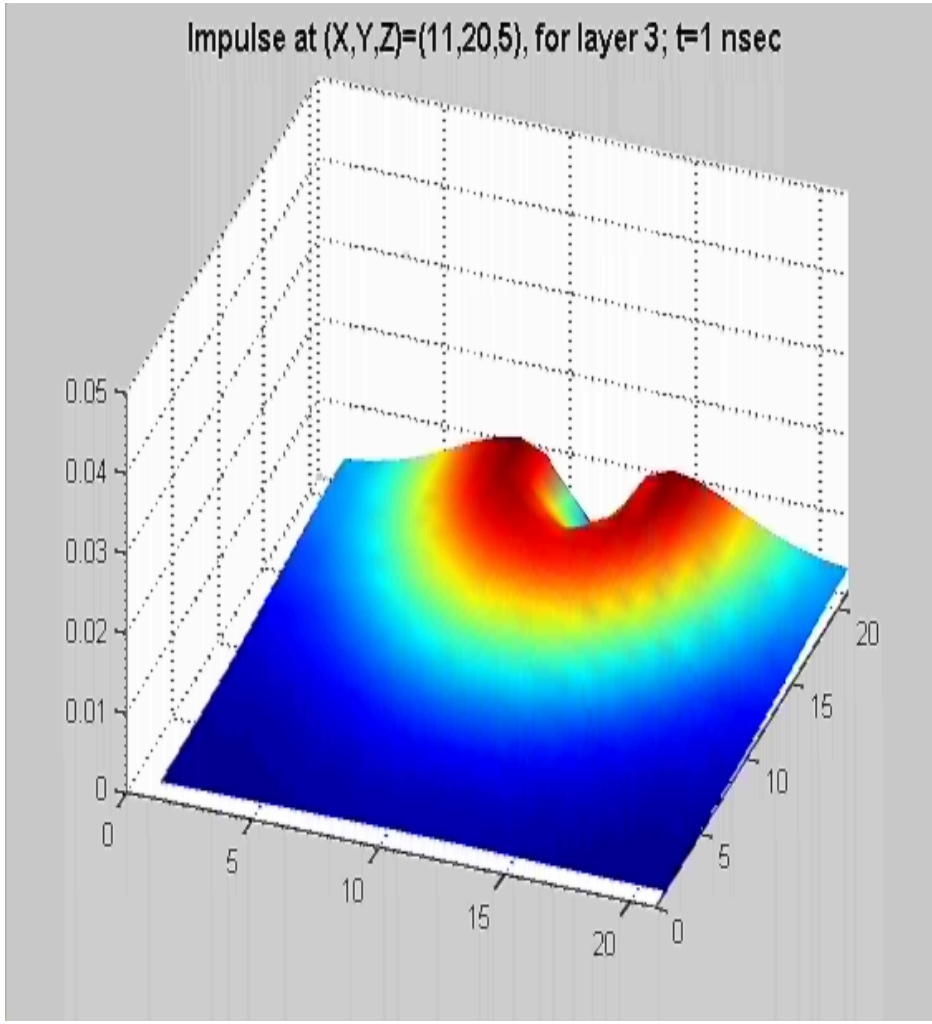
Sample impulse responses shown one layer at a time (click to play; horizontal connections resistive only.):

Layer 3: Note that the north-south resistors are smaller than east-west resistors; hence the uneven response distribution.

Impulse at (1,1,1)



Impulse at (11,20,5)

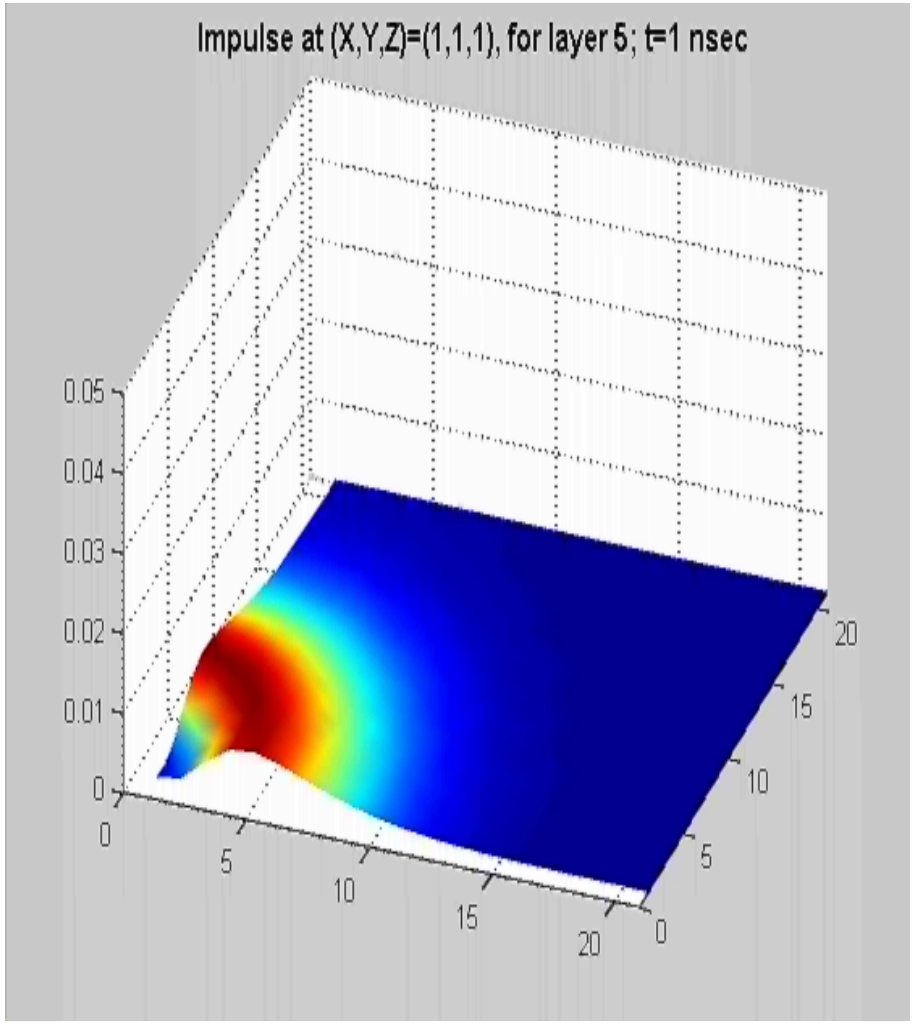


Impulse Response Solver Results : 11x11x5 Mesh

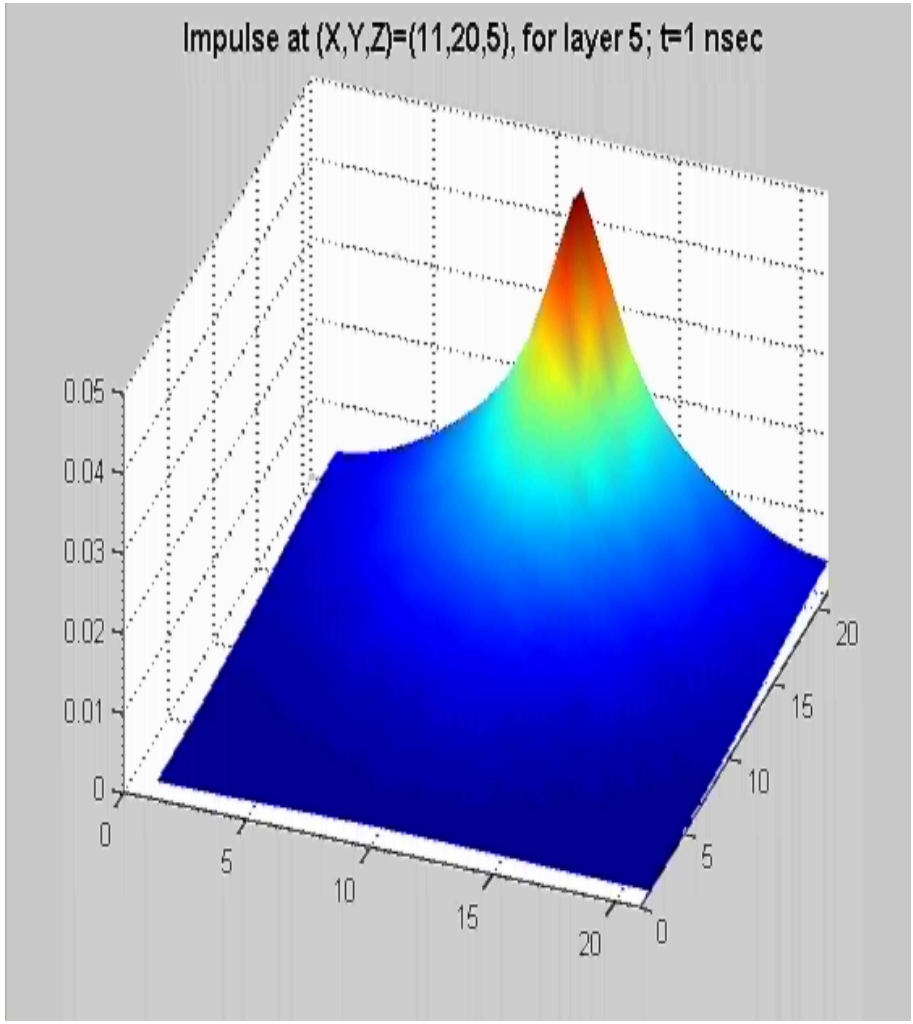
Sample impulse responses shown one layer at a time (click to play; horizontal connections resistive only.):

Layer 5: Note that the north-south resistors are smaller than east-west resistors; hence the uneven response distribution.

Impulse at (1,1,1)

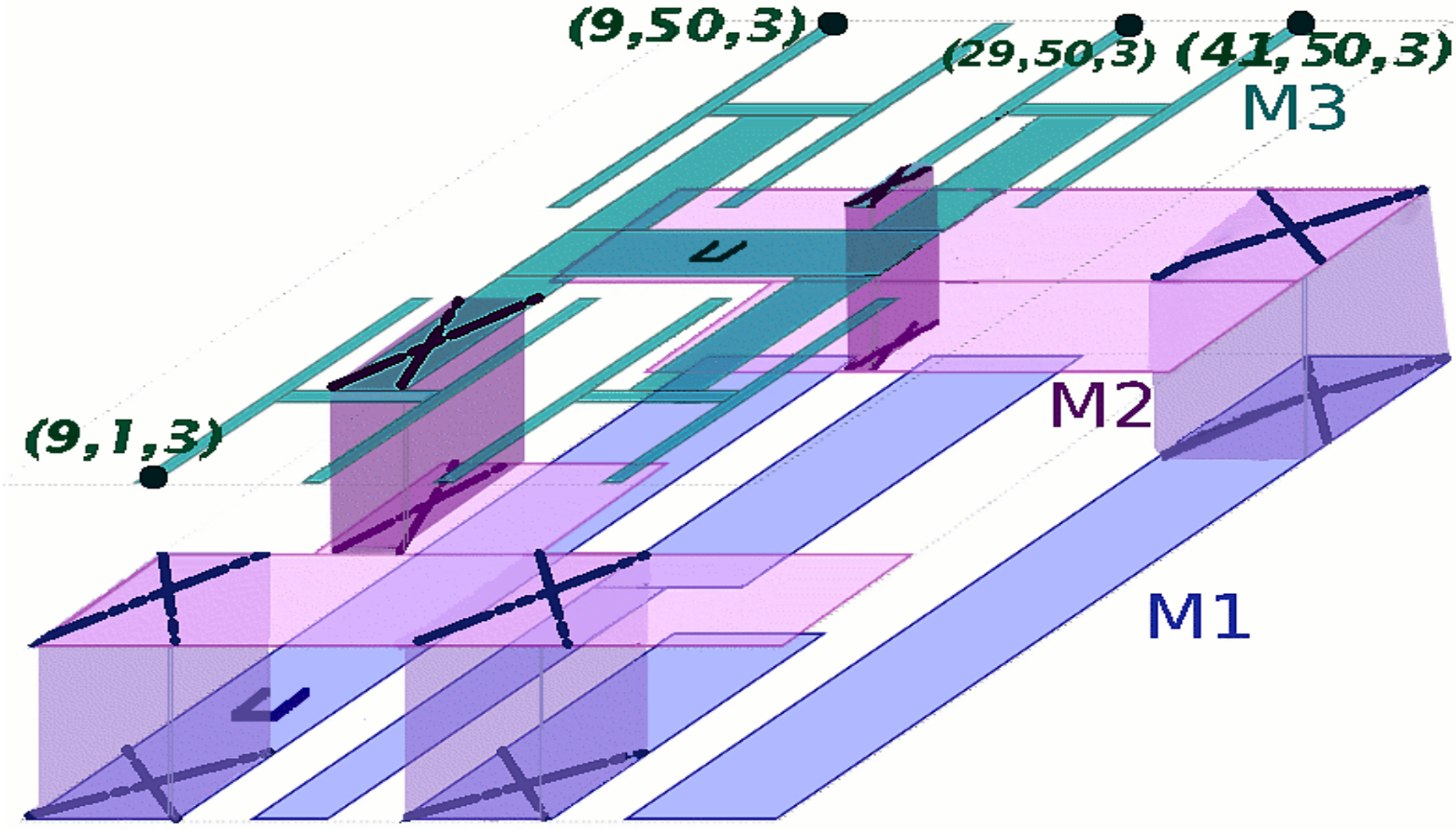


Impulse at (11,20,5)

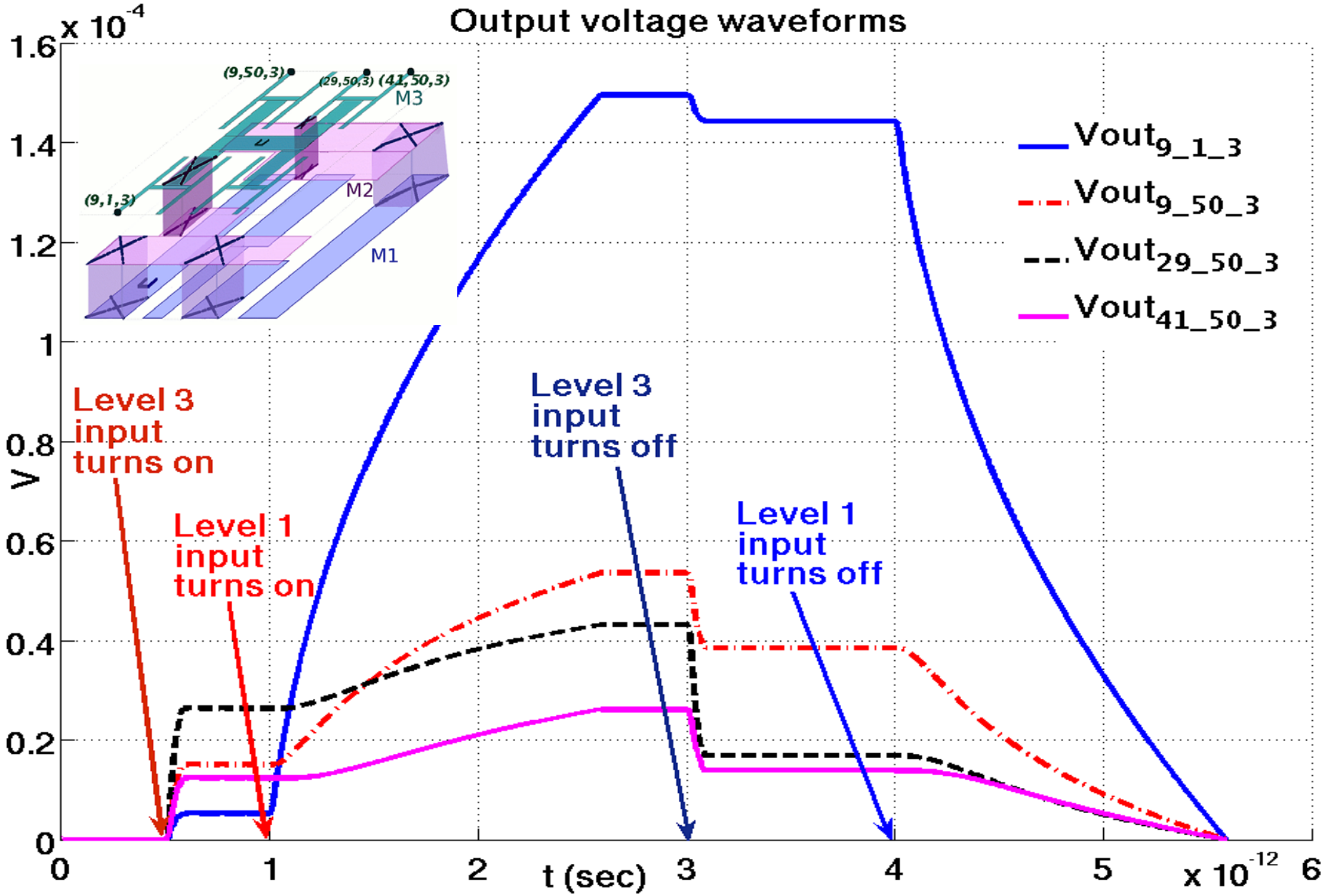


Impulse Response Solver Results: Clock Tree

An example three-metal-layer interconnect network representation. The connections are resistive and/or capacitive as required.



Impulse Response Solver Results: 50x50x3 Mesh



Current work

- The method is flexible enough for mesh expansion; we are investigating computationally efficient ways of solving much larger mesh networks.
- We are developing unit cells modeling physical interconnect structures:
  - With appropriate unit cells, we can investigate the full networks of 3-D integrated chips
  - We plan to use EM modeling tools and S-parameter measurements and extraction
- Example goal application: Determine which locations are most vulnerable for substrate and ground/VDD noise-sensitive subcircuits included in 3-D integrated system with different types of circuit networks on the individual layers (e.g. communication on top layer, data storage in the middle, data processing at the bottom…)

Conclusion

- Developed a method to model and investigate the response of a complex on-chip interconnect network to external RF interference or to internal coupling between different chip regions or subcircuits.
- Computational advantages:
  - Impulse responses calculated once characterize system
  - System response arbitrary input can then be predicted.
  - System response to deterministic, random, Gaussian, etc. can be easily modeled.
  - The same unit cells can be combined for many interconnect layouts; thus flexibility in the systems that can be investigated;

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- X. Shao, N. Goldsman, O. M. Ramahi, P. N. Guzdar, A New Method for Simulation of On-Chip Interconnects and Substrate Currents with 3D Alternating-Direction-Implicit (ADI) Maxwell Equation Solver. *International Conference on Simulation of Semiconductor Processes and Devices,* pp. 315-318, 2003.
- X. Shao, N. Goldsman, and O. M Ramahi, The Alternating-Direction Implicit Finite-Difference Time-Domain (ADI-FDTD) Method and its Application to Simulation of Scattering from Highly Conductive Material, *IEEE International Antennas and Propagation Symposium and USNC/CNC/URSI North American Radio Science Meeting: URSI, Digest*, p. 358, 2003.
- Y. Bai, Z. Dilli, N. Goldsman and G. Metze, Frequency-Dependent Modeling of On-Chip Inductors on Lossy Substrate, *International Semiconductor Device Research Symposium, 2003*, Accepted for publication.
- X. Shao, N. Goldsman, O. M. Ramahi,and P. N. Guzdar, Modeling RF Effects in Integrated Circuits with a New 3D Alternating-Direction-Implicit Maxwell Equation Solver, *International Semiconductor Device Research Symposium, 2003*, Accepted for publication.

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- Dilli, Goldsman, Akturk, "An Impulse-Response Based Methodology for Modeling Complex Interconnect Networks," 2005 International Semiconductor Device Research Symposium (ISDRS 2005), pp.324-325, , December 7-9 2005, Bethesda, MD.
- Dilli, Goldsman, Akturk, Metze, "A 3-D Time-Dependent Green's Function Approach to Modeling Electromagnetic Noise in On-Chip Interconnect Networks," to be presented in 2006 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2006), Monterey Bay, CA.
- Yang, Shao, Goldsman, Ramahi, "Modeling RF Signal Propagation Along On-Chip Interconnect and the Effect of Substrate Doping with Alternating-Direction-Implicit Finite-Difference Time-Domain (ADI-FDTD) Method," 27th Power Modulation Symposium and 2006 High Voltage Workshop (PMC 2006), May 14-18 2006, Washington DC.