Degradation in gate dielectrics and the effects on simple integrated circuit building blocks (SICBBs)

Richard Southwick III\textsuperscript{1}, Bill Knowlton\textsuperscript{1,2} and Jake Baker\textsuperscript{1}

\textsuperscript{1}Department of Electrical and Computer Engineering
\textsuperscript{2}Department of Materials Science and Engineering

Boise State University, Boise, ID
Acknowledgments

University Involvement

STUDENTS:
- Betsy Cheek (G), ECE
- Mike Ogas (UG,G) ECE
- Nate Stutzke (UG), ECE
- Windy Wilson (UG) ECE
- Carrie Lawrence (UG,G), ECE
- Dave Whelchel (UG) ECE
- Patrick Nagler (UG) ECE
- David Jenkins (UG) ECE
- Mark Elgin (UG) ECE
- Dave Estrada (UG) ECE
- Terry Gorseth (UG) ECE
- Josh Kiepert (UG) ECE
- Patrick Price (UG) MSE

FACULTY:
- Amy Moll, ME Faculty

Industry Involvement

- Santosh Kumar, Cypress Semiconductor
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- Dr. Rino Choi, SEMATECH

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Outline

- Statement of Work for Gate Oxide Reliability
- Measurement Techniques Developed
- Circuits Studied Relative to Gate Oxide Thickness
- Alternative Gate Dielectrics
- Future Work
Focus: Gate dielectric/oxide (SiO$_2$) degradation by EM radiation in MOSFETs & Effects on ICs

- Determine degradation mechanisms in gate dielectric due to EM radiation
- Mimic EM radiation-induced degradation in gate oxides using DC techniques
- Determine how gate oxide degradation mechanisms affect simple integrated circuit building blocks
  - Inverters
  - Logic gates: NAND & NOR

To do this: Developed 2 - test and measurement techniques

- **1) Multi-Waveform Pulse Voltage Stressing**
- **2) Switch Matrix Technique**
Techniques for Examining EM Radiation Effects on Devices and Circuits

- **Multi-Waveform Pulse Voltage Stressing (MWPVS)**

- **Switch Matrix Technique**
Continued size reduction in ICs, leads to:

- Very close interconnect proximity
- EM radiation will Capacitive Couple to Interconnects
- Cause noise spiking
- Increase voltage:
  - From: $V_{carrier}$
  - To: $V_{carrier} + V_{EM} = V_{noise}$
Reliability Test Methods

- **RVS** (ramped voltage stress)
  - DC – difficult to extract time dependency

- **CVS** (constant voltage stress)
  - DC - NOT typical for digital circuit operation

- **PVS** (pulse voltage stress)
  - Better mimics digital device behavior

- **MWPVS**
  - Represents circuit operation with noise source such as EM radiation

Diagram:
- **Agilent 81110A Pulse Pattern Generator**
- **Ch 1**
- **Ch 2**
- **O’scope**
- **Agilent 4156C**
- **Probe**
- **Device**
Experimental Results

- Pre- and post- MWPVS \( I_{\text{GATE}}-V_{\text{GATE}} \) results:
  - Degradation mechanisms observed
    - SILC (Stress Induced Leakage Current)
    - SBD and Softer SBD (Soft Breakdown)
    - LHBD (Limited Hard Breakdown)
    - HBD (Hard Breakdown)

Finding: Degradation mechanisms induced by either EM-like pulse voltage stressing or DC stress the same.
Weibull plots indicate device lifetime decreases by orders of magnitudes when compared to preliminary CVS data.

Similar results for lower frequencies.
Initial data indicates that increasing the noise signal decreases device lifetime exponentially†
- $d$, constant proportional to $DC_{BASE}$ of carrier signal
- $d'$, constant proportional to $DC_{SPIKE}$ of noise signal
- $c$, voltage accelerator factor
- $dV$, noise amplitude

Preliminary noise model for a spike voltage with a $DC_{SPIKE}$ of 20%

\[
\frac{1}{t_{bd,noise}} \approx d \cdot e^{c|V|} + d' \cdot e^{c(|V|+|dV|)}
\]

EM Radiation can cause significant reduction in lifetime (over 3 orders of magnitude)

\[
\Delta t_{bd} = \frac{t_{bd} - t_{bd,noise}}{t_{bd,noise}}
\]

\[
t_{bd} = T \cdot DC_{BASE} \cdot P_{bd}
\]

Conclusions

- Designed a MWPVS technique to simulate effects of EM radiation on MOSFETs

- Reliability Issues
  - Constructive Interference occurs due Superposition of waveforms
    - Electromagnetic radiation
    - Capacitive Coupling
    - Mixed Signals

- Device lifetime shorter for EM-like radiation than PVS or CVS

**Data corresponds to the noise model**: Device lifetime exponentially decreases with increase in noise voltage
Techniques for Examining EM Radiation Effects on Devices and Circuits

- Multi-Waveform Pulse Voltage Stressing (MWPVS)
- Switch Matrix Technique (SMT)
Only one other group examining SICBB reliability

They can only perform VTC – a DC technique

- They did not examine time domain
- Cannot determine oxide degradation mechanism
- Why? Because they cannot examine individual MOSFETS

Switch Matrix Technique (SMT)

- Reliability studies - focus mainly on MOSFETS and large-scale ICs.
- Degradation effects in MOSFETs cannot be directly correlated to gate oxide degradation in ICs.

**Answer:** We developed a method that can isolate MOSFET from IC to:
- examine EM-radiation-like oxide degradation in individual MOSFETs
- Induce EM-radiation-like oxide degradation in individual MOSFETs or circuit

**Method:** Switch Matrix Technique (SMT) enables reliability studies at the simple integrated circuit building block (SICBB) level.

Using SMT, reliability studies have focused on the following SICBBs:
- Inverter ($t_{ox}$: 3.2 and 2 nm)
- Transmission Gate (TG not shown)
- NAND ($t_{ox}$: 2 nm)
- NOR ($t_{ox}$: 2 nm)

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Switch Matrix Technique (SMT) - System

- Agilent 41501B SMU and Pulse Generator Unit
- Agilent E5250A Low Leakage Switch Matrix
- Agilent 4156C Precision Semiconductor Parameter Analyzer
- HP 4284A LCR Meter
- Agilent Infinium 54832D 1GHz Oscilloscope
- Metrics ICS Software
- Micromanipulator Probe Station:
  - 8 Cascade Microtech Micromanipulators
  - Faraday Cage
- High Resolution: femtoampere and microvolt
Switch Matrix Technique (SMT) - Experimental Setup

Switch Matrix Technique

Station #1

Station #2

SICBB Circuit

Input A

Input B

Output

VDD
Switch Matrix Technique (SMT) - Addressing Load Capacitance

\[ \Delta t_r \] is within standard deviation when comparing wire bonded NAND circuit and SMT NAND circuit.

Simulation of NOR circuit shows when \( C_{load} \) is decreased, \( \Delta t_r \) percent remains constant.

SMT is a viable technique

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SMT Experimental Procedure

Before stress measurements
Circuit: VTC, V-t, $I_{IN} - V_{IN}$

Device Or Circuit?

Transistor-level
Stress applied to the gate terminal of the device

Circuit-level
+RVS applied to the input node of the circuit

After stress measurements
SICBB Circuit: VTC, V-t, $I_{IN} - V_{IN}$

Data Analysis & Parameter Extraction
Circuit: $I_{IN}$ $V_{OH}$ $V_{OL}$ $V_{SP}$ $V_{Out,MAX}$ $V_{Out,MIN}$ $t_r$ $t_f$
MOSFET: $I_G$, $I_{On}$, $I_{Off}$, $V_{th}$, $g_m$, $S$
SMT – SICBBs Studied

**SICBB: 3.2nm Inverter**
Circuit Level Degradation

![Circuit Diagram](image1)

**SICBB: 2nm Inverter**
Device Level Degradation

![Circuit Diagram](image2)

**SICBB: 2nm NAND Gate**
Device Level Degradation

![Circuit Diagram](image3)

**SICBB: 2nm NOR Gate**
Device Level Degradation

![Circuit Diagram](image4)
3.2nm Inverter VTC and V-t Response

- Time-domain degradation more significant!
  - $\Delta V_{OH} \ll \Delta V_{Out,MAX}$
  - $\Delta V_{OL} = \Delta V_{Out,MIN}$

Increasing Degradation
- Fresh
- LHBD ($P,N$)
- HBD ($P$), LHBD ($N$)
- HBD ($P,N$)
2nm pMOSFET Gate Oxide Degradation ($I_G$-$V_G$)

- Observed gate leakage current increase (2.0 nm)
  - Accumulation mode ~ 2 to 3 orders of magnitude
  - Inversion mode < 1 order of magnitude
2nm Inverter VTC and V-t Response

DC Operation

\[ V_{OUT} (V) \]

\[ V_{IN} (V) \]

- Fresh
- \( V_{SP} \)
- \( V_{OL} \)
- \( V_{OH} \)

Fresh → E level degradation:
- \( \Delta V_{SP} \approx 8\% \) shift left\(^1\)
- Output behavior transitions from 1 to 0

AC Operation

\[ \text{Voltage (V)} \]

\[ \text{Time (a.u.)} \]

- 90\%
- 10\%
- \( t_r \)
- Input Signal
- Output Signal

Fresh → E level degradation
\( \Delta \) rise time\(^1\) ~36\% to 62\%

2nm NAND Gate VTC and V-t Response

- Significant reduction in NAND circuit performance

\[ \Delta V_{SP} \approx 9.0\% \text{ left, } \pm 1.2\% \]
\[ \Delta t_r \approx +64.2\%, \pm 17.5\% \]
\[ t_r = t_{90\%} - t_{10\%} \]

Setting 1-3

\[ V_{\text{OUT}}(V) \]
\[ V_{\text{IN}}(V) \]

\[ V_{SP} \]

\[ V_{\text{SP}} \approx 9.0\% \text{ left, } \pm 1.2\% \]

\[ t_{r} \approx +64.2\%, \pm 17.5\% \]

Approximately $\frac{1}{2} \Delta t_r,_{NAND}$

- Significant reduction in NOR circuit performance
NAND Gate - Potential Circuit Failure

Want: $t_{\text{delay}} < t_{\text{setup}}$

If $t_{\text{delay}} \uparrow$ then output becomes:

Resulting problem:
- Does data get clocked?
- Too much delay $\rightarrow$ fail
SICBB - Conclusions

- Switch Matrix Technique – viable technique
  - Determine degradation in individual devices
  - Ability to connect device degradation to circuit degradation

- Gate Oxides: 2.0 nm more susceptible than 3.2 nm to EM-radiation-like degradation
  - SICBB failure may result at a fairly low level degradation

- VTC measurements may show negligible inverter degradation
  - Suggests Oxide degradation effects in SICBBs are not a reliability issue

- Decrease in logic gate performance, particularly in time domain, directly related to:
  \[ \Delta I_{DRIVE} \rightarrow I_{DRIVE} \propto \frac{1}{R_{CH}} \rightarrow \Delta t_r \propto \Delta R_{CH} \]

- Observed degradation in \( \Delta t_r \) of the NOR gate is about half of that observed in NAND gates
High k Dielectrics to Replace SiO$_2$

Motivation

Leading high k candidate: HfO$_2$

Dielectric Constant: ~25

High k Dielectrics – HfO₂

Many Issues with HfO₂:
- Prompted by SiOₓ interfacial layer (IL)
- Larger number of defects
- Reliability Assessment of IL needed

HfO$_2$ – Preliminary RVS Reliability Testing

- Time-zero dielectric breakdown studies
Future Work: Will use Variable Temperature Probestation

- Custom Design (3+ years in design & development)
  - Temperature Range: 5.5 – 450 K
  - System Pressure: ~10^{-6} Torr

- High Resolution: attoampere and microvolt

- Agilent 81110A 2-channel PPG
- Keithley 595 QSCV
- Keithley 4200 SCS
- Keithley 707A Switch matrix
- Agilent 4284A LCR meter
Future Work: *Will use*

**Variable Temperature Probestation**

- **Cryogenic Temperature Studies**
  - **SiO₂ gate oxides**
  - ✔ Device reliability
  - ✔ Circuit reliability
  - **High dielectric constant reliability**

- **High temp measurements**
  - **Thermal stability**
  - **Reliability: thermal & voltage acceleration**

<table>
<thead>
<tr>
<th>$V_D (V)$</th>
<th>$I_D (\text{A})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$10^{-11}$</td>
</tr>
<tr>
<td>-0.2</td>
<td>$10^{-10}$</td>
</tr>
<tr>
<td>-0.4</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>-0.6</td>
<td>$10^{-8}$</td>
</tr>
<tr>
<td>-0.8</td>
<td>$10^{-7}$</td>
</tr>
<tr>
<td>-1.0</td>
<td>$10^{-6}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$V_G (V)$</th>
<th>$I_G (\text{A})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1.0</td>
<td>$10^{-10}$</td>
</tr>
<tr>
<td>-0.5</td>
<td>$10^{-11}$</td>
</tr>
<tr>
<td>0</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>0.5</td>
<td>$10^{-13}$</td>
</tr>
<tr>
<td>1.0</td>
<td>$10^{-14}$</td>
</tr>
</tbody>
</table>

**pMOSFET: 10 \mu m/125 nm**

- $t_{ox} = 2.0 \text{ nm}$

**Boise State University**

- Knowlton’s Group
- [LTPS 4.19.06]
Thank you

Questions?