Vulnerabilities in Analog and Digital Electronics

Microelectronics and Computer Group
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Vulnerabilities in Analog and Digital Electronics
<u>Overview</u>

The Fundamental Issues:

1) Modern ICs contain millions of transistors and millions of metal interconnects

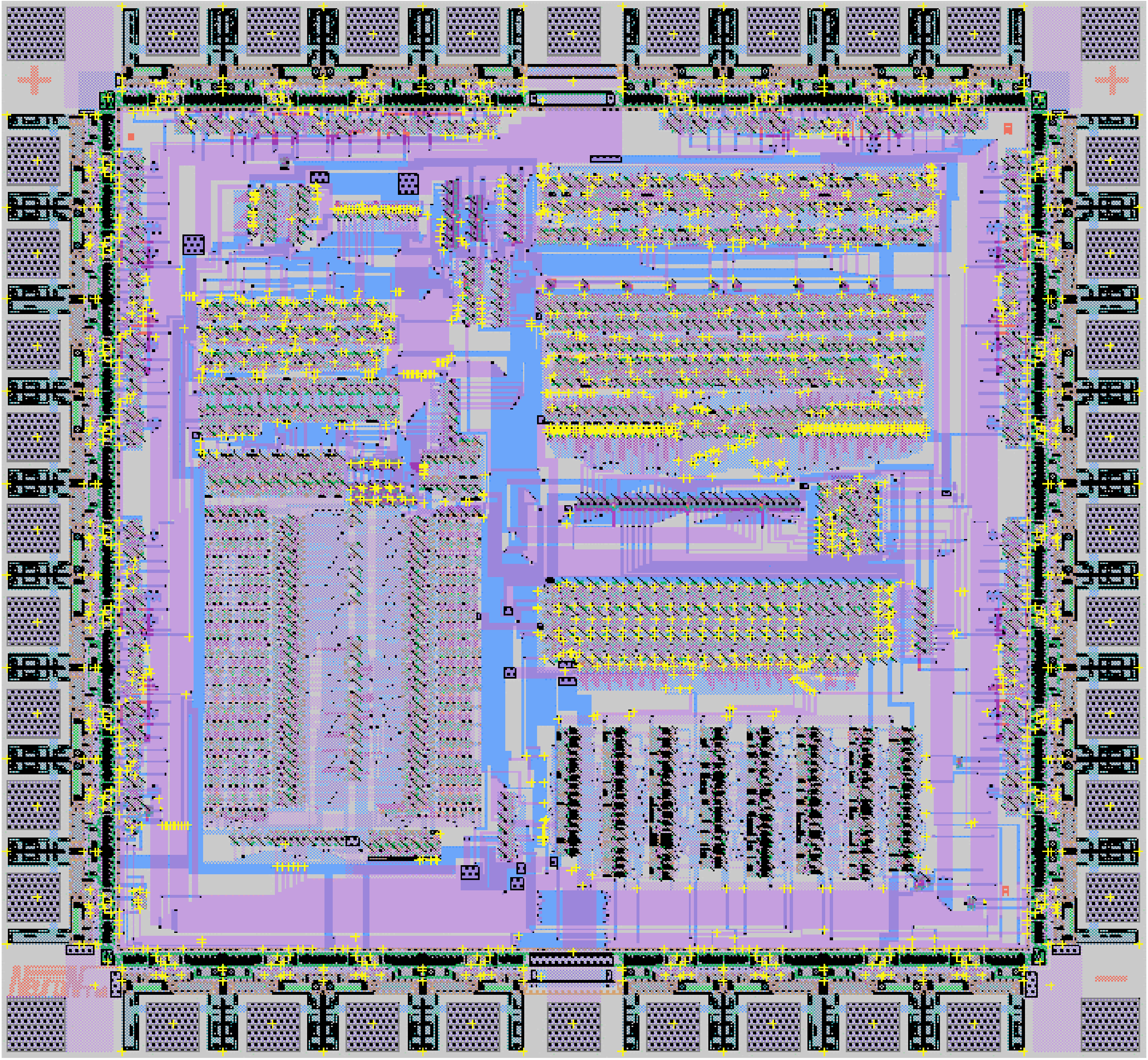
2) Critical dimensions of standard transistors are below 0.1μm with digital voltage levels of 1.0V, leaving very low noise margins.

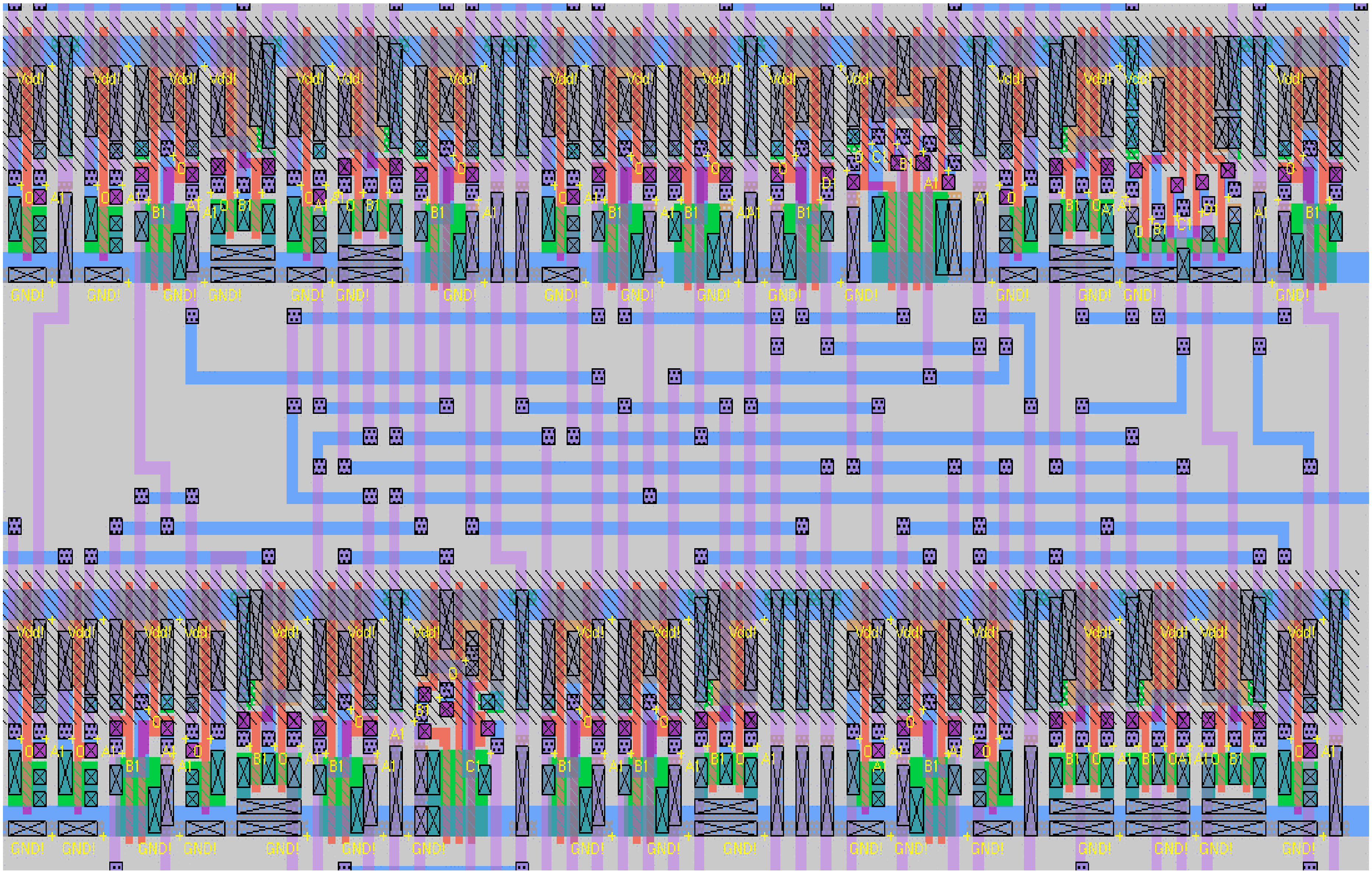
3) Interconnect networks can be highly capacitive and inductive.

4) Such small devices are extremely fragile, especially MOSFET gate oxides which are 0.002μm thick

5) Induced voltages from coupling to external and internal E&M sources can cause circuit errors and permanent damage.

NEURON





Metal 2 interconnect   Metal 1 interconnect

Vulnerabilities in Analog and Digital Electronics
Overview

Circuit Topology Issues:

1) Communication circuits are especially vulnerable.

2) Communication circuit topology typically consists of an antenna, coupled into an LNA at input, followed by a mixer/down-converter, into a demodulator, then a ADC and finally a processor.

3) Each stage has its unique vulnerabilities.
   - -Input LNA especially vulnerable: can overload, jam, etc
   - -Demodulator often contains a PLL, which is subject to phase noise
   - -Processor can introduce bit errors

4) Damage can be temporary or permanent

Vulnerabilities in Analog and Digital Electronics
<u>Presentations</u>

1. Microwave radiation effects in digital data processors
   ------------ B. Jacob
2. On-chip measurement of electromagnetic pulses
   ---------- R. J. Baker
3. Numerical modeling & analysis of nanoscale devices
   ------- N. Goldsman
4. Experimental studies of interference & upset in devices & gates
   ------------ A. Iliadis
5. Diagnostics of upset & damage using focused ion beams
   ---------- J. Melngailis

Numerical Modeling & Analysis of Nanoscale Devices

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Numerical Modeling & Analysis of Nanoscale Devices

<u>Outine</u>

- Introduction
- Modeling Overview
- Numerical Boltzmann/Spherical Harmonic Method
- Results:
  - MOSFET
  - Bipolar Junction Transistor

Numerical Modeling & Analysis of Nanoscale Devices
Introduction

Issues:

- Nanoscale devices are very fragile with gate lengths of 0.1μm and below, and oxide thickness of 0.002μm.
- E&M pulses can couple to device terminals and momentarily alter voltage levels
- Such terminal voltage changes can radically alter I-V characteristics and if large enough, can destroy device though oxide breakdown and/or filament formation related to excessive avalanching.

Use Numerical Modeling of Nanoscale Devices to help understanding and to predict consequences of E&M coupling to terminals, and to present design alternatives for safeguarding against coupling effects.

Numerical Modeling & Analysis of Nanoscale Devices
Goals

Goals:

1) Use advanced semiconductor device modeling tools to understand effects of E&M coupling on nanoscale transistors, especially for rapid coupling to device terminals.

2) Where possible, use existing tools

3) When necessary, develop new tools by adding physics and algorithms

4) Examine E&Ms effect on existing as well as future devices scaled to 25*nm*

5) Extract device circuit models for SPICE to predict how the affected devices will influence circuit operation

Numerical Modeling & Analysis of Nanoscale Devices

Numerical Boltzmann Approach to Semiconductor Device Modeling (Developed at University of Maryland):

Achieves detailed device modeling by self-consistent solution of:

- Boltzmann Transport Equation for Electrons
- Current-Continuity Equation for Holes
- Poisson Equation
- Schrodinger Equation

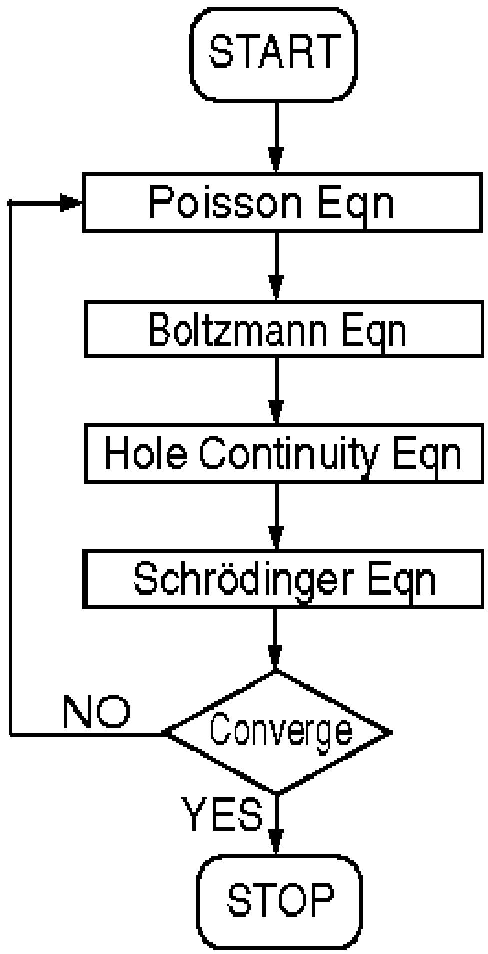
E&M coupling to device terminals can dramatically change boundary conditions of these equations and thus alter the results

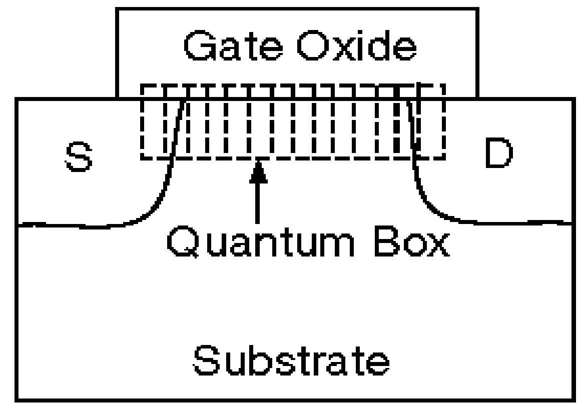
Solution gives the following for the entire device

- Quantum corrected nonequilibrium distribution function
- Electrostatic potential
- From the distribution function, these quantities can be obtained:
  - Terminal currents, electron concentrations, impact-ionization, gate currents

Numerical Boltzmann/Spherical Harmonic Device CAD
Quantum Effects: Schrödinger Results

Mathematical Model

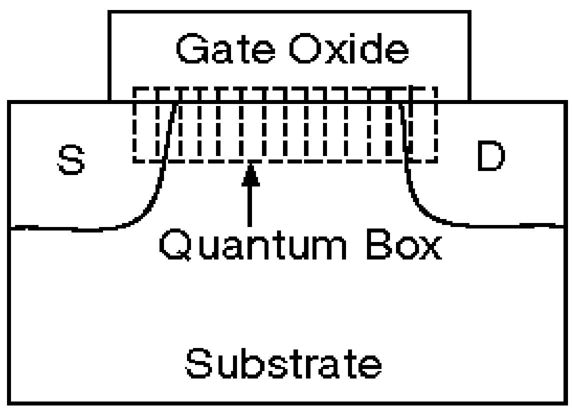




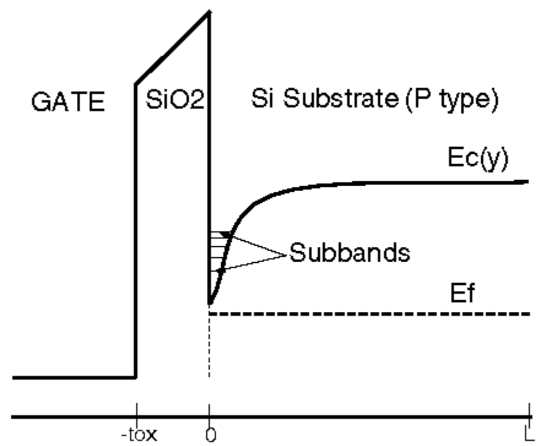
MOSFET CROSS SECTION

Numerical Boltzmann/Spherical Harmonic Device CAD
E&M Influences Quantum Effects: Schrodinger Results

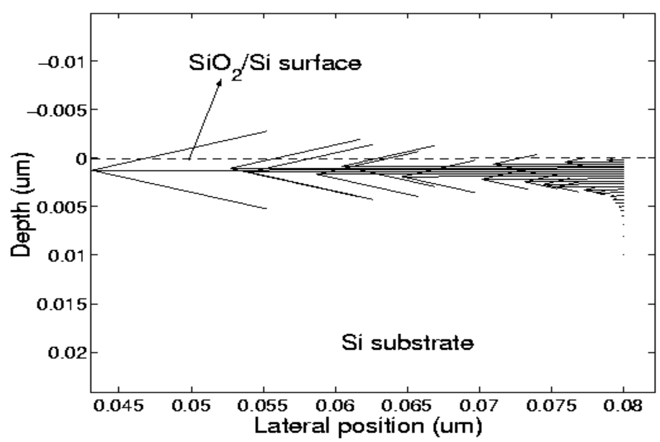
MOSFET Cross Section



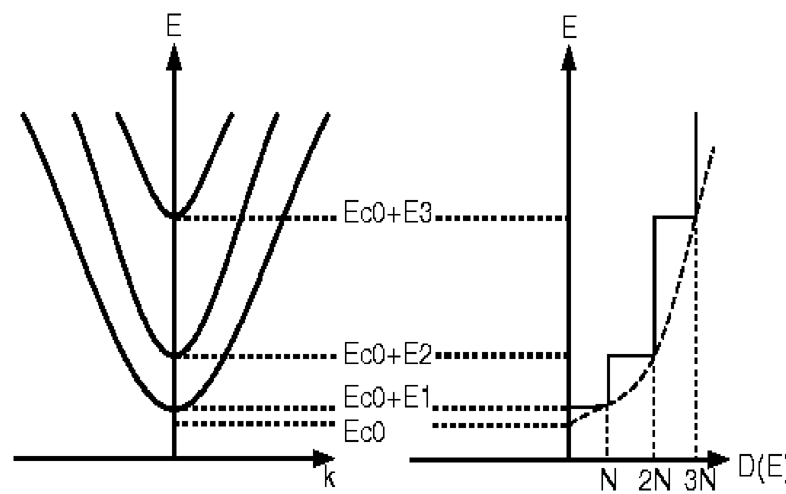
MOSFET QM Confinement Shown



MOSFET Current Density

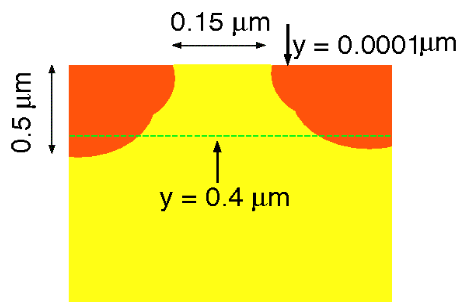


Dispersion Relation of QM Well

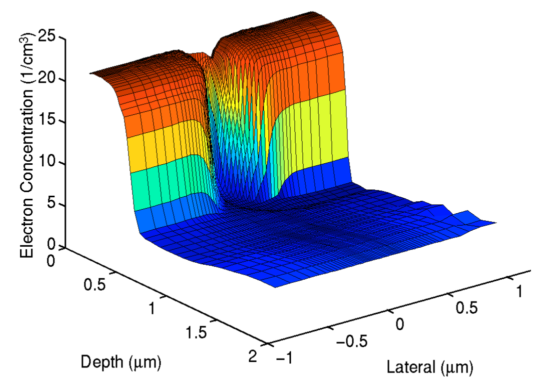


Numerical Boltzmann/Spherical Harmonic Device CAD Results: Device Structure and Distribution Function

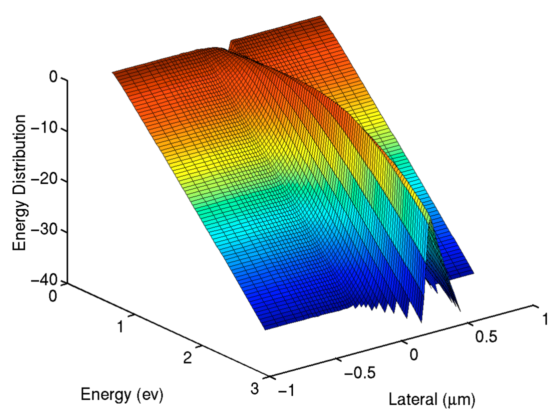
MOS Cross Section



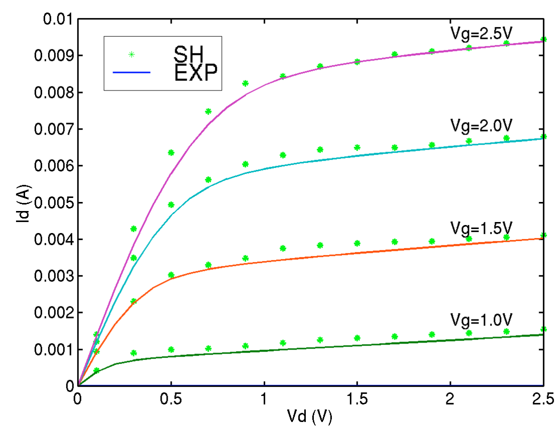
Electron Concentration



Channel Distribution Function



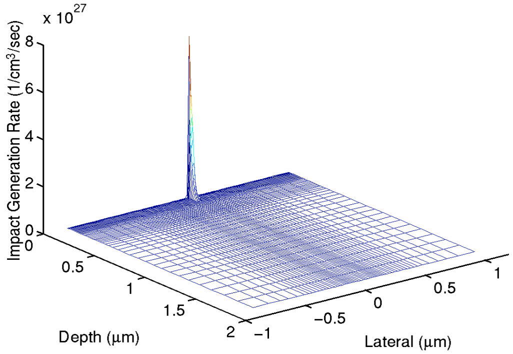
I-V: Agreement



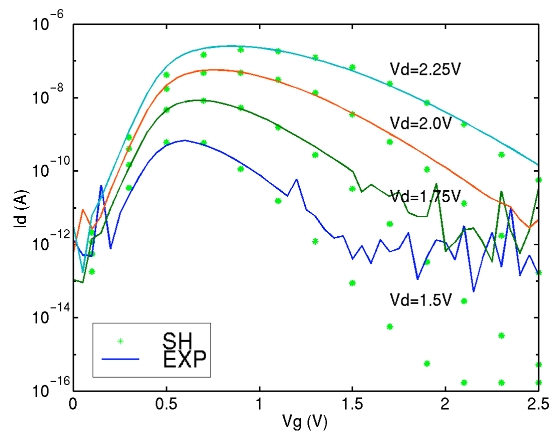
Numerical Boltzmann/Spherical Harmonic Device CAD E&M Coupling can Dramatically Increase: Impact Ionization, Substrate & Gate Currents

Agreement with experiment: No fitting parameters!

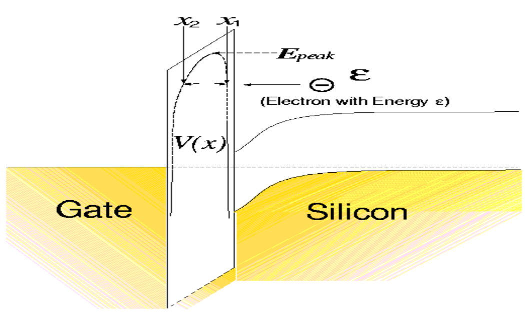
Impact-Ionization Generation Rate



Substrate Current

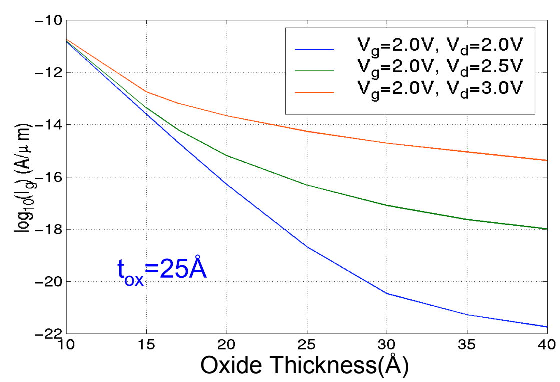


Gate Current Illustration



I_g vs V_g, V_d

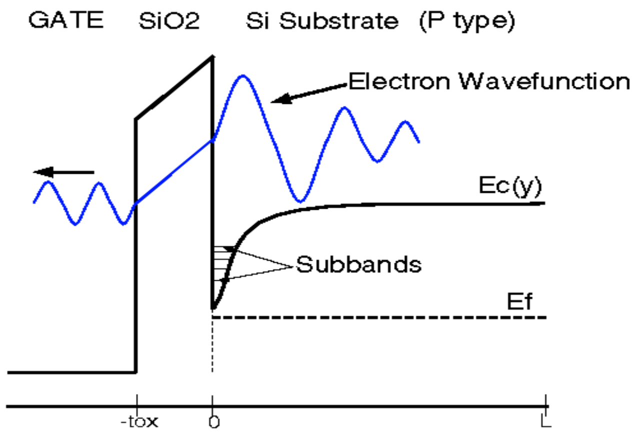
Gate Current



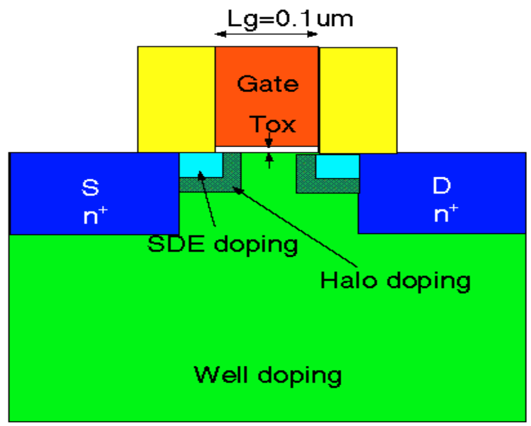
I_g vs Oxide Thickness

Numerical Boltzmann/Spherical Harmonic Device CAD E&M Coupling can Cause More Direct Tunneling Gate Currents

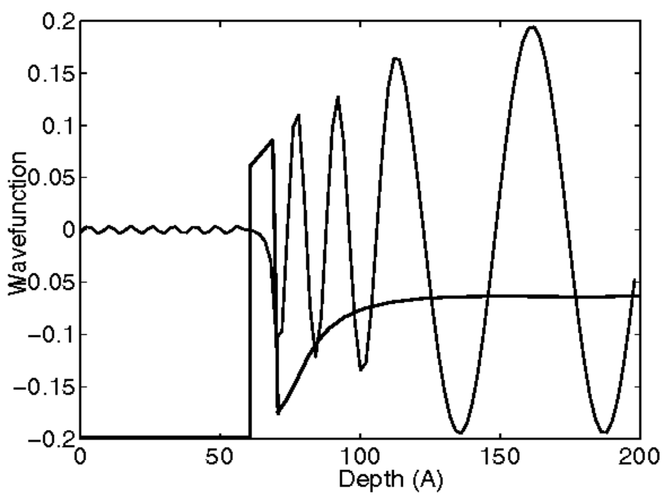
Gate Tunneling Illustration



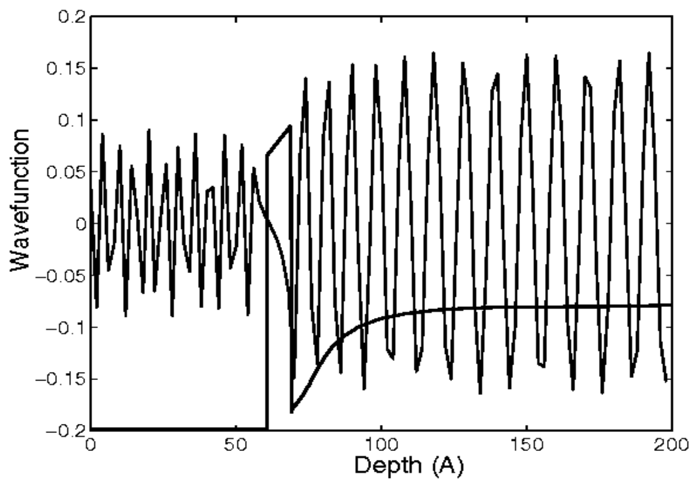
Device Structure



Wave function with lower energy



Wave function with higher energy



Numerical Modeling & Analysis of Nanoscale Devices
BJT Transient

Time-Dependent BJT Simulation

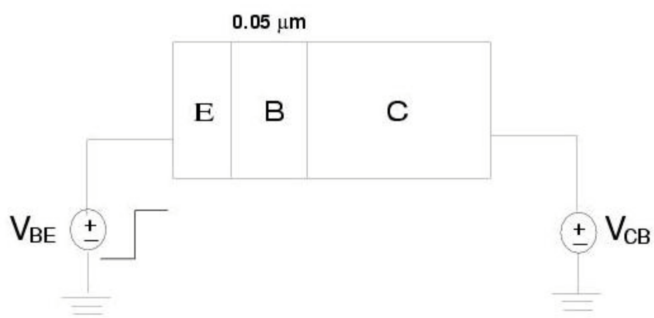
1) 0.75V, 0.1 psec pulse input to BJT base
2) Transient simulation (movie) shows response
   - Field responds in 1.0 psec
   - Carriers respond fully in 20psec
   - Distribution function responds in 20psec

Response demonstrates 20psec limitation in response time.

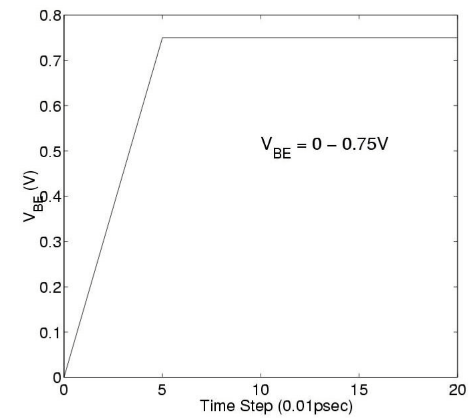
Indicates critical time scales for inducing damage and errors.

Numerical Boltzmann/Spherical Harmonic Device CAD
Quantum Effects: Schrödinger Results

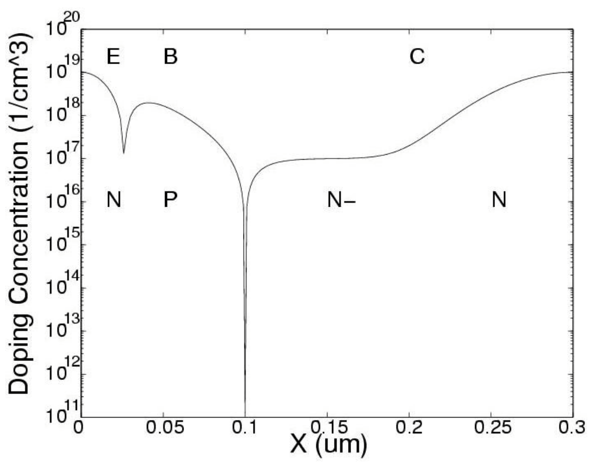
BJT Structure



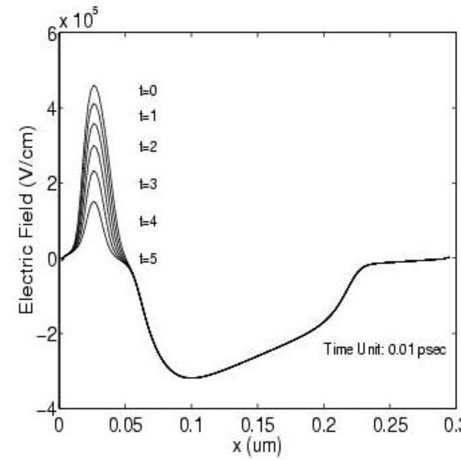
Input Signal



Doping Profile



Electric Field



Numerical Modeling & Analysis of Nanoscale Devices
Summary

1) E&M coupling to device terminals can give rise to unwanted, potentially large and damaging voltage and current variations.

2) Use advanced semiconductor device modeling tools including Numerical Boltzmann method to understand and model effects of E&M coupling on nanoscale transistors

3) Where possible, use existing tools

4) When necessary, develop new tools by adding physics and algorithms

5) Examine E&Ms effect on existing as well as future devices scaled to 25*nm*

6) Extract device circuit models for SPICE to predict how the affected devices will influence circuit operation.