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I. INTRODUCTION / OBJECTIVES

This is the fifth report on the MURI 2001 program, "Effects of high-power microwaves and chaos in analog and digital circuits", being carried out at the University of Maryland, College Park (UMCP) with subcontract to Boise State University. The program was initiated in May 2001. The present report covers the period September 1, 2004 to August 31, 2005. The objective is to study at a fundamental level the effects of high power microwave pulses and chaos in electronic devices, circuits and systems that might lead to upset or damage.

The program at UMCP has the four interrelated parts as follows:

1. Chaos studies, especially wave chaos which provides a statistical description of microwave field in complex topologies such as circuits in boxes;
2. Analysis, simulation and testing of microwave effects on devices, circuits and systems. The testing is primarily in the frequency range 300 MHz to 10 GHz while pulse duration and power level are varied;
3. Custom-design and fabrication of integrated circuits with on-chip microwave diagnostics;
4. Studies of enclosures and shielding.

Progress on each of these topics at UMCP will be reported in the body of this report. A separate report of progress at Boise State University is appended.

III. STATUS OF EFFORT

Our studies in the area of wave chaos have yielded a stochastic formalism, the Random Coupling Model (RCM), for describing the statistical properties of 3-dimensional microwave cavities which can support multiple modes and have a complex geometry including ports and wall loses. Salient predictions of this formalism have now been confirmed experimentally for both the one-port and two-port cases. The two-port studies in particular are enabling one to predict the probability distribution function of electric field on an electronic component inside a partially shielded enclosure from a knowledge of microwave power entering a "port" (such as a cooling vent) and minimal information about the properties of the enclosure (such as cavity dimensions compared with wavelength and cavity Q),; the formalism allows the "target" electronic component to be viewed as the output "port". In recent theory progress, we have developed a code which simulates pulse-modulated signals interacting with chaotic microwave cavities. We have also included in this report a comparison of our RCM approach with the approach for EM modeling in complicated cavities at Sandia National Laboratory; our approach is not limited to 2-D analysis and essentially encompasses all the features of the Sandia model.

We have also included in this report a description of recent progress in circuit chaos studies. In place of the "classical" lumped parameter Resistor-Inductor-Diode (RLD) circuit which has exhibited chaos when excited at relatively low frequencies (kHz to MHz) , we have studied a distributed parameter transmission line terminated in a diode. We have observed chaos in this circuit at driving frequencies in excess of 1 GHz.

Another important aspect of our studies concerns modeling of Electromagnetic (EM) coupling and performance of interconnects in Integrated Circuits (ICs). EM coupling from point to point within integrated circuits causes performance degradation and can lead to failure. In this report we explain work we have done in developing methodologies for modeling these phenomena. The Metal-Insulator-Semiconductor-Metal (MISM) structure is a basic interconnect unit in integrated circuits. A significant feature that sets this work apart form other EM studies is the inclusion of the effects of semiconductor conducting substrates in the analysis, which of course exist on virtually all ICs. Three fundamental modes, namely the dielectric quasi-TEM mode, the slow-wave mode, and the skin-effect mode, have been modeled analytically and

verified by experiment in our early studies of this fundamental IC unit . Subsequent investigators used the conventional Finite-Difference Time-Domain method to analyze on-chip interconnects in two of these modes. However, the analysis was not previously performed on the skin-effect mode until our recent work that is described in this report. In modern ICs, clock rates are above 3GHz, and their harmonics are well into the tens of GHz. In addition, EM coupling from external sources can range well into GHz frequencies. At these frequencies, the MISM structure is operating in the skin-effect mode for the higher substrate doping that is increasingly found in modern nano-scale IC's. Therefore, it is very critical to study wave propagation in this range, as it determines high frequency interconnect losses, which strongly impact the signal integrity.

In experiments on RF effects, we moved beyond our studies of upset in circuits to include studies of effects in systems. The parasitic inductance-diode-conductance model developed previously proved to be very effective at predicting effects in a wide variety of integrated circuits. However, when many thousands or even millions of these circuits are combined into networks and ultimately into systems, the cascaded interaction between many electronic stages could generate new dynamics and upset mechanisms. As a result of the continued decrease in the size of advanced integrated circuits, the margin of error for signal voltages and transient levels have become very small. Consequently, signal integrity and system stability have become critical reliability issues. Circuit controllers and power regulators are often required to provide timing and voltage levels, respectively, with very tight tolerances. In order to achieve a high degree of operating stability, these circuits typically include sensors which feed back status signals to systems regulators. Often, the response of the control loop must be fast (wideband) in order to maintain stability during transient operating conditions. The gain bandwidth of the loop must be restricted (usually with filters) to reject noise and spurious electromagnetic interference (EMI). However, these networks reject signals over a limited bandwidth. . We have found that that some high frequencies pass through the filter with minimal attenuation due to parasitic elements in the network. This effect working in concert with circuit nonlinearity can produce upset in systems at microwave frequencies.

In another set of experimental studies we have focused on identifying the effects of microwave interference signals on the fundamental units of CMOS integrated circuits (IC's) such as individual MOSFETs, single inverters and inverter clusters, and differential amplifiers. We have also sought to develop microwave hardened chips by identifying the vulnerabilities of the elemental IC units, re-designing units accordingly, and introducing on-chip protection using nano-composite coatings.

On the topic of developing on-chip microwave detectors , Focused Ion Beam (FIB) Schottky diode fabrication on a CMOS processed chip was successful A MOSFET power detector circuit was also designed and tested.

Finally, in the area of Enclosures and Shielding, efforts in the past year have been directed at developing electromagnetic band gap (EBG) material or surface for noise mitigation in electronic printed circuit boards (PCB) and for reducing coupling between radiating objects or cavities. While our group has introduced the primary concepts previously (2003), our recent focus was on: (1) miniaturization of EBG structures to enable their practical use in small PBCs and very critically, to allow their use in chip/system packages, and (2) experimental validation of the concept of EBG as surface wave inhibitors to reduce coupling between radiating structures that low impedance links.

Throughout the part of this report dealing with research accomplishments, brief sections have been included which are entitled “Ongoing work and Suggested Future Studies”. Since the current grant terminates on April 30, 2006, much of the important follow-on work that is described will need to be accomplished under alternative sponsorship.

III. RESEARCH ACCOMPLISHMENTS

III.1 Chaos Studies

(Professor Thomas M. Antonsen Jr., Professor Edward Ott, Professor Steven Anlage.
Students: Vassili Dermergis, James Hart, Sameer Hemmady, X. Henry Zheng)

III.1.a Field and Impedance Statistics in Complex Enclosures

We have developed a model for the statistical description of impedance and scattering matrices of complex electromagnetic enclosures. This in turn leads to statistical predictions for electromagnetic field and current distributions at key locations in the enclosure. Our Random Coupling Model (RCM) uses results and concepts from the fields of wave chaos and random matrix theory to make very general predictions. The strength of this approach is that it requires only a bare minimum of information about the enclosure. It hinges on knowledge of the *radiation impedance* (or *radiation reflection coefficient*) of the ingress and absorption routes for the electromagnetic waves (Fig. 1). This information is used to cleanly separate out the effects of coupling in the problem. One can take measured impedance (Z) and scattering (S) matrices and find a normalized impedance matrix z and a normalized scattering matrix s, which show 'universal' properties. The predictive value of the RCM lies in going from the universal matrices back to real Z and S matrices, and the fields.

Figures 1 and 2 illustrate the algorithmic description of our predictive approach, and some representative results. Figure 1 is a flow chart of the algorithm for predicting cavity field distributions. Figure 2 depicts the application of the RCM to a real world problem; viz., predicting the induced voltage PDFs in a computer enclosure in a room.

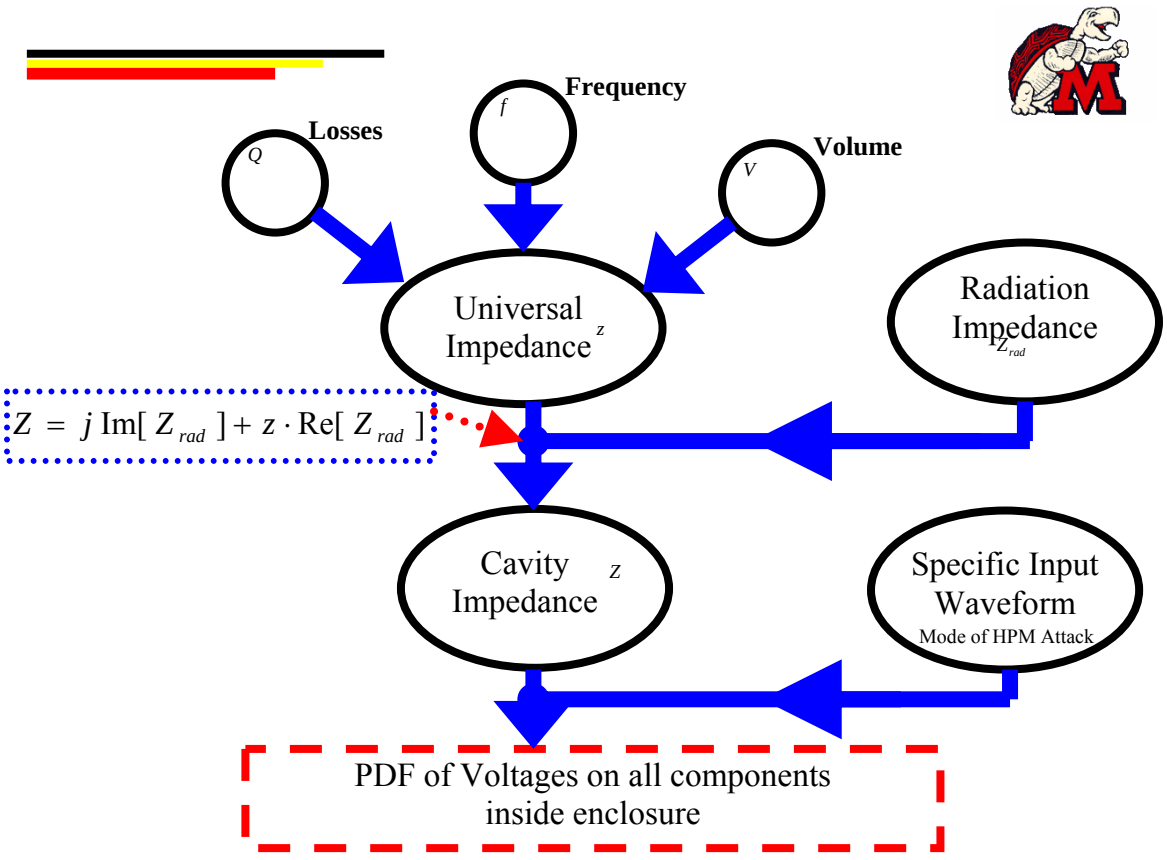


Fig. 1 Flow chart outlining the algorithm to calculate the voltage distributions induced on components inside a complicated enclosure, using only a bare minimum of information: Q, frequency and volume of the enclosure, as well as the radiation impedance of the ingress point and target.

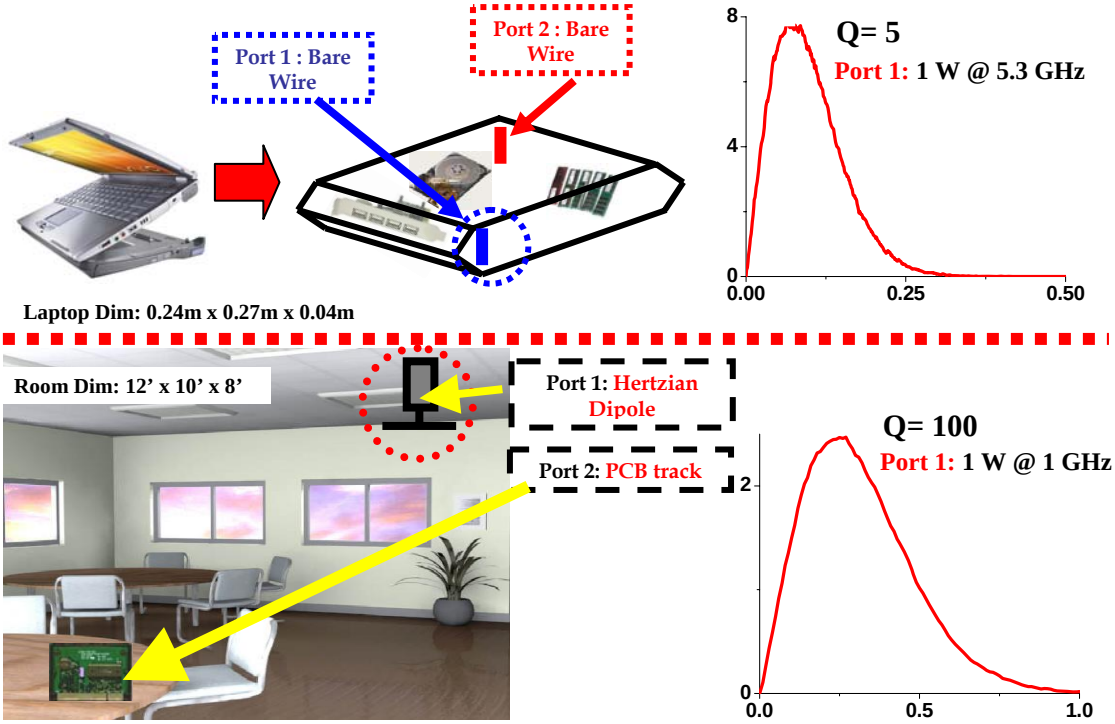


Fig. 2 Examples of the application of our Random Coupling Model (RCM) to real-world problems. The top example shows a computer case in which a 1 W, 5.3 GHz signal is injected by a bare wire and picked up by another bare wire elsewhere in the enclosure. The resulting PDF of voltages induced on the second wire is shown. The lower case is a 1 W, 1 GHz signal created by a dipole antenna, and the resulting voltage PDF induced on a printed circuit board in the room.

We have experimentally tested many basic predictions of RCM using our microwave resonator system. These include the following predictions for 1-port systems:

- ❖ Single-parameter fits to PDF of Re[z], Im[z]
- ❖ Equivalence of variances of PDFs and single fitting parameter
- ❖ Insensitivity of Re[z] and Im[z] to irrelevant details
- ❖ Frequency, volume, loss dependence of Re[z] and Im[z] PDFs
- ❖ Single-parameter fits to PDF of |s|, uniform distribution of Arg[s]
- ❖ Independence of |s| and Arg[s]
- ❖ Fits to the PDF of the cavity reflection coefficient P(R)
- ❖ Developed the procedure to determine the normalized s, z and work backwards to calculate the raw S and Z of a realistic cavity enclosure

All experimental tests are in very good agreement with the predictions of RCM.

For 2-port systems, we have experimentally tested the following predictions:

- ✓ Eigenvalue distribution for the normalized 2x2 impedance matrix z (Fig. 3)
- ✓ Eigenvalue distribution for the normalized 2x2 admittance matrix y (Fig. 3)
- ✓ Re-discovery of the "Hauser-Feshbach" relation for raw S from nuclear physics

- ✓ Development of an improved H-F relation involving the raw impedance Z (Fig. 4)
- ✓ Parameterization of the general S-matrix in terms of 5 independent parameters
- ✓ Measurement of the conductance distribution P(G) for a microwave cavity (see Fig. 5)

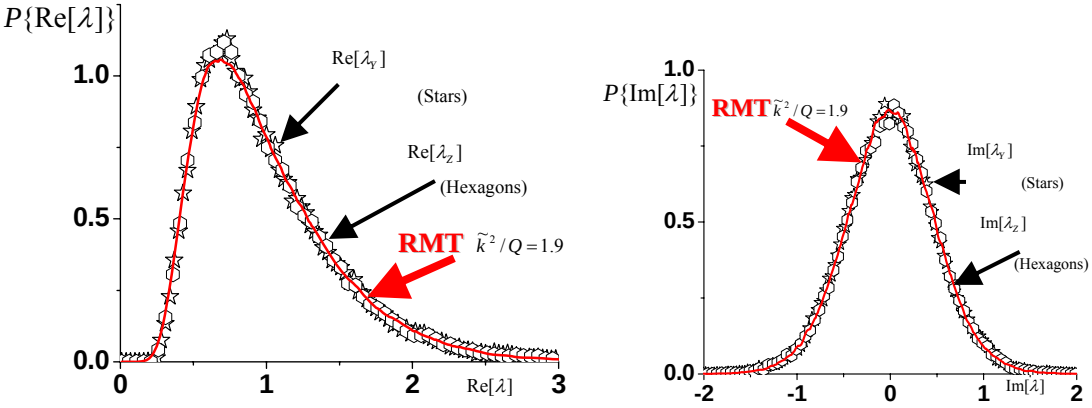


Fig. 3 Distribution functions for the (left) real and (right) imaginary parts of the eigenvalues of the normalized impedance (z) and admittance (y) matrices of a 2-port chaotic microwave resonator. The data is shown for a loss-case 0 resonator at room temperature, between 10.5 and 12 GHz, and a loss parameter $k^{\sim 2}/Q = 1.9$. Note the equality of the distributions for y and z, and un-expected result. Also shown is a random matrix theory calculation in red.

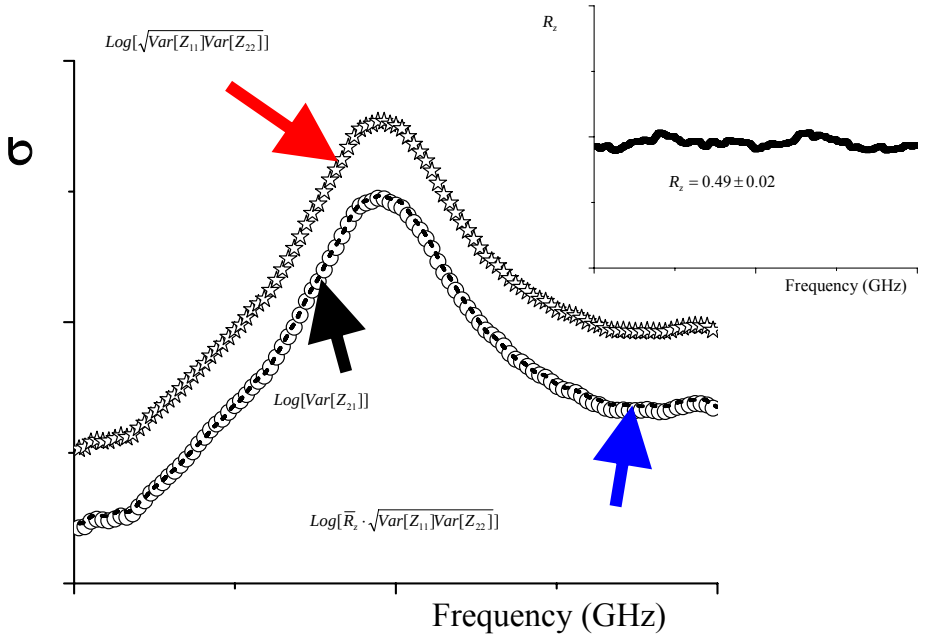


Fig. 4 Measured variance of the impedance distribution Z_{12}, compared to the variances of the Z_{11} and Z_{22} distributions for a wave chaotic microwave cavity between 4 and 12 GHz. We find that the ratio $R_z = [\mathrm{Var}(Z_{11})\ \mathrm{Var}(Z_{22})]^{1/2} / \mathrm{Var}(Z_{12}) = 0.5$ to good approximation, in agreement with our theory. This relation can be used to predict $\mathrm{Var}(Z_{12})$ through reflection measurements of Z_{11} and Z_{22} alone, without the need for a transmission experiment!

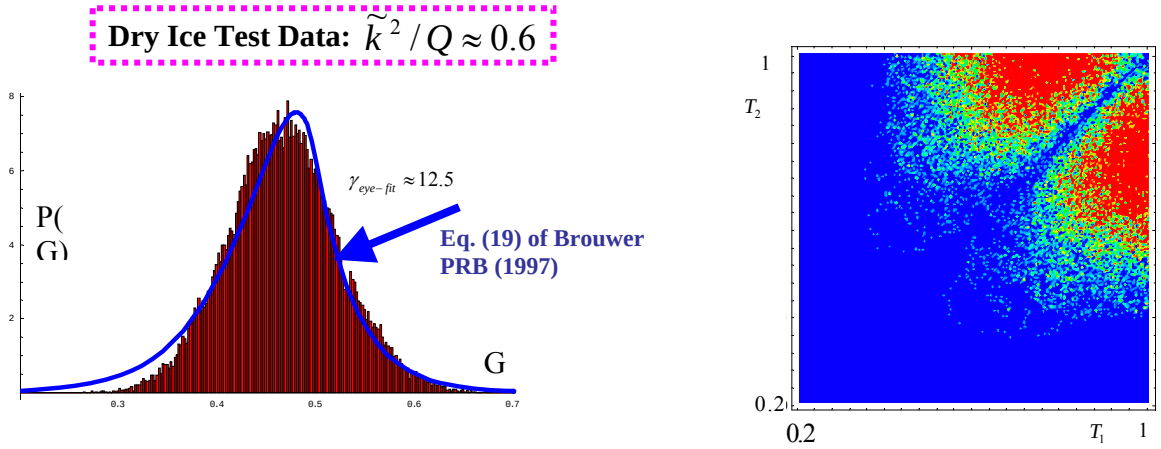


Fig. 5. a) Distribution of conductance values P(G) for a 2-port wave chaotic microwave cavity measured at "dry ice" temperature. The distribution is in fair agreement with theoretical predictions, valid in the high-loss limit, of Brouwer and Beenakker. B) Joint distribution of the eigenvalues of the $SS^{\dagger}$ matrix, T_1 and T_2. T_1 and T_2 measure the lossiness of the absorption channels in the cavity, 0 is no loss, while 1 represents maximum loss. These results are in excellent agreement with the theoretical work of Brouwer and Beenakker.

The successful experimental validation of the RCM opens up the door to applications to problems of direct concern to the Air Force. We can now use the RCM to predict field distributions inside enclosures. For example, Fig. 2 shows an application to a computer enclosure being irradiated by a signal at 2.4 GHz. We can derive the probability density function (PDF) of the voltages induced at any other location in the enclosure that couples to electromagnetic fields, using only a minimum of assumptions.

The RCM gives clear strategies to engineer the field PDFs to prevent damage to circuits, components, etc. On the other hand, it gives clear predictions of 'effects' given a minimum of assumptions about target.

ONGOING WORK and SUGGESTED FUTURE STUDIES

Much remains to be done to test and validate our Random Coupling Model for the description of HPM effects on circuits in complicated enclosures. Some tasks include:

- Describe the statistical aspects of coupling of pulsed signals. This can be done if our AFOSR/DURIP'06 proposal is funded.
- Predict the coupling in complex geometries involving enclosures, circuits and cables.
- Test the RCM for multiple ports in close proximity, and for the case of multiple modes in a single port.
- Investigate the probability of occurrence of unusually intense fields, called 'scars', that are observed on closed ray paths in chaotic enclosures.
- Study the mitigation of large local fields ('hot spots') by addition of nonreciprocal media (magnetized ferrite) to the enclosure.
- Investigate statistical properties of networks formed by transmission line links, which will explore the application of ideas and formalism from quantum chaos to the quantum graph problem.

III.1.b Some Similarities and Differences between the UMD and Sandia Approaches to EM Modeling of Complicated Enclosures

Similarities:

For the single port case, both approaches use the same expression for the system impedance, and make the same assumption regarding the Guassian random variable treatment of the eigenfunctions and coupling. Slightly different assumptions are made about the eigenvalue spacing statistics which yields a small quantitative difference between the two models. Both use the same loss parameter.

The Sandia group does a good job of estimating the asymptotic tails of the distributions for P(Re[z]) and P(Im[z]), the PDFs of the real and imaginary parts of the normalized impedance.

The Sandia group also appears to have a variance expression (Eq. (35) of [1]) similar to ours, but is missing the factor $1/\pi$. This result may be corrected in [2]. They do not derive any result for the case of broken time-reversal symmetry.

Differences:

The Sandia group calculates the scalar input impedance of a one-port mode-stirred chamber, as measured through a single antenna. The UMD model calculates this, but goes much further and treats all objects inside the enclosure. In particular it considers how much energy finds its way from the ingress point to the absorption point (induced voltage, current, etc.). The Sandia approach seems to be mainly concerned with the classical problem of predicting electric field amplitude distributions inside an empty box, without regard for what is in the box, other than the fact that it has ray chaos. Our approach explicitly considers the "target" object through the use of multi-port expressions for impedance, scattering matrix, etc. In our approach, nearby objects affect the matrix radiation impedance by giving it correlations.

To construct the normalized impedance, we use the measured frequency-dependent radiation impedance, whereas the Sandia group seems to normalize with single values of R and X. As a result they only show results in Ref. [2] over very narrow frequency ranges (5 or 10 MHz wide at 200 to 900 MHz). Our approach provides normalized impedance data over the continuous range 600 MHz to 12 GHz, for example (this can be expanded as well). Thus we are in a position to gather large quantities of data for statistical analysis.

Our approach includes the effects of time-reversal symmetry-breaking.

Our approach explicitly works out the multiport case, which leads to qualitatively new and different predictions not available to a 1-port model.

Our work makes connections to theoretical work that derives both approximate and exact analytical forms for the PDFs of Re[z] and Im[z], as well as the reflection coefficient.

Our work also deals with the **scattering matrix** of an N-port system. We established the one-port S-matrix statistical properties in a published paper [Sameer Hemmady, Xing Zheng, Thomas M. Antonsen, Edward Ott, and Steven M. Anlage, "Universal Statistics of the Scattering Coefficient of Chaotic Microwave Cavities," Phys. Rev. E 71, 056215 (2005)], and the 2-port statistics in a paper submitted to Phys Rev. E and available at http://arxiv.org/abs/cond-mat/0504196, as well as papers in preparation. The latter paper also presents data on the approximate S_{12} variance ratio discovered by the ONERA group, as well as our exact Z_{12} variance ratio, which is derived from our model.

We have also extended our analysis and measurements to include the following:

1) We find that the statistics of the real and imaginary parts of the admittance are identical to that of the impedance.
2) We find that the statistical properties of the eigenvalues and eigenfunctions of the measured multi-port scattering matrix are in detailed agreement with theory.

3) We have related the results of two-port experiments, which simulate the full HPM effects problem, to the transport properties of mesoscopic conductors. This opens the door to a tremendous body of theoretical literature which can be applied to the HPM effects problem.
4) We have developed and numerically tested a time-domain version of our model that deals specifically with pulsed-excitations, like those put out by HPM weapons.

Our model in not restricted to 2D and is not restricted to structures where the Schrödinger-Helmholtz analogy holds.

The Sandia model has a different approach to the problem which is complimentary to ours (they look at "wall impedance," internal electric fields, tails of distributions, etc.), but we do not think that they have anything that is not already essentially contained in our model.

We firmly believe that further basic research on a quantum/wave chaos approach to this problem will result in more deep insights, resulting in qualitatively better engineering solutions, to the HPM effects problem.

[1] L. K. Warne, *et al*., IEEE Trans. Antenn. Prop. 51, 978 (2003).
[2] L. K. Warne, W. A. Johnson, R. E. Jorgenson, Sandia Report SAND2005-1505.

III.1.c Advanced Theoretical Studies of Chaotic Microwave Cavities

A code has been developed which simulates pulse-modulated signals interacting with chaotic microwave cavities. Results have been found which give power law time decay exponents of the output power that results from situations in which pulse modulated signals are incident on chaotic microwave cavities.

Universal properties of the variance ratios of the frequency domain fluctuations of impedance matrices for the case of chaotic scatterers have been discovered.

In collaboration with the experimental group, the random coupling model has been further developed and the results have been applied to experimental data on impedance and scattering matrices of two-port chaotic microwave cavities. These experiments are described above in section III.1.a.

ONGOING WORK and SUGGESTED FUTURE STUDIES

Ongoing studies on which progress is expected by the end of the current grant on on April 30, 2006 include the following:
- Development of the theory and carry out numerical simulations on time-domain aspects of reflection of pulse modulated microwave signals from chaotic microwave cavities.
-Further development of the random coupling model application to multi-port microwave experiments and application of the results to ongoing experiments
-Use of the HFSS code to perform simulation tests of random coupling model for the case in which there is near field coupling between ports and/or multimode incoming channels.

Suggestions for follow on studies include the following:
-Deviations from random matrix theory In all out previous work we have used results from random matrix theory (RMT). The applicability of RMT presupposes that the wavelength is small compared with the characteristic system scales, and that all trajectories are strongly chaotic. Deviations from RMT have been observed in some of our preliminary studies, and we believe we might be able to characterize these

using a theory based on geometric optics with short ray paths. This appears to be an important issue for further study.

-Statistics of scars. Another area of interest not described by RMT is the occurrence of 'scars', regions along periodic orbits where anomalously large fields occur. While previous theory exists for this phenomenon, no work has been done for the case with losses and/or ray splitting. Given the danger of large electric fields causing upset, such studies may be very productive.

-Wave chaos on graphs. Many systems can be regarded as involving wave interactions in which the waves propagate along a limited number of well-defined paths. As a paradigm of this situation, a network of branching, interconnected transmission lines possibly joining a number of simple components. In such cases techniques from quantum chaos (including RMT) can be applied, and we are well prepared to do this. Application to complex systems of connected elements, and comparison to experiments by S. Anlage's group would be important goals.

III.1.d Inducing Chaos in Distributed Transmission Line Diode Circuits

The p/n junction is well known for its nonlinear properties – from voltage dependent capacitance and nonlinear current-voltage characteristics, to the memory and reverse recovery effects of the minority carriers. These nonlinearities make p/n junction diodes ideal for creating circuits that demonstrate chaotic behavior and yield chaotic waveforms.

The nonlinear dynamics of the driven, lumped-element series resistor-inductor-diode (RLD) circuit have been thoroughly studied, and the key physical phenomena giving rise to chaos in this classic p-n junction system are essentially understood. It has been established that the nonlinear capacitance as well as the reverse recovery time of the diode both play important roles for the development of chaos.

It has been found that chaos and period doubling in the lumped-element series RLD circuit is best understood by examining the time scales in the problem. First, period doubling and chaos occur for driving frequencies near the resonant frequency of the system:

$$f_0 \approx \frac{1}{\sqrt{L \times C_j(0)}},$$

where L is the value of the inductor element and $C_j(0)$ is the junction capacitance of the diode measured at 0 volts. It was also found that the reverse recovery time of the diode (τ_{RR}) should also be on the order of the driving period: $\tau_{RR} \approx f_0^{-1}$.

Generally, the reverse recovery time of packaged diodes is in the range of about 10^{-2} to 10 μs. Consequently the frequencies associated with generating chaos are low (kHz to MHz range). There has been a growing need to understand the origins of chaos in electrical circuits at higher frequencies. In modern computer electronics, operational frequencies of devices are in the 100 MHz to 10 GHz range. It is in this range in which we intend to generate and understand chaos.

The potential for nonlinearity and chaos in modern computer circuits has already been demonstrated. Electrostatic discharge (ESD) protection diodes are integrated into almost all electronic devices as a means of protecting the logic circuits from potentially destructive outside signals and high-voltage discharges. Parasitic inductance and capacitance associated with the diodes and their packaging can create nonlinear RLD circuits that resonate at GHz frequencies. It has been shown that through out-of-band excitation, these systems can be driven into nonlinear behavior and possibly chaos at GHz frequencies [See our annual report of Sept. 2004]. These chaotic signals could then be transmitted into the primary circuitry and disrupt, or possibly damage, the device.

Our approach is to develop a generalized version of the driven RLD circuit to generate chaos at RF and microwave frequencies. Essentially, the inductor is replaced with a distributed transmission line, thus introducing a new memory/feedback mechanism on the diode.

Here, the distributed, driven, nonlinear diode will be treated as a generalization of the classic, lumped RLD circuit. The addition of a transmission line introduces a new time scale associated with the delayed feedback of the reflected and re-reflected waves. We also consider a variable impedance mismatch between the generator and the transmission line, so the value of the reflection coefficient ρ can be changed in a controlled manner. This system also serves as a realistic model of the ESD diode problem in modern computer circuits and opens up new opportunities to generate chaos at GHz frequencies with relatively simple and ubiquitous systems.

The model in Fig. 6 shows a harmonically driven, distributed, lossless transmission line terminated with a diode. It is important to note that the impedances of the source and transmission line are mismatched so that the wave reflected off the diode can be linearly re-reflected at the source boundary.

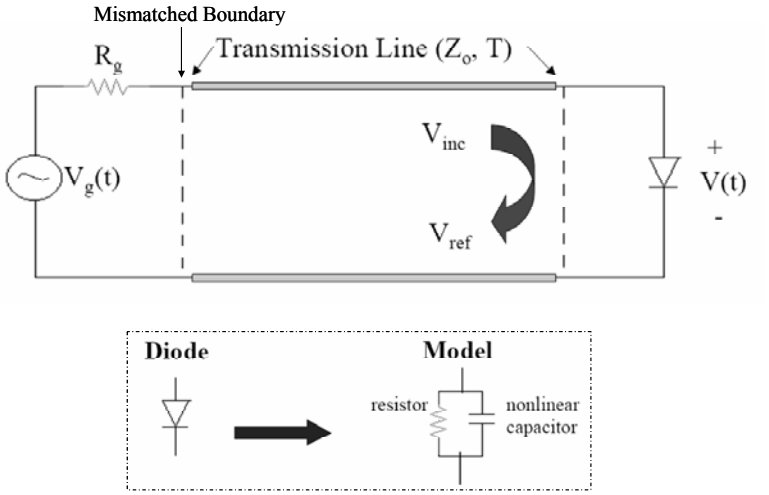
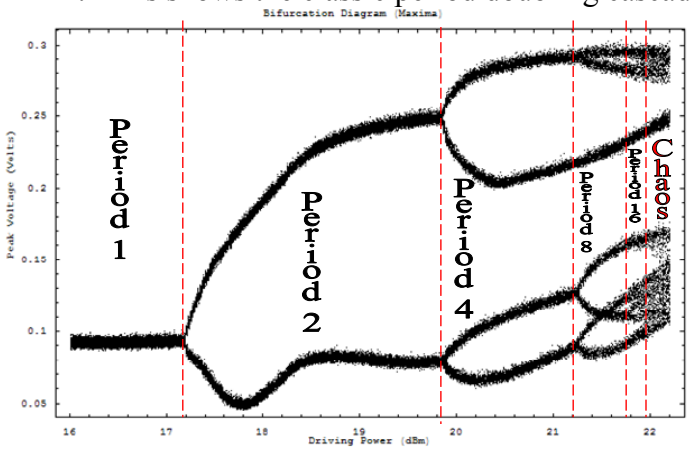


Fig. 6 Schematic diagram of the model of the driven, lossless, diode-terminated transmission line. Shown in the inset is the equivalent electrical schematic model of the diode.

Figure 7 shows an experimental bifurcation diagram on the BAT41 diode transmission line circuit driven at 85 MHz. This shows the classic period doubling cascade to chaos.



Bat41
Length1 = 0m
Length2 = 0.7m

Recycled Power
10dB Directional Coupler
800-1000MHz Circulators
100-600MHz Power Combiner
No Amplifier

Data &Analysis
Frequency = 85MHz
Power Step = 0.01dBm
Source = HP 83620B
Oscilloscope= Agilent Infiniium DSO81204A @ 20GS/s

Fig. 7 Experimental bifurcation diagram; BAT41 diode, *f*=85MHz, T~3.9ns.

Figure 8 shows a set of bifurcation diagrams and spectra at 353 MHz demonstrating the creation of chaos from a circuit like that in Fig. 6. Here the DC bias on the junction is changed, as it would be in a real HPM attack, and the resulting increase in chaotic dynamics is observed.

1N4148
L1=0.0m
L2=0.7m
T ~ 4.4ns

Bias={10,5,2,0,-1,-2}V

f = 353.4 MHz

100-600MHz Power Combiner
10dB Directional Coupler
0.8-1Ghz Circulators

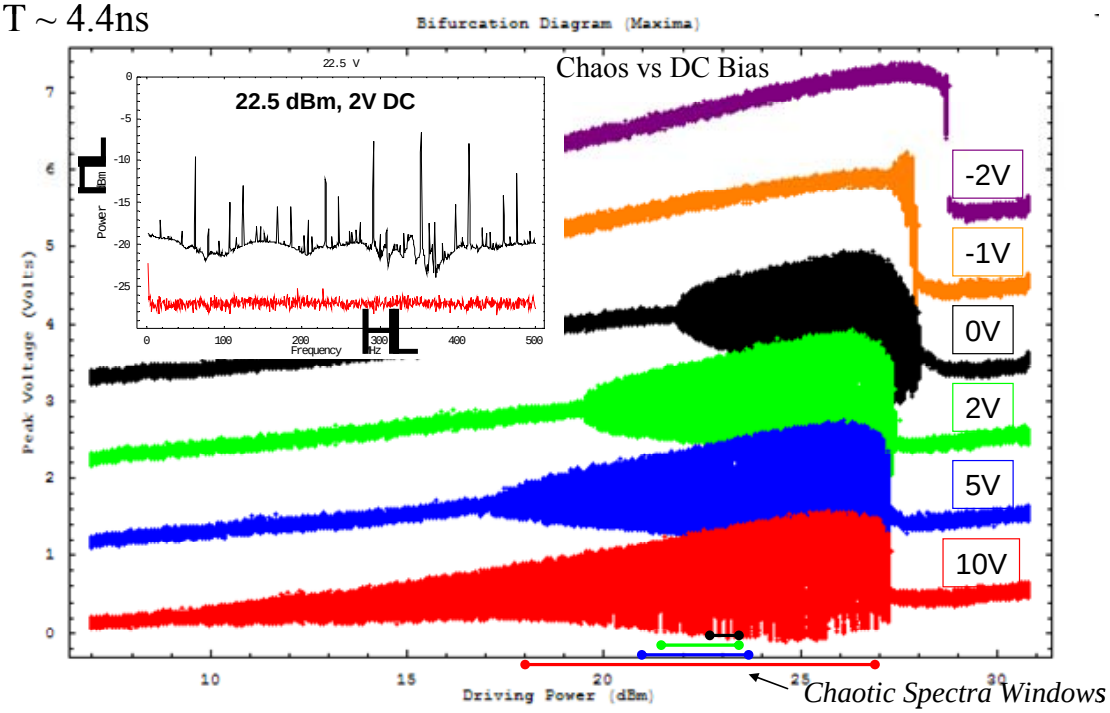


Fig. 8 Experimental bifurcation diagrams taken at different DC bias voltage values on the diode. The solid horizontal lines underneath the bifurcations represent the driving powers of chaos for each bias voltage (from top to bottom: 0V, 2V, 5V, 10V). The chaotic frequency spectrum of the 2V case driven at +22.5 dBm is inset. The system parameters are: f=353.4 MHz, 1N4148 diode, bent-pipe experiment, T~4.4ns.

ONGOING WORK and SUGGESTED FUTURE STUDIES

We have now observed chaos in this driven transmission line diode circuit at driving frequencies up to over 1 GHz. We are continuing detailed measurements and simulations of this circuit and plan to submit a paper for publication before the end of 2005. We are also about to acquire a high-speed sampling oscilloscope (with the help of an AFOSR DURIP'05 grant) to further improve the measured bifurcation diagrams and return maps. Further experiments are planned to elucidate the generality and applicability of these ideas to real-world electronic systems.

Another objective is to seek external support for this work. We have been using internal Center for Superconductivity Research funds for the past 1+ year to fund the student performing this research.

III.2 Microwave Effects on Electronics

(Professor Neil Goldsman, Professor Victor Granatstein, Professor Agis Iliadis, Professor Bruce Jacob, Professor Omar Ramahi, Dr. John Rodgers.

Students: Vincent Chan, Cagdas Dirik, Todd Firestone, Kyechong Kim, Laise Parker, Bo Yang)

III.2.a Modeling of Electromagnetic Coupling in Integrated Circuits

Electromagnetic (EM) coupling from point to point within integrated circuits causes performance degradation and can lead to failure. In this report we explain work we have done in developing methodologies for modeling these phenomena. Our work is focused EM coupling and performance of interconnects on integrated circuits (ICs). The Metal-Insulator-Semiconductor-Metal (MISM) structure is a basic interconnect unit in integrated circuits. A significant feature that sets this work apart form other EM studies is the inclusion of the effects of semiconductor conducting substrates in the analysis, which of course exist on virtually all ICs. Three fundamental modes, namely the dielectric quasi-TEM mode, the slow-wave mode, and the skin-effect mode, have been modeled analytically and verified by experiment in early studies of this fundamental IC unit [1]. Subsequent investigators used the conventional Finite-Difference Time-Domain (FDTD) method to analyze on-chip interconnects in two of these modes. However, the analysis was not performed on the skin-effect mode because of the computational overhead required to satisfy the Courant–Friedrichs–Lewy (CFL) stability limit [2]. In modern ICs, clock rates are above 3GHz, and their harmonics are well into the tens of GHz. In addition, EM coupling from external sources can range well into GHz frequencies. At these frequencies, the MISM structure is operating in the skin-effect mode for the higher substrate doping that is increasingly found in modern nano-scale IC's. Therefore, it is very critical to study wave propagation in this range, as it determines high frequency interconnect losses, which strongly impact the signal integrity.

To investigate the skin-effect mode in digital IC's, we apply the Alternating-Direction-Implicit Finite-Difference Time-Domain (ADI-FDTD) method, because it is not limited by the CFL condition [3]. The ADI-FDTD is especially suited to solving problems in digital ICs which have fine physical scales much less than the wavelength at the higher frequency of operation.

To the best of our knowledge, this is the first time the ADI-FDTD method is applied to analyze on-chip MISM structures. In our work, we first obtained a quasi-analytical solution of the mode equations to generate a frequency-doping map. The map gives the attenuation factor (α), and the phase constant (β), as a function of frequency and silicon doping. We then compare the attenuation factor and the phase constant, obtained from the map in the various modes, with ones that we obtain from the ADI-FDTD method. In addition to illustrating the critical physical aspects of the interconnect, this serves to help validate and verify the accuracy of the ADI-FDTD method. We then use the ADI-FDTD method to investigate the signal propagation characteristics along 4-layered Metal-Insulator-Semiconductor-Metal (MISM) structures. This work extends the numerical analysis from the slow-wave and the dielectric quasi-TEM mode, to the skin-effect mode. In addition, it provides details of the losses in the semiconductor substrate and the metal interconnect.

Quasi-Analytical And Numerical Analysis: Procedures And Results

We performed our analysis on the MISM structure. Fig.1 shows the side view of the MISM structure.

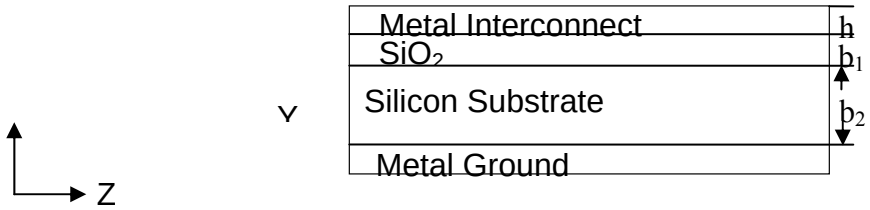


Fig. 1. Side view of the MISM structure. Z is the direction of propagation. h, b_1, and b_2 is the thickness of the metal layer, the SiO_2 layer, and the silicon substrate, separately.

Quasi-Analytical Analysis and 3-Mode Limits

The MISM structure gives rise to a 4 layered boundary problem. In the quasi-analytical analysis, we neglect the metal thicknesses, and extend the line width to infinity. We use Perfectly Electric Conductor (PEC) boundary conditions for the top and bottom metal layers. The equations for the longitudinal and the transverse propagation constants have been derived previously [1], and are written below:

$$\gamma_i^2 + \gamma^2 = -k_0^2 \mu_i \varepsilon_i^{'} \quad i=1,2 \qquad (1)$$

$$\sum_i \frac{\gamma_i}{\varepsilon_i^{'}} \tanh(\gamma_i b_i) = 0 \quad i=1,2, \qquad (2)$$

where γ_1 and γ_2 denote the transverse propagation constants (y direction) in SiO_2 and Si layers, respectively, and γ is the longitudinal one (z direction). Here, $\gamma = \alpha + j\beta$, where α is the attenuation factor, and β is the phase constant. k_0 is the wave number in free space, and $\varepsilon_i' = \varepsilon_i + \sigma_i/(j\omega\varepsilon_0)$, i=1,2. ε_0 and μ_0 are the permittivity and permeability in the vacuum, respectively. We solve this set of coupled non-linear equations using the Newton-Raphson method. The resulting attenuation factors and the phase factors on the frequency-doping plane are shown in Fig. 2. In the figure, three bold lines divide the map into 3 fundamental mode regions, and a transition region. The characteristic frequency for the skin-effect in the Si substrate is $f_\delta = 1/(2\pi)\cdot 2/(\mu_0\sigma_2 b_2^2)$, the dielectric relaxation frequency in the Si substrate is $f_e = 1/(2\pi)\cdot\sigma_2/(\varepsilon_2\varepsilon_0)$, and the characteristic frequency of slow-wave mode is $f_0 = (f_s^{-1} + 2/3\cdot f_\delta^{-1})^{-1}$. $f_s = 1/(2\pi)\cdot\sigma_2/(\varepsilon_2\varepsilon_0)\cdot(b_1/b_2)$. The location of these edge lines depends on both the geometrical factors (b_1,b_2), and the electrical factors (σ_2,ε_1,ε_2). The conductivity and the doping density transform comes from [4].

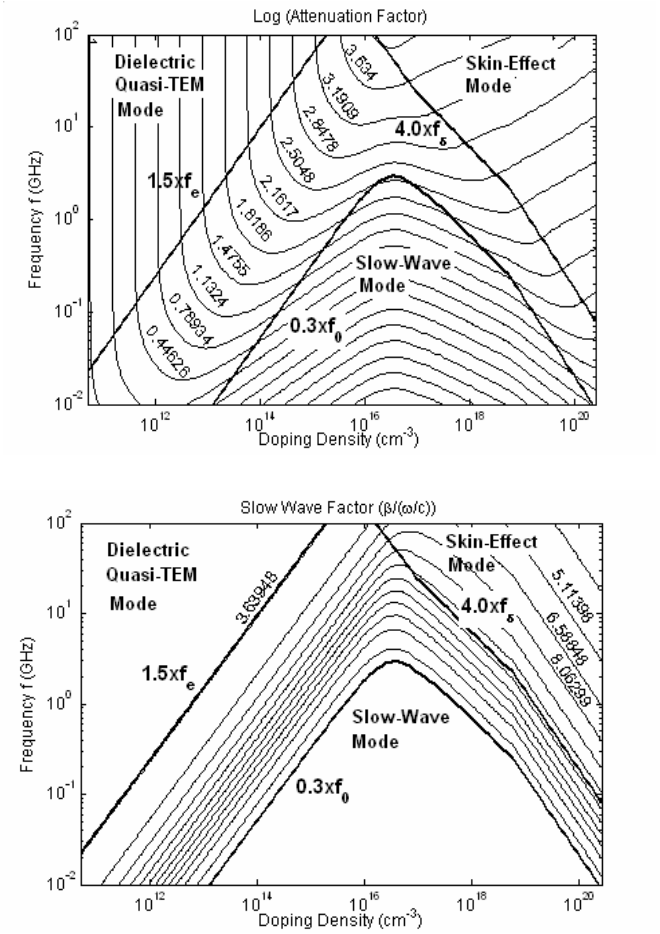


Fig. 2. For the MISM structure, b_1=2μm, b_2=200μm. The three bold lines divide the map into 3 regions of fundamental modes as marked. Top figure: contour of attenuation factor α (along propagation direction z) vs. substrate doping and wave frequency. Bottom figure: contour of normalized phase constant β/(ω/c) (along propagation direction z) vs.
substrate doping and wave frequency.

Numerical Analysis: Extracting Propagation Modes and Constants

We next use our ADI-FDTD simulator to analyze the structure in Fig. 1. In contrast with the quasi-analytical approach, here we account for the thickness of the metal interconnect. The metal line is excited at one end; Mur's 1st absorbing boundary condition [5] is applied on the open region, and the PEC boundary condition is added on the ground plane. We consider a MISM structure with h=1.8μm, b_1=2μm, b_2=200μm, and the metal conductivity to be $\sigma_{Al}=3\times10^7 S/m$. A sharp Gaussian pulse with time constant τ = 8.83 ps (bandwidth is 50GHz) is used as the excitation waveform. 82 grid points are laid out along the y direction with the minimum grid size of 0.1μm inside the oxide and the metal layers; 29 grid points in the y direction are laid out in the upper free space region; 240 uniform grid points are laid out along the z direction with $\Delta z = 150um$. For the traditional FDTD, Δt_{FDTD} must be less than 3.3×10^{-16} s to satisfy the CFL stability limits. In our simulation, the time step is $\Delta t_{ADI\text{-}FDTD}$ 2×10^{-13} s, which is an acceptable choice according to [3]. $\Delta t_{ADI\text{-}FDTD}/\Delta t_{FDTD}$ = 600. This helps to calculate the field distribution in the very thin silicon skin depth region in the skin-effect mode, and the field distribution in the metal layer in all three modes of propagation.

From the ADI-FDTD solution we extract the attenuation factor and the phase factor, as a function of frequency and semiconductor doping. This is achieved by applying the Gaussian pulse in the time domain

as described above, and then taking the Fourier transform. The propagation constants extracted from ADI-FDTD electromagnetic field time domain solutions are shown in Fig.3 for a frequency range of 1GHz to 50GHz, and the substrate dopings of $8.9x10^{11}cm^{-3}$, $8.9x10^{16}cm^{-3}$ and $6.9x10^{19}cm^{-3}$. The curve corresponding to a doping of $6.9x10^{19}cm^{-3}$ represents operation in the skin-effect mode. The curve corresponding to a doping of $8.9x10^{11}cm^{-3}$ represents propagation in the dielectric quasi-TEM mode. The middle range curve, with doping of $8.9x10^{16}cm^{-3}$ reflects propagation ranging from the slow-wave mode to the transition mode, and then to the skin-effect mode as the frequency increases. In the skin-effect mode, the loss is higher, and the phase velocity is relatively large, whereas in the dielectric quasi-TEM mode, they are both relatively small constant. The numerical results in each case also match the quasi-analytical calculations.

C. Numerical Analysis: Calculating Field Distributions in Mixed Dimensional Structures

To further understand the energy flow and distribution in each mode, a comparison of the field distributions obtained from the ADI-FDTD full-wave results is made. In Fig.4 (a)-(c), the sine wave with the frequency of 60GHz is excited on the MISM with doping = $1.0\ x10^{20}cm^{-3}$, and the field is taken at t=40ps. The skin-depth mode field distribution is observed as expected. In Fig.4 (d)-(f), a sine wave with frequency of 1GHz is excited on the MISM structure with doping = $8.9x10^{16}cm^{-3}$; the field is taken at t=1ns, and the slow-wave mode field distribution is shown. In Fig.4 (g)-(i), a sine wave with frequency of 4GHz is excited on the MISM with doping = $1.8x10^{13}cm^{-3}$, and the field is taken at t=0.6ns, and the dielectric quasi-TEM field distribution is shown. The field is normalized to the field in the oxide layer in each of the 3 cases. In the last two modes, in order to show at least one period of the wave pattern, we elongated the interconnects to 60 mm, which is larger than their actual on-chip length. In the skin-depth mode, the field in the Si substrate is concentrated close to the SiO_2-Si interface, with an equivalent skin-depth of 10 to 20μm; whereas in the dielectric quasi-TEM mode, the field penetrates through the Si substrate. In the slow-wave mode, although the field extends all the way down to the substrate, its magnitude is orders less than the field in the SiO_2 layer. This implies that relatively little energy penetrates into the Si substrate. In our numerical simulation, we show that in the skin-effect mode, the field in the metal layer is concentrated close to the Al-SiO_2 interface with a skin depth of less than one micrometer (for the case considered here). In the other two modes, the field is distributed more evenly in the metal layer, the skin depth is larger.

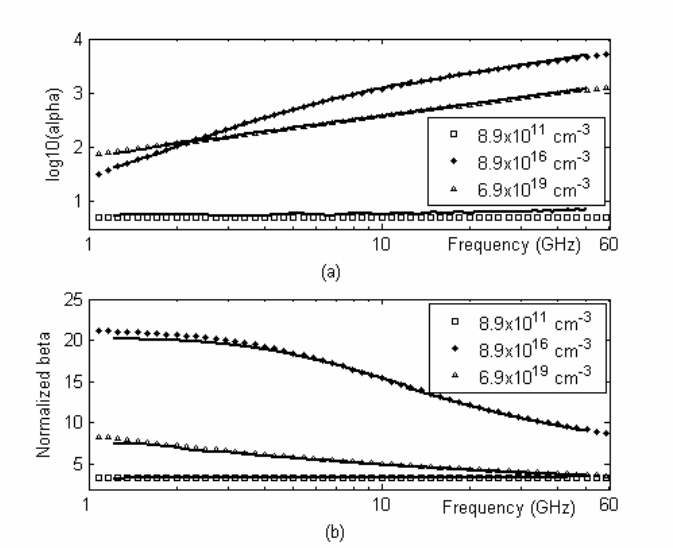


Fig. 3. Propagation constant versus frequency and doping density for the quasi-analytical and ADI-FDTD numerical analysis. b1=2μm, b2=200μm. The lines with markers are the quasi-analytical results, and the solid lines are the numerical results: (a) attenuation constant in log scale (b) normalized phase constant.

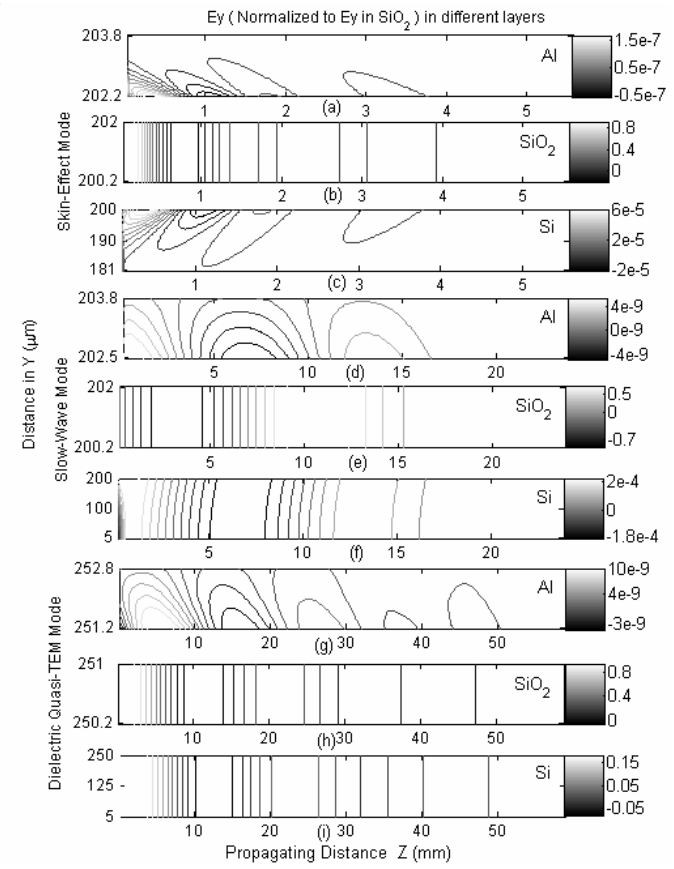


Fig. 4. Ey distribution in different layers in 3-mode: (a)-(c) skin-effect mode, h=1.8 μm, b1=2μm, b2=200μm, doping = $1x10^{20}cm^{-3}$, t=40 ps, f=60 GHz; (d)-(g) slow-wave mode, h=1.8 μm, b1=2μm, b2=200 μm, doping = $8.9x10^{16}cm^{-3}$, t=1 ns, f=1 GHz; (h)-(i) dielectric quasi-TEM mode, h=1.8 μm, b1=1μm, b2=250 μm, doping=$1.8x10^{13}cm^{-3}$, t=0.6 ns, f=4 GHz.

ONGOING WORK and SUGGESTIONS for FUTURE STUDIES

We reported above on the implementation of the ADI-FDTD method to extend the investigation from the slow-wave and the dielectric quasi-TEM modes into the skin-effect mode. The propagation loss, the dispersion, and the skin-depth is examined over different substrate dopings in the frequency range from 1GHz to 50 GHz. The instantaneous field distribution is also analyzed in our work. Future studies should use this work to pave the way for accurate prediction of substrate losses and coupling of more complicated on-chip interconnect and doping structures, a characterization that is becoming increasingly critical for the design of high-speed interconnects.

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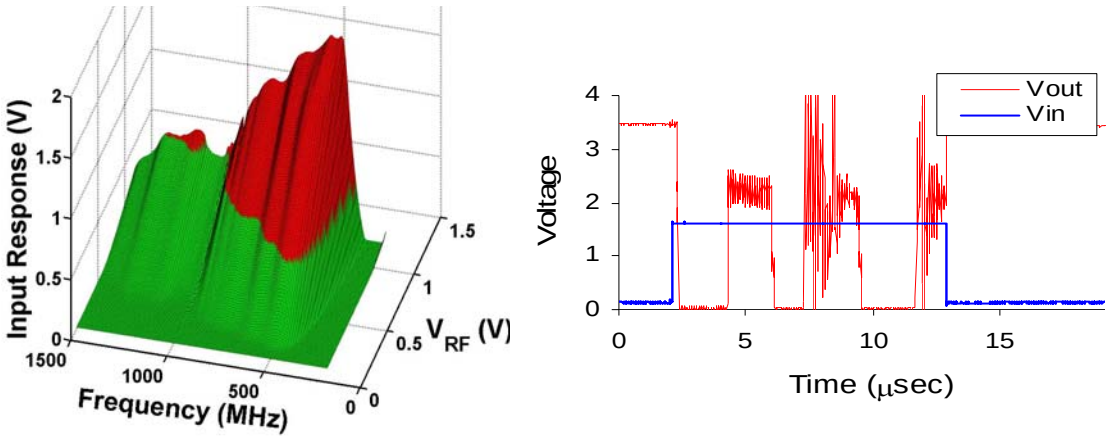
III.2.b Effects in Circuits and Systems from High Power Microwave Pulses

Our previous work focused on RF effects on the integrated circuit level. There is reasonable concern about the threat to electronics imposed by high-power microwave (HPM) sources with waveforms of a very complex nature. RF effects from microwave pulses whose amplitude is less than the operating voltages in integrated circuits were studied extensively at the University of Maryland [1-2]. This work showed that high-frequency parasitic resonances and on-chip ESD protection devices in integrated circuits had resonant frequencies in the microwave regime with quality factors as high as seven. When excited near resonance, these elements produced gate voltages at the input transistor that were higher than the amplitude of the RF pulse. These studies resulted in a comprehensive effects model based on these parasitic elements working in concert with the characteristics of electrostatic protection devices in integrated circuits. The networks cause upset and instability in circuits when driven by out-of-band carriers with wideband modulation. Figure 1 shows an example of the input and output response in advanced, low-voltage CMOS when excited by microwave pulses with such modulation. The figures show that circuits can exhibit complicated dynamics that may lead to bit errors, oscillation and undefined logic states.



(a) (b)

Fig. 1 Example of the measured response in high-speed CMOS integrated circuit showing (a) voltage gain characteristics due to parasitic resonances, and (b) the instability in the output voltage caused by microwave pulses.

Studies of Systems-Level Microwave Upset

In 2005, we extended our research concentration to include studies of effects in systems. The parasitic inductance-diode-conductance model developed previously proved to be very effective at predicting effects in a wide variety of integrated circuits. However, when many thousands or even millions of these circuits are combined into networks and ultimately into systems, the cascaded interaction between many electronic stages could generate new dynamics and upset mechanisms. Thus, a thorough investigation of system

effects was commenced in 2005. In the following, a brief summary of this work is presented.

As a result of the continued decrease in the size of advanced integrated circuits, the margin of error for signal voltages and transient levels have become very small. Consequently, signal integrity and system stability have become critical reliability issues. Circuit controllers and power regulators are often required to provide timing and voltage levels, respectively, with very tight tolerances. In order to achieve a high degree of operating stability, these circuits typically include sensors which feed back status signals to systems regulators. Often, the response of the control loop must be fast (wideband) in order to maintain stability during transient operating conditions. The gain bandwidth of the loop must be restricted (usually with filters) to reject noise and spurious electromagnetic interference (EMI). However, these networks reject signals over a limited bandwidth.

Figure 2 shows the results of RF transmission measurements on a low pass filter. It can be seen that some high frequencies pass through the filter with minimal attenuation due to parasitic elements in the network. This effect working in concert with circuit nonlinearity can produce upset in systems at microwave frequencies. Figure 3 shows a schematic of a typical feedback amplifier with protection diodes at the input, and Fig. 4 shows the results of measurements of the amplifier output voltage when the circuit was irradiated by an RF pulse with a carrier frequency of 1.7 GHz and wideband amplitude modulation. Even though the gain-bandwidth was designed to be approximately 100 MHz, the microwave pulse caused the circuit to become so unstable that the output deviation was enough to clip the output at the negative supply voltage (-9V). If this were to occur in a power-regulating amplifier, the protection circuitry would shut the system down.

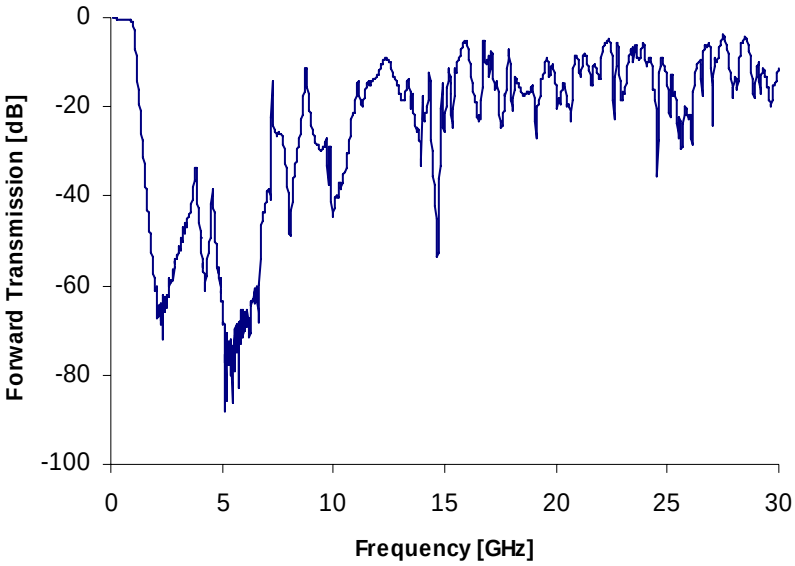


Fig. 2 Transmission coefficient of a low pass filter showing that component parasitics a cause spurious passbands to appear at microwave frequencies.

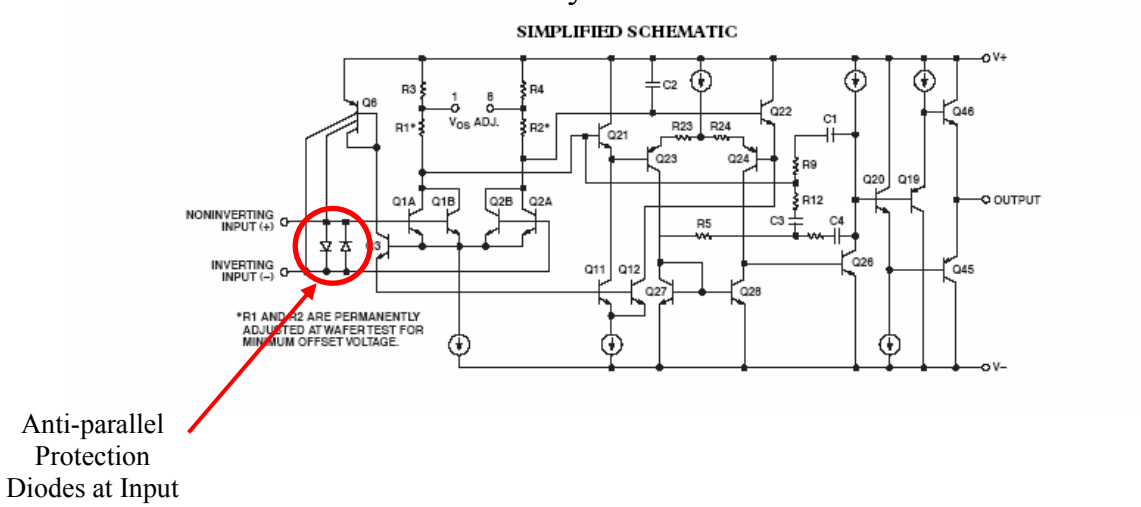


Fig. 3 Schematic of a typical feedback amplifier used in a wide variety of systems controllers such as voltage regulators and over-current protection. The inputs include nonlinear elements (anti-parallel diodes) for over-voltage protection. The diodes, along with parasitic resonances in the circuit, respond to microwave pulses and generate spurious voltages that may cause system instability.

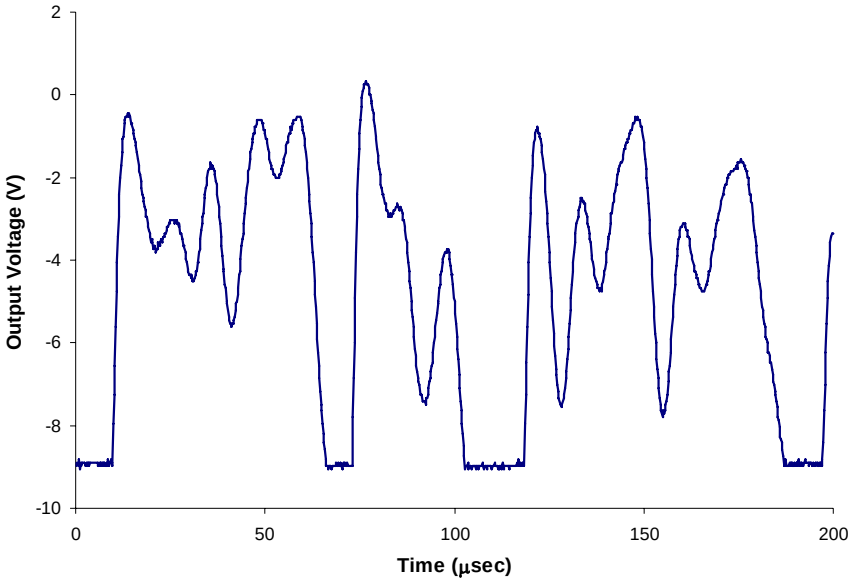


Fig. 4 Time series of the baseband output voltage from an amplifier with feedback when the circuit was irradiated by pulsed RF with wideband modulation.

ONGOING WORK and SUGGESTED FUTURE STUDIES

Our work to date has concentrated either on RF effects that do not permanently alter the electrical characteristics of devices; effects were studied for RF pulse amplitudes that were typically below about 1.0 VRMS. Breakdown and avalanche mechanisms in semiconductor materials due to microwave pulses have not been thoroughly investigated. At RF amplitudes that are higher than operating voltages on chips, sub-micron scale electronics are stressed to the point where the semiconductor lattices could be permanently damaged by energetic (hot) carriers. The peak fields in the semiconductor materials will depend on excitation parameters such as the frequency and modulation characteristics of the RF pulses and internal factors such as parasitic elements, ESD response times and the scale and type of semiconductor structures. Future studies should include conducting experimental and theoretical research on the basic physics of RF-induced hot carriers in semiconductors and the resulting temporal and permanent effects in circuits. Avalanche mechanisms initiated by tunneling currents in thin gate oxides should also be investigated. The goal of this research would be to study the threshold conditions for formation and subsequent avalanche of hot carriers excited by high-frequency fields in semiconductors. One should seek to characterize how and to what extent these processes degrade or damage electronics and how these changes depend on the frequency, amplitude and modulation of RF pulses.

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III.2.c Experimental Studies of RF Interference effects on CMOS MOSFETs, Inverters, and Differential Amplifiers.

This project focuses on identifying the effects of microwave interference signals on the fundamental units of CMOS integrated circuits (IC's) such as individual MOSFETs, single inverters and inverter clusters, and differential amplifiers. Furthermore it seeks to develop microwave hardened chips by identifying the vulnerabilities of the elemental IC units and re-designing units accordingly, and introducing on-chip protection using nanocomposite coatings.

In the past year we have designed and fabricated individual inverters, cascaded inverter clusters, differential amplifiers, D flip-flops, and 4 bit timer circuits and investigated the effects of pulsed microwave interference signals on the operational parameters. The CMOS inverter units of 1.6μm and 0.6μm in packaged and unpackaged forms, with width sizes varying from 1.2 to 120um for the n-MOS and p-MOS transistors, have been designed and fabricated.

Measurements with and without microwave interference were performed on-chip at the input and output of the devices, using microwave probes with a coplanar waveguide and a ground-signal-ground (G-S-G) probe pattern having a 150μm pitch, at a probe station. The current, voltage, and load line characteristics were measured using the HP4145B semiconductor parameter analyzer when controlled CW, pulsed microwave signals, and a logic DC input were applied into the input of the device through a bias-T, as shown in Fig. 1. The power and frequency of the microwave signal were varied from 0 to 24dBm and 800MHz to 3GHz respectively. The period and width of the pulsed microwave were from 200ms to 4s and 1 to 500ms, respectively.

Pulsed microwave interference effects on individual CMOS inverter units exhibited a significant change in the output current and voltage level, a substantial increase in current density (J), and serious bit-flip errors. The voltage and current transfer characteristics showed an abrupt change from a normal DC level to the level comparable to those with CW microwave injection. It is known that the output current of an inverter decreases when the device is thermally excited because of mobility decrease. However, the current transfer characteristics of the 1.6 and 0.6μm inverters, with 1GHz 24dBm pulsed microwave injection (i.e. with much smaller thermal excitation), show reduced output current level compared to those with CW injection (Fig. 2 and 3). Therefore, the effects are related predominantly to excessive charges rather than thermal effects in our case. The current density (J) of each device at a different input bias (V_{IN}) shows that the 0.6μm inverter is more vulnerable to the microwave interference than the 1.6μm device due to output current density increase. Moreover, as the dimension of the inverter unit becomes smaller, the output current density is more sensitive to the change of the pulsed microwave power level suggesting that charge effects are accentuated in the smaller devices.

A new "bit-flip" error is observed when pulsed microwave interference is introduced into the input of CMOS inverters. With 1GHz, 24dBm pulsed microwave having a width of 1.5ms and a period of 500ms, the voltage transfer characteristic of a 1.6μm inverter

shows a bit-flip from V_{OH} (5V) to V_{OL} (0V) when the microwave pulse happens at the threshold voltage (V_{THN}=0.55V) as shown in Fig. 4. In addition, with a 0.6μm inverter, more frequent bit-flip errors are obtained at sub-threshold region, when 1GHz, 24dBm pulsed microwave is introduced at the input of the device (Fig. 5). Moreover, the increased output voltage level due to the pulsed microwave introduced at V_{IN}=4.17V (V_{THP}), won't drop to zero until V_{IN} reaches 4.92V. The frequency increase of the microwave interference suppresses the power effects in our study.

CW Microwave interference on CMOS inverter units also revealed significant degradation in gain, switching capability, and noise margins, as well as, increased intrinsic propagation delay, and excess static and dynamic power dissipation. The current transfer and I-V load line characteristics of the inverter showed substantial increase in current level and degradation of effective on-resistance with the power of microwave interference, resulting in significant stand-by static power dissipation and increased intrinsic propagation delays (Fig. 6. and 7). This increase of current at stand-by is a serious problem as the system experiences a significant disturbance in the power budget distribution from the power rails, leading to local soft and hard errors due to excess currents through contacts and interconnects especially in deep sub-micron systems, and eventually leading to entire system failure.

The voltage transfer characteristics of the inverter (Fig. 8), measured with a 1GHz microwave signal of varying power injected into the input of the device, show the degradation in the input-output voltages, which results in severely compressed noise margins. The integrity of the noise margins in the inverters is critical to the ability of cascaded inverter systems to reject noise and retain the regenerative signal property of inverters in digital systems. This substantial noise margin suppression makes the system vulnerable to bit-flip errors. When 1GHz, 24dBm microwave interference is introduced to the first inverter in a cluster of three cascaded inverters and the input signal is corrupted by a noise signal V_n = 2.1 V resulting in an input $V_{IN}–V_n$=5V–2.1V=2.9V, the output of the third inverter showed a bit-flip error (Fig. 9).

The power effects of microwave interference injection are observed to be suppressed with frequency increase beyond 3GHz as seen previously.

ONGOING WORK and SUGGESTED FUTURE STUDIES

The errors identified in this report are serious problems when the units subjected to pulsed microwave interference are connected to other system units, particularly for deep sub-micron systems where timing speed is high and not synchronized and power budget distribution is very limited. As the pulse width of pulsed microwave interference decreases and the power level increases, protection circuits at the input and output port of a victim system will not be able to respond fast enough before the high power signal disrupts the inside units. Even though the protection circuit can successfully turn on before the interference reaches inside the system, repeated high power microwave pulses will cause substantial current increase at the protection circuit units at first, and cause

burn out and serious upsets later. Therefore, our continuing study will examine the effects of pulsed microwave interference, with much narrower width (≤ μs) and higher power level, on the fundamental building blocks of electronic systems such as positive edge-trigger D flip-flop, 4-bit ring timer (Fig. 10), differential amplifiers with current source load, and PLL. Based on the experimental evidence we are developing a theoretical framework of equations to include these effects in order to provide the basis for re-designing these devices for improved microwave interference hardness.

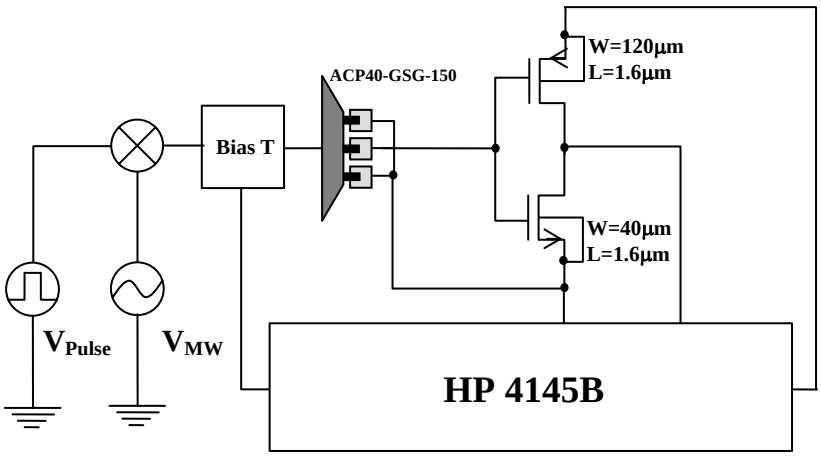

Fig. 1. A schematic of measurement set-up for transfer characteristics of CMOS inverter units with pulsed microwave interference. The current and voltage transfer characteristics of the device were measured using HP 4145B semiconductor parameter analyzer when the pulsed microwave and DC input were injected into the input of the device through a bias-T.

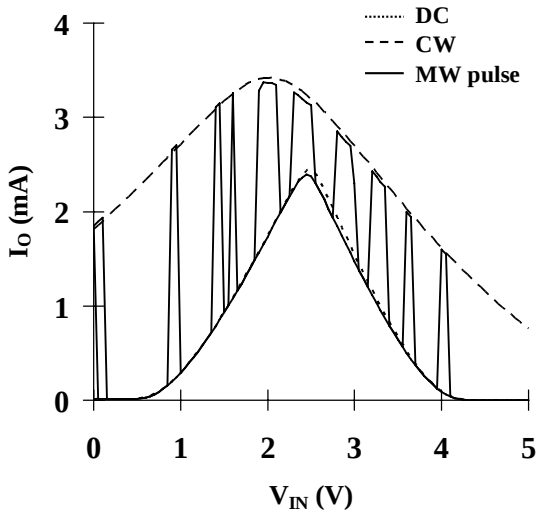

Fig. 2. The measured current transfer characteristic of a 1.6μm inverter with 1GHz, 24dBm pulsed microwave. The width and period of the pulse was 1.5 and 200ms respectively. The characteristic shows an increase of the output current level when pulsed microwave is on. The increase of the current around the inflection point is a little lesser than those with CW microwave interference.

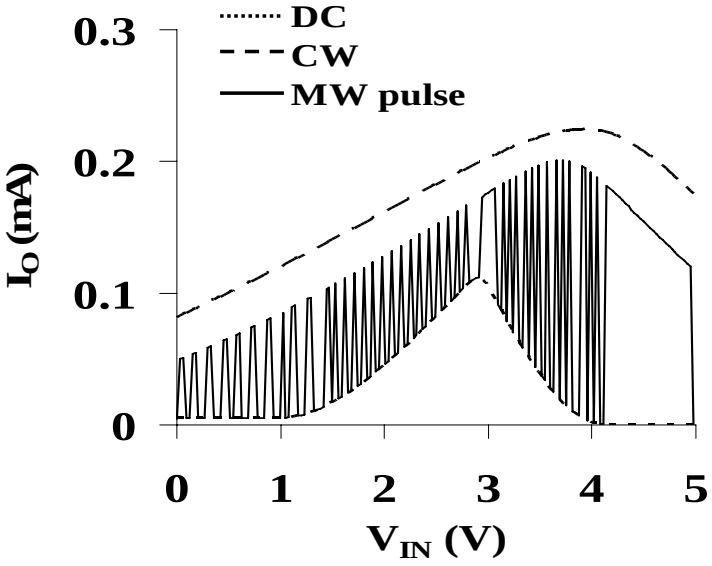

Fig. 3. The current transfer characteristic of a 0.6μm inverter when 1GHz, 24dBm microwave pulse, with a width of 1ms and a period of 200ms, is injected. The inverter consists of p-MOS (W/L=3.6μm/0.6μm) and n-MOS (W/L=1.2μm/0.6μm) devices. The increase of the output current due to pulsed microwave is much smaller than those due to CW microwave. When the microwave pulse is on at V_{IN}=4.92V (V_{THP}), the output current jumps to 1.8mA from 189nA and won't drop until V_{IN} reaches 4.92V.

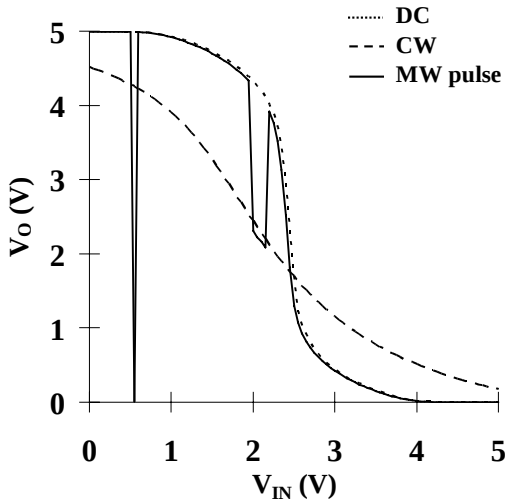

Fig. 4. The voltage transfer characteristic of the 1.6μm inverter with 1GHz, 24dBm pulsed microwave interference. The width and period of the pulse was 1.5ms and 500ms respectively. The characteristic was measured when the pulsed microwave was injected into the input of the device. A new "bit-flip" error from V_{OH} (5V) to V_{OL} (0V) is observed if the interference pulse happens when V_{IN} approaches the threshold voltage (in this case V_{THN}=0.55V), as shown for the two pulses.

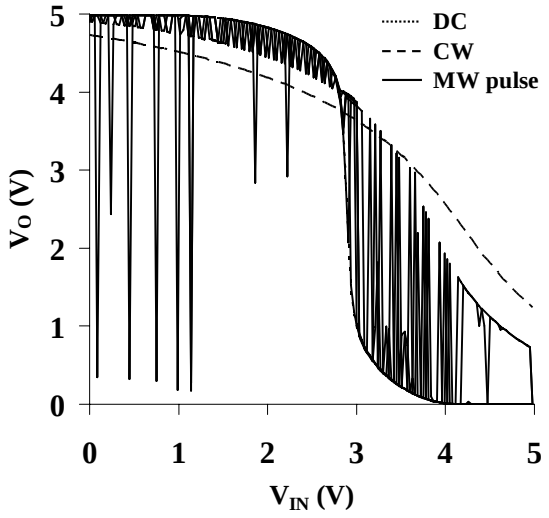

Fig. 5. The voltage transfer characteristic of a 0.6μm inverter with 1GHz, 24dBm pulsed microwave (width: 1ms, period: 200ms). The data measured in a different time frame were plotted together. More frequent bit-error is observed at sub-threshold region (V_{IN}≤1.14V). Moreover, the output voltage level won't drop to zero after the level jumps to 1.67V at V_{IN}=4.17V (V_{THP}), until V_{IN}=4.92V.

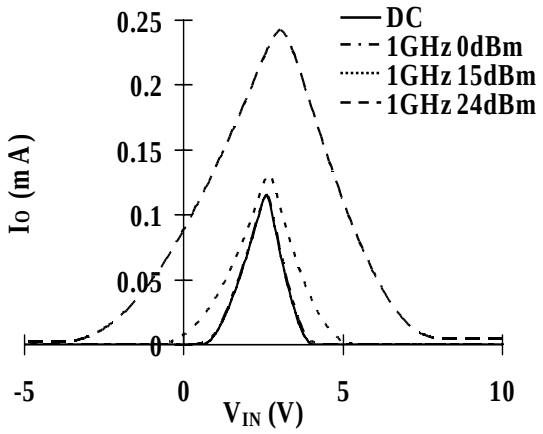

Fig. 6. The current transfer characteristics (I_O-V_{IN}) of a CMOS inverter with and without microwave interference at 1GHz.

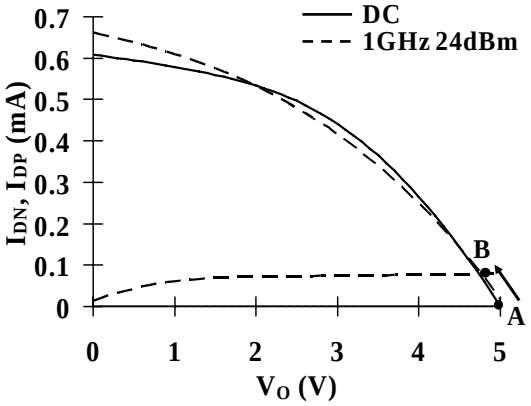

Fig. 7. I-V load line characteristics of the CMOS inverters with 1GHz, 24dBm microwave interference. For V_{IN}=0V, the quiescent operating (Q) point moves from A to B due to the increase in the output current from 12.6nA to 0.11Ma

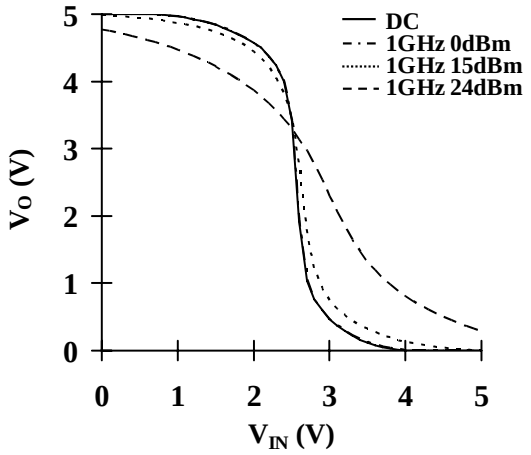

Fig. 8. The voltage transfer characteristics (V_O-V_{IN}) of a CMOS inverter with and without 1GHz microwave interference injection. The characteristic shows degradation of device parameters with interference power. Inflection point shift, gain reduction, input-output voltage shifts, and noise margin compression, are observed.

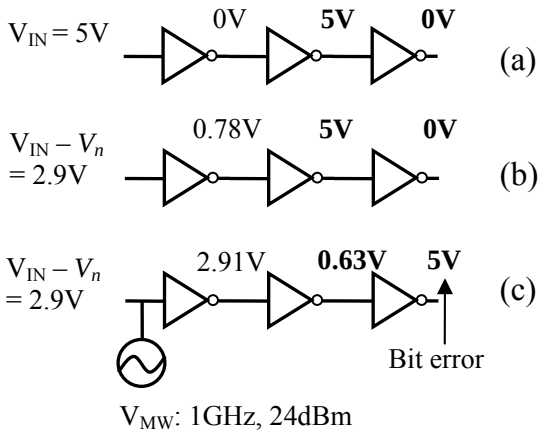

Fig. 9. Measured responses of a cluster of three cascaded CMOS inverter gates. (a) Without microwave interference and noise at the input (b) with noise only at the input and (c) with microwave interference and noise at the input. The measurement showed bit error at the third stage output with a 1GHz, 24dBm interference signal, confirming the loss of the regenerative signal property in cascaded inverters upon interference.

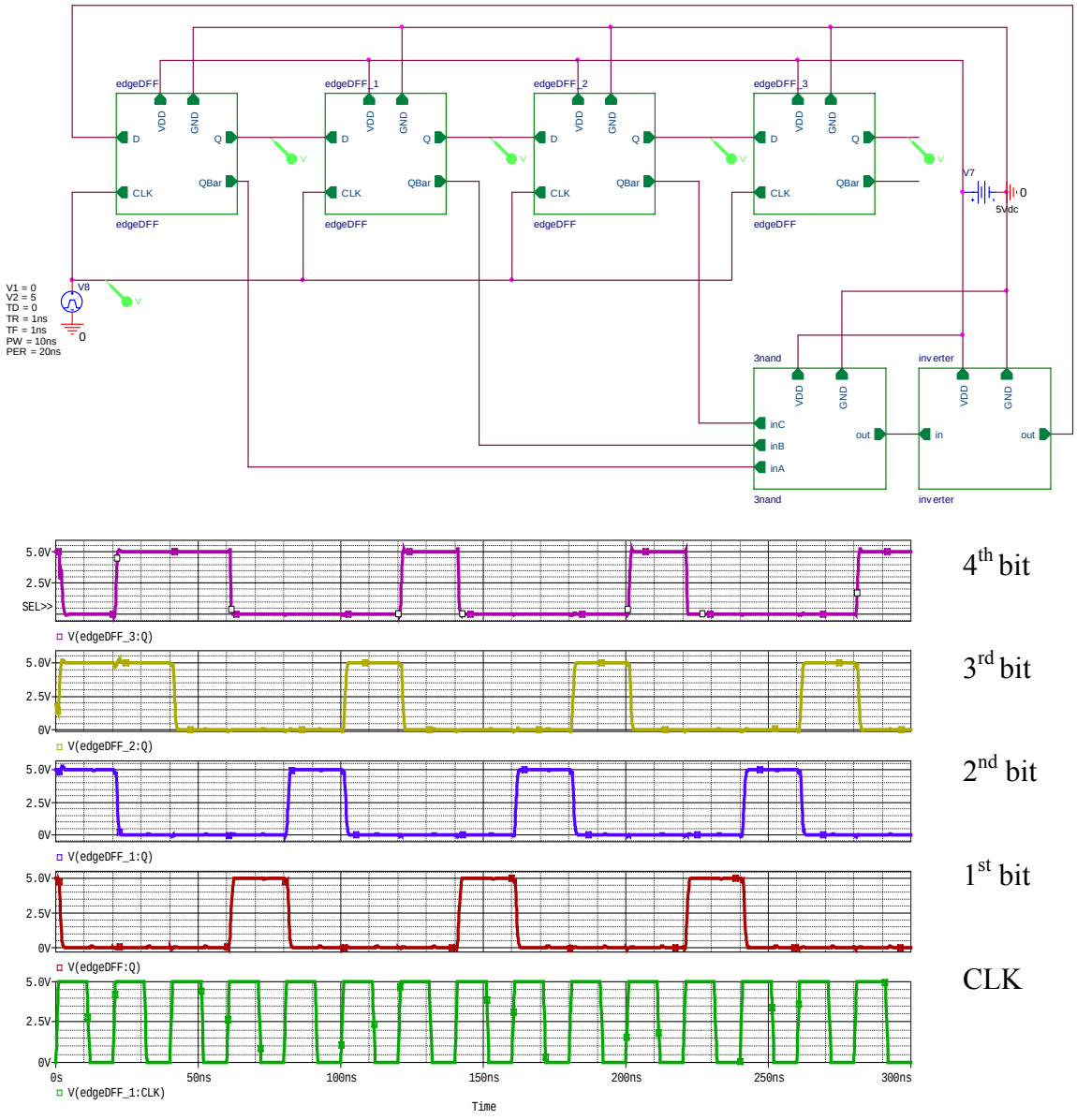

Fig. 10. The schematic of 4-bit timer circuit. The simulation result shows that the circuit gives timing 4bit response after transient time in the beginning.

III.3 Fabrication and Testing of On-Chip Microwave Detectors

(Professor John Melngalis, Dr. John Rodgers;
Students: Todd Firestone, Woochul Jeon)

Since the previous report, several Schottky diodes were fabricated on a test wafer in our laboratory using a CMOS compatible fabrication process and a post-CMOS fabrication process with focused ion beam (FIB) milling and FIB induced deposition. Fabrication of CMOS Schottky diodes through three different commercial CMOS processes (AMIS 1.5μ, 0.5μ, 0.35μ CMOS process) was attempted but was unsuccessful. On the other hand, FIB Schottky diode fabrication on a CMOS processed chip was successful A MOSFET power detector circuit was also designed and tested.

1. CMOS Schottky diode

To make RF pulse power detectors through the standard CMOS process, we have tried to make Schottky diodes by a modified CMOS process and succeeded. We found that every contact layout automatically generates n+ or p+ diffusion to prevent Schottky contacts. We have intentionally removed these diffusions by modifying the layout files. Since we could make Schottky diode through several CMOS processes, our modification is valid and it becomes possible to make Schottky diodes through any CMOS process. The fabricated CMOS Schottky diodes were tested up to 10GHz and showed dynamic range of 35dBm. The series resistances were measured to be 100Ω to 6.5kΩ.

2. Post-CMOS Schottky diodes by FIB

To minimize the contact area and the spreading resistance effect, bridge shaped FIB Schottky diodes were fabricated and tested. Even though the frequency response was not better than previously fabricated FIB diodes, the pulse response time was reduced to 170ns.

3. MOSFET power detector circuits

A previous circuit was a half wave rectifier constructed using a diode connected MOSFET with a bias circuit. We have designed a full wave rectifier circuit to increase the sensitivity and had it fabricated through a 0.5μm CMOS process. Fabricated power detector circuits were tested up to 10GHz. The measured result showed 101ns of pulse response time and flatter frequency response than the previous detector circuits.

4. Measured result

Table 1 summarizes the measured results. For comparison a p-n junction diode and a diode connected MOSFET without a bias circuit were also fabricated and tested. Both the diode connected MOSFET and the p-n junction diode showed poor detection in terms of both sensitivity and frequency response. MOSFET power detectors showed the quickest pulse response time. CMOS Schottky diodes showed the widest dynamic range and highest sensitivity. FIB Schottky diodes showed the best frequency response.

5. RF radiation test

To illustrate an application of these detectors, a fabricated CMOS detector was connected to a metal line on a circuit board and an RF pulse was radiated onto the board with a horn antenna in an anechoic chamber. After measuring, the metal line was cut and tested again to determine the actual power that the metal line picked up. The connected metal line, which acts like an antenna, was tuned to 10.15GHz.

Table 1

	CMOS diode		FIB diode		MOSFET detector		Full wave MOSFET	MOSFET	Junction diode
	n-type 900μm²	n-type 4μm²	n-type 15μm²	Bridge 1μm²	150kΩ Load	1kΩ Load			
Pulse response time(sec)	820n	776n	6 μ	170n	200n	**56n**	101n	1.2μ	16μ
Frequency response (Vout at 1GHz / Vout at 10GHz)	4.93	2.05	**1.52**	3.97	9.59	4.43	2.44	11.33	27.4
Dynamic range (dBm)	**> 35**	> 28	> 25	> 15	15	> 25	>22	> 10	> 10
Sensitivity (dBm) (smallest possible detection)	**-20**	-13	-15	-10	-15	-10	-7	4	7

ONGOING WORK and SUGGESTED FUTURE STUDIES

For future work, another MOSFET power detector circuit with wide dynamic range will be fabricated and tested; this circuit will be fabricated in October. Our MURI work has led us into two new areas, testing the vulnerability of RFID tags and the "harvesting" of RF power for passive devices. The challenge is similar to the detection of hostile RF in chips. For this, an RFID transponder chip was designed and is being fabricated. Since CMOS Schottky diodes were used at the front end of the RFID tag, it could be easy to upset this tag by injecting a low level RF burst. After adding several FIB power detectors, this RFID tag will be tested under RF direct injection to determine which power level and frequency would give the strongest effect on the RFID tag. This experiment would be the focus of our project, since RFID tags are ubiquitous and may be one of the most vulnerable systems.

III.4 Studies of Enclosures and Shielding

(Professor Omar M. Ramahi. Students who have graduated: Lin LI, Xin Wu, Baharak Mohajer-Iravani. Current Students: Sharooz Shaparia, Mohanmmad Haeri Kermani)

In the past year, considerable efforts have been directed at developing electromagnetic band gap (EBG) material or surface for noise mitigation in electronic printed circuit boards (PCB) and for reducing coupling between radiating objects or cavities. While our group has introduced the primary concepts previously (2003), our recent focus was on: (1) miniaturization of EBG structures to enable their practical use in small PBCs and very critically, to allow their use in chip/system packages, and (2) experimental validation of the concept of EBG as surface wave inhibitors to reduce coupling between radiating structures that low impedance links. The progress in each of these two areas is described below.

(1) Miniaturization of EBG structures.

Two strategies were developed to achieve this objective. The first was based on using high-k material as it allows reduction of the electrical size of the EBG patches. Numerical simulations were conducted using material of εr=100-300. As a summary of the simulations conducted, we conclude that EBG patches can be reduced to few mm in size and maintain band gap effectiveness to as low as 1GHz. We have developed a collaboration with two material manufacturers to produce the desired materials. In the past month, samples were obtained with εr=100 and εr=140 and currently we are in the process of fabricating EBG surfaces for testing. We expect to finish this work in the coming two months.

(2) Experimental validation of the concept of EBG structures as surface wave inhibitors.

EBG structures of different patch sizes (2-5mm rectangular patch size) were fabricated and experimentally tested for their effective band gap. The experimental setup used is shown in the Figure 1. Figure 2 shows a sample of the experimental results obtained showing the 3dB band gap. A full description of this experiment in addition to numerical simulations was summarized in a recently submitted paper (see [1] below). The qualitative assessment of the experimental results is that EBG structures made of simple fr4 material and cupper can be effective is appreciably reducing coupling between radiating structures linked through low impedance paths. This technique is considerably less expensive and more mechanically and thermally stable than using engineered lossy material.

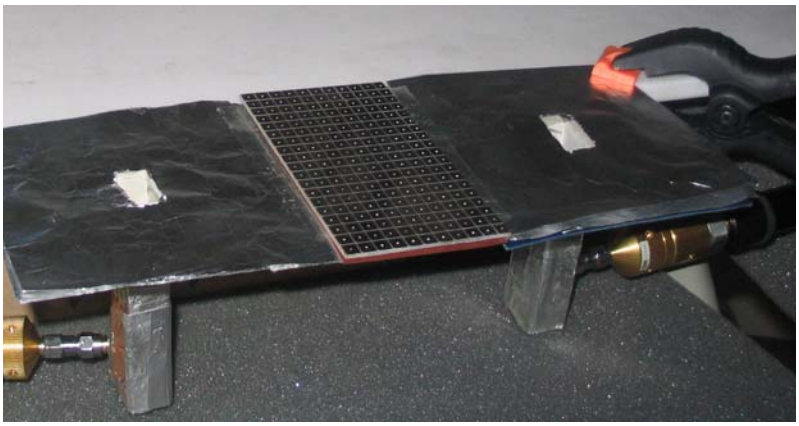

Fig. 1. Experimental setup used to test the effective band gap of different EBG structures.

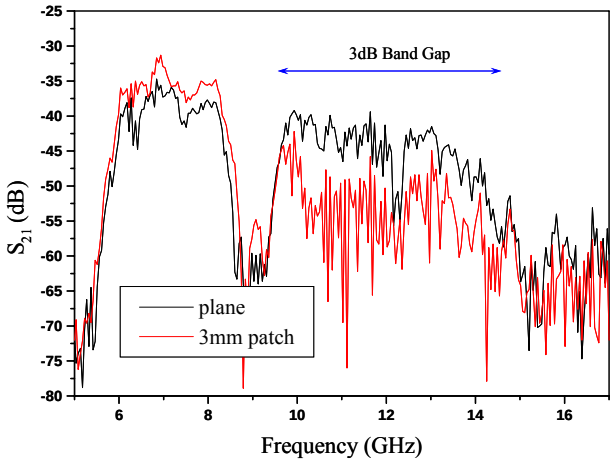

Fig. 2. Coupling between the two antennas as represented by the magnitude of S_{21} with and without the EBG surface. EBG parameters: 3 mm patch, h=1.54 mm, g=.4 mm, d=.8 mm, and a substrate of FR4.

IV. PERSONNEL SUPPORTED

IV.1 Academic Faculty

Professor Steven Anlage, Physics

Professor Thomas M. Antonsen, Jr., Physics and Electrical Engineering

Professor Neil Goldsman, Electrical Engineering

Professor Agis Iliadis, Electrical Engineering

Professor Bruce Jacob, Computer Engineering

Professor John Melngalis, Electrical Engineering

Professor Edward Ott, Physics and Electrical Engineering

Professor Omar Ramahi, Mechanical Engineering

IV.2 Research Faculty

Dr. Yuval Carmel, Inst. for Research in Electronics & Applied Physics (IREAP)

Dr. John Rodgers, IREAP

IV.3 Graduate Students

Vincent Chan

Cagdas Dirik

Todd Firestone

James Hart

Sameer Hemmady

Woochul Jeon

Mohammad Haeri Kermani

Kyechong Kim

Lin Li (graduated with Ph. D.)

Baharak Mohajer-Iravani (Graduated with M.S.)

Laise Parker

Shahrooz Shaparnia

Xin Wu (graduated with Ph. D.)

Bo Yang

X. (Henry) Zheng (graduated with Ph. D.)

V. PUBLICATIONS AND PATENTS

V.1 Refereed Journal Papers During the Reporting Period

1. Sameer Hemmady, Xing Zheng, Thomas M. Antonsen, Edward Ott, and Steven M. Anlage, "**Universal Statistics of the Scattering Coefficient of Chaotic Microwave Cavities**," Phys. Rev. E 71, 056215 (2005). nlin.CD/0503012

2. Sameer Hemmady, Xing Zheng, Edward Ott, Thomas M. Antonsen, and Steven M. Anlage, "**Universal Impedance Fluctuations in Wave Chaotic Systems**," Phys. Rev. Lett. 94, 014102 (2005). cond-mat/0403225.

3. Thomas M. Antonsen, Xing Zheng, Edward Ott, Sameer Hemmady, and Steven Anlage, "**Statistical Model for Scattering Matrices of Open Cavities**," URSI EMTS 2004, 825-827 (2004).

4. Renato Mariz de Moraes and Steven M. Anlage, "**Effects of UHF Stimulus and Negative Feedback on Nonlinear Circuits**," IEEE Trans. Circuits Systems I: Regular Papers, 51, 748 (2004). nlin.CD/0208039

5. S. Shahparnia and O. M. Ramahi, "A simple and effective model for electromagnetic bandgap structures embedded in printed circuit boards," *IEEE Microwave and Wireless Components Letters*, Vol. 15, No. 10, pp. 621-623, Oct. 2005.

6. X. Wu and O. M. Ramahi, "Application of C-COM to the Absorption of Evanescent Waves in Waveguides," *IEEE Microwave and Wireless Components Letters*, to appear in 2005,

7. O. M. Ramahi and L. Li, "Analysis and reduction of electromagnetic field leakage through loaded apertures: A numerical study," to appear in *Electromagnetics Journal,* to appear in 2005,

8. T. Kamgaing and O. M. Ramahi, "Design and modeling of high-impedance electromagnetic surfaces for switching noise suppression in power planes,"*IEEE Transactions on Electromagnetic Compatibility*, to appear in 2005,

9. S. Shahparnia and O. M. Ramahi, "Miniaturized Electromagnetic Bandgap Structures for Broadband Switching Noise Suppression in PCBs," *Electronics Letters*, Vol. 41, No. 9, pp. 519-520, April 2005.

10. K. Kim, A. A. Iliadis, V. Granatstein, "Effects of microwave interference on the operational parameters of n-channel enhancement mode MOSFET devices in CMOS integrated circuits", ***Solid State Electronics***, 48 (10-11), pp. 1795-1799 (2004).

11. W. Jeon, T. Firestone, J. Rodgers, and J. Melngailis, "Design and fabrication of Schottky diode, on-chip RF power detector", Solid state electronics, Vol. 48, Iss. 10-11, pp. 2089-2093, Oct 2004

12. W. Jeon, T. Firestone, J. Rodgers, J. Melngailis, "On-chip RF pulse power detector using FIB as a post-CMOS fabrication process", Journal of Electromagnetics, in-press

V.2 Papers Submitted to Refereed Journals

1. Xing Zheng, Sameer Hemmady, Thomas M. Antonsen Jr., Steven M. Anlage, and Edward Ott, "**Characterization of Fluctuations of Impedance and Scattering Matrices in Wave Chaotic Scattering**," submitted to Phys. Rev. E. cond-mat/0504196.

2.. Sameer Hemmady, Xing Zheng, Thomas M. Antonsen Jr., Edward Ott and Steven M. Anlage, "**Aspects of the Scattering and Impedance Properties of Chaotic Microwave Cavities**," submitted to Acta Physica Polonica A (2006). nlin.CD/0506025.

3. B. Mohajer-Iravani, S. Shahparnia, and O. M. Ramahi, "**Coupling Reduction in Enclosures and Cavities using Electromagnetic Band Gap Structures"**, submitted to IEEE Transaction in Electromagnetic Compatibility. Revised Sept. 2005.

4. T.M. Firestone, J. Rodgers and V.L. Granatstein, **"Investigation of the Radio Frequency Characteristics of CMOS Electrostatic Discharge Protection Devices**", Submitted to IEEE Trans. on Circuits and Systems.

5.K. Kim, A. A. Iliadis, V. Granatstein, "**Operational Degradation and Bit-Flip Errors in CMOS Inverters due to Microwave Interference"**, IEEE Trans EMC, submitted (July, 2005)

6.W. Jeon, T. Firestone, J. Rodgers, J. Melngailis, **"CMOS/Post-CMOS fabrication of on-chip Schottky diode microwave pulse power detectors",** Journal of Directed Energy, under review

V.3 Papers Published in Conference Proceedings

1. O. M. Ramahi, and S. Shahparnia "Miniaturized Electromagnetic Bandgap Structures for Noise Suppression," in proceedings, the 9th International Conference on Electromagnetics in Advanced Applications (ICEAA '05) and the 11th European Electromagnetic Structures Conference (EESC'05), Turin, Italy, pp. 379-381, Sept. 12-16, 2005. (invited paper)

2. S. Shahparnia and O. M. Ramahi, "Design, Implementation and Testing of Miniaturized Electromagnetic Bandgap structures for Broadband Switching Noise Mitigation in High-Speed Printed Circuit Boards," in proceedings, 9th Workshop on Signal Propagation on Interconnects, Garmisch-Partenkirchen, Germany, May 10-13, 2005, pp. 39-40. (invited paper)

3. S. Shahparnia and O. M. Ramahi, Ultra-wideband Miniaturized Electromagnetic Bandgap Structures Embedded in Printed Circuit Boards: Theory, Modeling and Experimental Validation," in proceedings, IEEE/ACES International Conference on Wireless Communications and Applied Computational Electromagnetics, Honolulu, Hawaii, April 3-7, 2005.

4.J. Rodgers, "Study and application of wideband oscillations in high power pulsed traveling-wave tubes for RF effects in circuits," *Proc. 32nd Int. Conf. on Plasma Sci.*, June 20-23, 2005, Monterey, CA.

5. W. Jeon, J. Rodgers, and J. Melngailis, "Design and fabrication of Schottky diode, on-chip RF power detector", Proceedings 2003 ISDRS, Washington DC. Dec. 2003

6. W. Jeon and J. Melngailis, "COMS/post-CMOS fabrication of on-chip Microwave Pulse Power Detectors", Proc., ISAP2005, Vol. 1, pp 221-224, Seoul, Korea, August 2005

7. W. Jeon, T. Firestone, J. Rodgers, and J. Melngailis, "CMOS/post-CMOS fabrication of on-chip Schottky diode microwave pulse power detectors", Proc. Of DET&E conference, Albuquerque, New Mexico, August 2005

V.4 Talks

1. "**Wave Chaotic Scattering Experiments in Microwave Billiards**," invited talk, LINAC Seminar, Institute of Nuclear Physics, Technical University of Darmstadt, Germany, 24 May, 2005. 50 minutes.

2. "**Universal Impedance Fluctuations in Wave Chaotic Systems**," invited talk, 2nd Workshop on Quantum Chaos and Localisation Phenomena," Institute of Physics, Polish Academy of Sciences, Warsaw, Poland, 20 May, 2005. 35 minutes.

3. "**Universal Impedance Fluctuations in Wave Chaotic Systems**," invited talk, International Workshop on Aspects of Quantum Chaotic Scattering, Max Planck Institute for the Physics of Complex Systems, Dresden, Germany, 11 March, 2005, 30 minutes.

4. "**Universal Field, Impedance, and S-Matrix Statistics of Metallic Enclosures**," Invited talk, 5-Power Air Senior National Representative MOU on HPM Semi-Annual Meeting, Eglin Air Force Base, FL, 16 February, 2005, 30 minutes.

5.. "**Chaos in Driven Diode and Electrostatic Discharge Protection Circuits**," Invited talk, 5-Power Air Senior National Representative MOU on HPM Semi-Annual Meeting, Eglin Air Force Base, FL, 16 February, 2005, 30 minutes.

6.. "**Wave Chaos Experiments – Universal Field, Impedance and S-Matrix Statistics of Metallic Enclosures**," Invited talk, MURI Program Review, Rockville, MD, 23 October, 2004, 40 minutes.

7. . J. Rodgers, **"Characteristics of Radio-Frequency Effects in CMOS with Electrostatic Discharge Protection,"** Invited talk presented at Beam Physics Branch, Naval Research Lab, Washington, DC, Aug. 6, 2004.

8, J. Rodgers, T. M. Firestone, V. L. Granatstein, V. Dronov, T. M. Antonsen, Jr. and E. Ott, **"TWT chaotic oscillators and application as source for generating RF effects in advanced CMOS,**" *6th IEEE Int. Vacuum Elec. Conf.*, April 20-22, 2005, Noordwijk, Netherlands.

9, J. Rodgers, T. Firestone, V. L. Granatstein and B. Yeshitla, "**Studies of nonlinear effects in circuits and systems,"** Invited talk presented at the *2005 Workshop on Circuit Chaos,* IREAP, University of Maryland, College Park, MD, May, 13, 2005.

with read-only memory for low cost fabrication", IEEE SOCC 2005, Washingtond DC, September 2005

10. J. Rodgers, **"Microwave sources with stochastic outputs for circuit effects**," Invited talk presented at the *1st Annual DTRA Workshop on HPM Threats*, June 24, 2005, Albuquerque, NM.

11. W. Jeon, J. Melngailis, "**CMOS passive RFID transponder with read-only memory for low cost fabrication"**, IEEE SOCC 2005, Washingtond DC, September 2005

V.5 Patents

1. A. Iliadis, "Sense and Protect Circuit": US Patent Pending # MR2833-15.

VI. INTERACTIONS / TRANSITIONS

Outreach activities:

Prof. Granatstein, Prof. Goldsman, Prof. Anlage and Dr. Rodgers presented a week-long tutorial course on RF Effects (RFW) at the Defense Intelligence Agency, Missile and Space Intelligence Center, Redsone Arsenal, Huntsville, Alabama in August 2005

Prof. Anlage has given invited talks on this work at conferences in Dresden, Germany and Warsaw Poland. He also gave an invited talk on wave chaos at the Nuclear Physics Institute in Darmstadt, Germany. Anlage also gave talks on classical and wave chaos effects in electronics to the NATO GENEC group meeting at Eglin AFB in February, 2005.

Sameer Hemmady gave an invited talk on this work at the DEPS Directed Energy Symposium classified session in October, 2004. He also gave a presentation at the UNM/DTRA review meeting in Albuquerque in June, 2005.

We organized a meeting of the ad hoc DoD group on chaotic effects in electronics in May, 2005. John Rodgers, Sameer Hemmady and Vassili Demergis all gave talks about their chaos research at this meeting.

We have also established working relationships with chaos theory groups in Europe and Mexico to continue developing new ideas for description of electromagnetic problems in complicated enclosures.

VII. HONORS /AWARDS

1. Edward Ott, A. James Clark School of Engineering Faculty Outstanding Research Award, 2005 (Chaos is listed in citation)

2. V.L. Granatstein, Fulbright Senior Specialist Award, Information Technology, Dec.2004-Jan. 2005

3. V.L.Granatstein, Sackler Professor by Special Appointment, Tel Aviv University, Oct.1, 2004 – Sept. 30, 2007.

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APPENDIX
Boise State University MURI Update: (September 2004-present)

Summary:

1. Used the results from the Schottky diode (for detecting RF in CMOS integrated circuits) to publish a paper on bandgap references using Schottky diodes.
2. Inverter Reliability Using MOSFETs with 2nm Gate Oxides
3. Pulse Voltage Stressing in nanometer CMOS
4. NAND Gate Reliability
5. High-Speed Input Buffer Design in the Presence of Interference
6. Publication Update:
   - Butler, D.L, and R.J. Baker, (2005) *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, 2005 Midwest Symposium on Circuits and Systems.
   - Cheek, B.J., R. G. Southwick III, M. L. Ogas, P. E. Nagler, D. Whelchel, S. Kumar, R. J. Baker, W. B. Knowlton, (2004) *Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits*, poster presentation at 2004 IEEE International Integrated Reliability Workshop, Oct. 18-21.
   - An abstract entitled, *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, has been accepted for oral presentation and paper publication at the 2005 IEEE Integrated Reliability Workshop.

5. Presentations:
   - A poster titled "*Defect Accumulation in 2.0 nm SiO_2 Layer of Metal Oxide Semiconductor (MOS) Devices – Effects on Device and Circuit Operation*" was submitted by Mark Elgin, David Whelchel, and David Jenkins to the Boise State University Undergraduate Conference.
   - Michael Ogas presented the poster titled "*Degradation in 2.0 nm and 3.2 nm Gate Oxides – Effects on CMOS Circuit Reliability*" at the Hewlett Packard Day Research Awareness Function in Boise, Idaho HP site.
6. Students:
   - Krishna Duvvada (Graduate Student, Electrical Engineering)
   - Michael Ogas (Graduate Student, Electrical Engineering)
   - Josh Kiepert (Undergraduate Student, Electrical Engineering)
   - Patrick Price (Undergraduate Student, Materials Science and Engineering)
   - Terry Gorseth (Undergraduate Student, Electrical Engineering)
   - David Whelchel (Undergraduate Student, Electrical Engineering)
   - David Jenkins (Undergraduate Student, Electrical Engineering)
   - Mark Elgin (Undergraduate Student, Electrical Engineering)
7. Future work:
   - Submitting a poster to the Boise State University Undergraduate Conference

- Focus towards low voltage wearout and the impact on the time domain of the inverter circuit with respect to the corner parameters,
- Initiation of a paper for publication (conference or journal) based on these results, specific to the inverter circuit.
- Initiate study on another SICBB, or…
- Focus toward low voltage wearout using MWPVS and the impact on the time domain of the inverter circuit with respect to the "corner" parameters,
- Initiation of a paper for publication (conference or journal) based on these results, specific to the inverter circuit.
- Focus toward the NOR circuit in comparison to NAND circuit performance,
- Initiation of a paper for publication (conference or journal) based on these results, specific to the NAND and NOR circuits.
- Initiate study on high *K* dielectric devices

November 1, 2004 to February 15, 2005:

Inverter Reliability Using MOSFETs with 2nm Gate Oxides

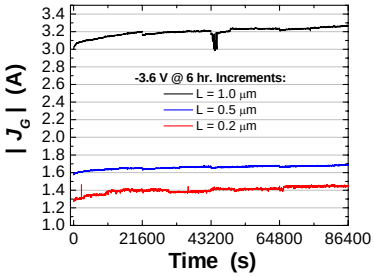


Fig. 1. (a) Constant voltage stress data for 6 hour increments.

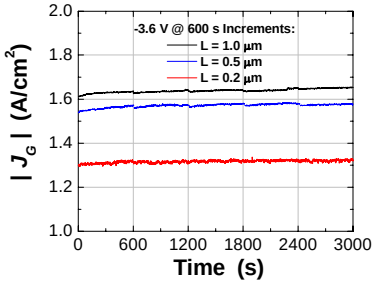


Fig. 1. (b) Constant voltage stress data for 600 second increments.

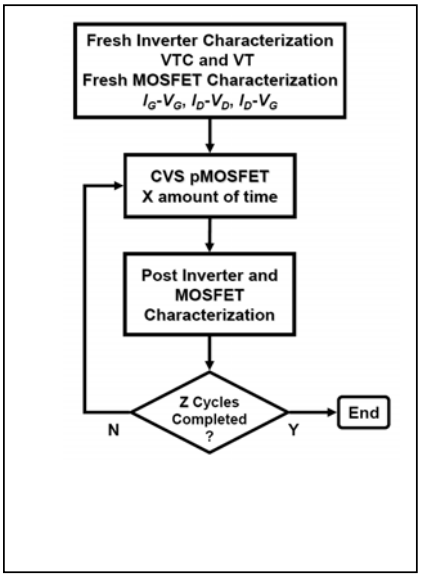


Fig. 2. Algorithm used for obtaining

For ultrathin gate dielectrics, our investigation to answer the question, "When devices in a circuit experience specific degradation that can be induced by electromagnetic coupling (EMC), how will: 1) the devices respond, and 2) the circuit respond?" Students involved in obtaining and analyzing data included Michael Ogas (graduate student) and undergraduate students David Whelchel and Mark Elgin, who have aided the graduate student considerably throughout this study.

The devices used in this study were pMOSFET and nMOSFET devices fabricated using a 0.1 µm CMOS process with an oxide thickness (t_{ox}) of 2.0 nm. The device width was 10 µm while the lengths were varied at 1.0 µm, 0.5 µm, and 0.2 µm. Measurements were conducted using an Agilent 4156C precision semiconductor parameter analyzer connected to an Agilent E5250A low-leakage switch matrix. The novel technique developed in this lab referred to as switch matrix technology (SMT) was utilized at the wafer level using eight Cascade Microtech micromanipulators on a probestation enclosed in a faraday cage, which allows for the configuration of an inverter circuit, as well as the isolation of two separate MOSFET devices to obtain individual IV characteristics.

Wearout or stress induced leakage current (SILC) have been induced by constant voltage stressing (CVS), pulse voltage stressing (PVS), and multiple waveform pulse voltage stress (MWPVS) in our lab. EMC can be caused by a single pulse or a coupling of multiple voltage pulses and thus can be modeled by both PVS or MWPVS. In this study, CVS is used to mimic PVS and MWPVS because of the time to breakdown is the most accurate. The stress voltage used is -3.6 V as it is a relatively low stress. Two sets of data were obtained using this stress voltage over the three different device sizes previously mentioned. After a specified stress time, the stressing was stopped and sense measurements were performed on

the devices. Subsequently, the stress was applied again for the specified stress time followed by sense measurements. Initially, a specified stress time of 6 hours and the gate leakage current was measured as a function time (fig. 1a). However, it was determined that wearout could be observed for shorter time periods and the specified stress time was changed to 600 seconds (fig. 1b).

Both sets of data followed the algorithm shown in Fig 2. This includes preliminary fresh data, followed by CVS, followed by post stress data. Plots of gate current density (J_g) versus gate voltage (V_g) are shown in Fig. 3 (a) and (b). From these current density plots, it can be concluded that approximately the same amount of wearout is occurring in the gate oxide

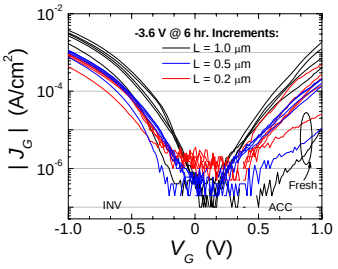


Fig. 3. (a) Current density data obtained between 6 hour increment CVS tests. (b) Current density data obtained between 600 seconds increment CVS tests.

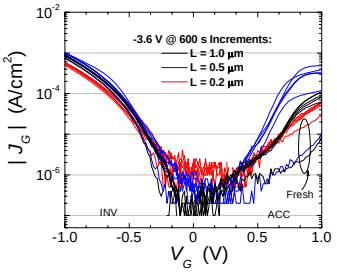


Fig. 3. (b) Current density data obtained between 600 seconds increment CVS tests.

relative to current leakage. In other words, wearout (i.e., I_g) progresses with time and this is seen in both figures 1 and 3.

Both the DC and AC characteristics of inverters were examined in this study. Parameters obtained from the measurements are compared to "corner parameters." "Corner parameters" are boundary parameters of a fabrication process that form a region or process window (i.e., corners of the window). Parameters falling inside of the window are considered within specification. The inverter transfer characteristics (VTCs) obtained confirm a change in the voltage

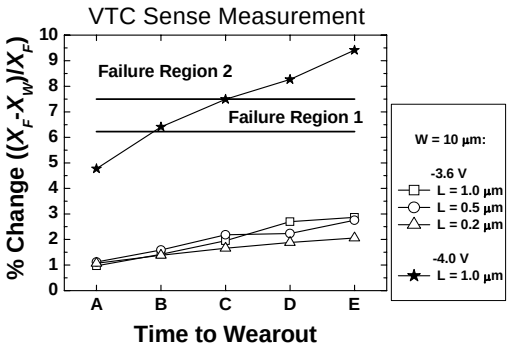
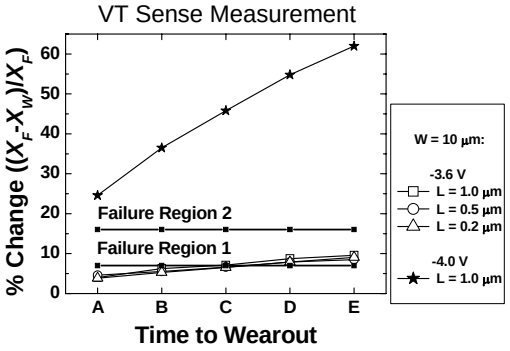


Figure 4. (a) Percent change in VTC measurements showing minimal change in DC characteristics with -3.6 V wearout compared to -4.0 V wearout.



(b) Percent change in VT measurements showing penetration into Failure Region 1 with -3.6 V wearout, suggestive of increased probability of high speed digital logic errors.

switching point by approximately 2.4%, 2.4%, and 2.6% for lengths of 0.2 µm, 0.5 µm, and 1.0 µm, respectively, due to the pMOSFET suffering wearout. Figure 4 (a) expresses the percent change in all device sizes due to -3.6 V wearout voltage compared with previous work on L = 1.0 µm at a -4.0 V wearout voltage. The V_{SP} shifts to the left in all cases. Additionally, the "corner" parameters (e.g. process window) are included with the lower and upper bounds defining Failure Region 1 and Failure Region 2 as the area with increased percentage change. Performance below Failure Region 1 is considered fully operational. Performance within Failure Region 1 may experience circuit failure. Performance within Failure Region 2 is considered to be critical circuit failure. Generally, operation beyond Failure Region 1 is no longer guaranteed due to violation of the corner parameters, while operation within Failure Region 1 is considered an increase in probable failure.

In addition to the DC characteristics, the AC voltage time sense measurements reveal an increase in t_r for lengths of 0.2 µm, 0.5 µm, and 1.0 µm as 9.5%, 9.2%, and 10%, respectively. Figure 4 (b) represents the percent change for the VT observed measurements compared to previous data obtained after -4.0 V wearout and the corner parameters. Failure Region 1 and 2 are defined by the lower and upper bounds of the corner parameters.

February 15, 2005 to May 15, 2005

Pulse Voltage Stressing:

In earlier work, we pioneered a reliability stress technique called multiple waform pulse voltage stressing (MWPVS) to mimic electromagnetic coupling (EMC). The idea behind using this technique is to answer the question, "When devices in a circuit experience specific degradation that can be induced by electromagnetic coupling (EMC), how will: 1) the devices respond, and 2) the circuit respond?" Graduate student, Michael Ogas, along with undergraduates David Whelchel and Mark Elgin, began addressing this question using pMOSFET and nMOSFET devices fabricated using a 0.1 µm CMOS process with an oxide thickness (t_{ox}) of 2.0 nm. The device width was 10 µm while the lengths were varied at 1.0 µm, 0.5 µm, and 0.2 µm. A constant voltage stress (CVS) at -3.6 V for five 600-second intervals (total time = 3000 s) was used to induce wearout, or stress induced leakage current (SILC), in the pMOSFET device to mimic pulse voltage stressing (PVS) and multiple waveform pulse voltage stressing (MWPVS). This data suggested wearout could potentially disrupt an inverter circuit operating in the AC (digital) realm, increasing rise time (t_r) for lengths 0.2 µm, 0.5 µm, and 1.0 µm by approximately 9.5%, 9.2%, and 10%, respectively.

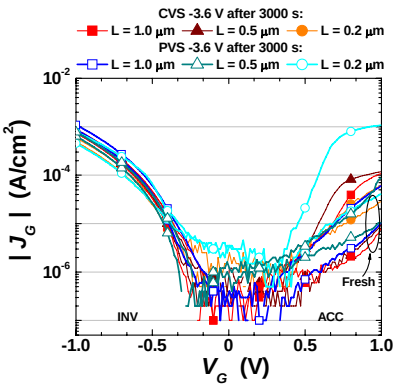


Fig. 5. Current density data obtained between 600 seconds incremented CVS and PVS.

Recently, steps have been taken to initialize MWPVS on the same device sizes studied with CVS. The parameters for MWPVS include wave frequency, base pulse width, spike pulse width, base amplitude, and spike amplitude, as illustrated in Fig. 5. For the initial stage of MWPVS, a spike amplitude of 0 V was used as a correlation point between CVS and MWPVS, which is essentially pulse voltage stressing (PVS). Additionally, the number of pulses was calculated using equation 1:

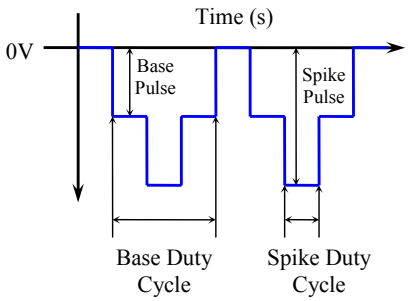


Fig. 6. Schematic of MWPVS waveform.

$$\#Pulses = \frac{TBD}{P \cdot DC_{Carrier}} \qquad [1]$$

(1)

to associate the PVS with the 600-second CVS tests previously mentioned, where time to breakdown (*TBD*) was set to 600 s, the period (*P*) was set to 10 µs, and the carrier wave duty cycle ($DC_{carrier}$) was set to 7.5 µs. MWPVS data was obtained by applying the same testing algorithm as used for the CVS tests, substituting the different stress methodology. Plots of gate current density (J_g) versus gate voltage (V_g) are shown in Fig. 2. From Fig. 6, it can be concluded that approximately the same amount of wearout is occurring in the

gate oxide relative to current leakage across the three device sizes. Furthermore, when comparing PVS to CVS, it can be concluded that wearout (i.e., I_g) progresses with time in approximately the same magnitude.

Results for both the DC and AC characteristics of the inverter were examined to compare to previous CVS tests and "corner" parameters. Recall that "corner" parameters are the typical boundary parameters of a fabrication process, standardized by industry, that form a region (or process window) where parameters falling inside the window are considered within specification. The voltage transfer characteristics (VTCs) obtained confirm a change in the voltage switching point (V_{sp}) by approximately 1.6% and 2.16% for lengths of 0.2 µm and 0.5 µm, respectively, as a result of the pMOSFET suffering wearout. Fig. 7 (a) expresses the percent change in V_{sp} for devices with lengths of 0.2 µm and 0.5 µm as a result of MWPVS compared to previous data obtained with CVS. Additionally, the "corner" parameters are included with the upper and lower bounds defining Failure Region 1 and Failure Region 2 as the area with increased percent change. Recall that operation within Failure Region 2 is no longer guaranteed due to violation of the "corner" parameters, while operation within Failure Region 1 is considered an increase in probable failure.

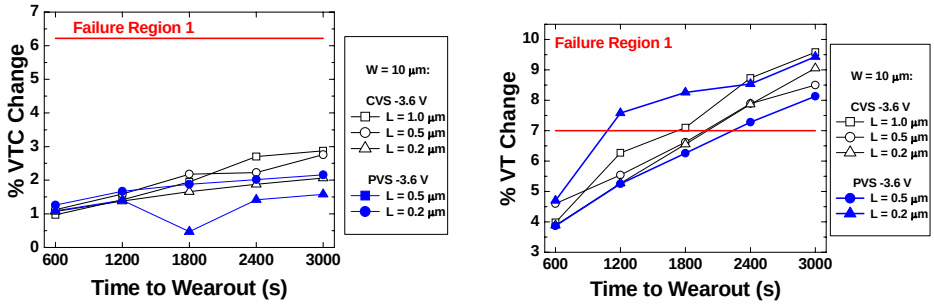


Fig. 7. (a) Percent change in VTC measurements showing minimal change in DC characteristics with -3.6 V CVS wearout compared to -3.6 V PVS wearout. (b) Percent change in VT measurements showing penetration into Failure Region 1 with -3.6 V CVS wearout compared to -3.6 V PVS wearout, suggestive of increased probability of high speed digital logic errors.

The AC voltage time sense measurements reveal an increase in t_r by approximately 9.4% and 8.1 for lengths of 0.2 µm and 0.5 µm, respectively, as a result of the pMOSFET suffering wearout. Fig. 7 (b) expresses the percent change in t_r for these device sizes as a result of MWPVS compared to previous data obtained with CVS. Moreover, the lower and upper bounds of the "corner" parameters define Failure Region 1 and 2.

Additional Highlights:

Two undergraduates working on the project have obtained employment in industry at Micron, Inc., a manufacturer of semiconductor memory. Work on this project provided the students with valuable experience which helped them obtain the industry positions. Several undergraduate students are being interviewed for potential replacement of those students that are leaving.

May 15, 2005 to August 15, 2005
NAND Gate Reliability:

In summary, the focus of this study is to answer the question, "When devices in a circuit experience specific degradation that can be induced by electromagnetic coupling (EMC), how will: 1) the devices respond, and 2) the circuit respond?" The graduate student, Michael Ogas, along with undergraduates Josh Keipert, Patrick Price, and Terry Gorseth, continued to address these questions using pMOSFET and nMOSFET devices fabricated using a 0.1 μm CMOS process with an oxide thickness (t_{ox}) of 2.0 nm. The device width was 10 μm and the length was 0.1 μm. During this quarter, a study was initiated in which defects and degradation mechanisms in MOSFETs that can be created by EMC were induced in a pMOSFET. The pMOSFET was subsequently placed in a NAND gate circuit and both the circuit and the device response was examined.

Using a novel switch matrix technique, a NAND gate circuit was configured using four devices; two nMOSFETs and two pMOSFETs (Fig. 8). A constant voltage stress (CVS) at -4.0 V for five 600-second intervals (total time = 3000 s) was used to induce wearout, or stress induced leakage current (SILC), in one pMOSFET device to mimic pulse voltage stressing (PVS) and multiple waveform pulse voltage stressing (MWPVS). The remaining three MOSFETs were not stressed.

The degraded pMOSFET was tested in two positions of the NAND circuit, as

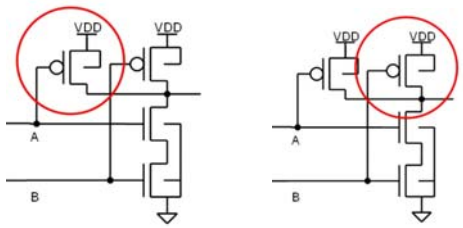
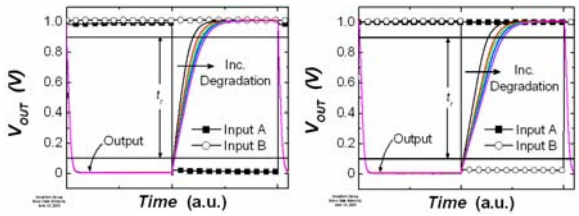


Fig. 8. NAND gate circuits indicating the position of degraded pMOSFET.

shown in Fig 8. Additionally, multiple NAND gate configurations were studied (Table 1). The measured device parameters included gate leakage current (I_G-V_G), maximum drain current ($I_{DRIVE,MAX}$), transconductance ($G_{M,MAX}$), threshold voltage (V_{TH}) and off-current (I_{OFF}). The NAND gate response was examined for both pMOSFET positions in all four input/output (I/O) states (i.e., configuration position # - I/O state #) shown in Table 1. Both the AC voltage time (V-t) sense measurements and the voltage transfer characteristics (VTC) were examined.

It has been observed that only configurations 1-3 and 2-1 have exhibited an effect from pMOSFET wearout in terms of V-t. Figure 9 shows the resulting NAND gate V-t circuit response. An increase in rise time (t_r) ranging from 63% to 70% for both configurations has been observed.

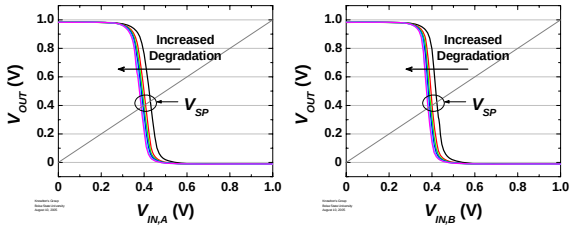
Additionally, degradation has been observed in the VTCs for configurations 1-3 and 2-1. Figure 10 depicts output voltage (V_{OUT}) versus input voltage ($V_{IN,A}$ or $V_{IN,B}$). A shift of the voltage switching point (V_{SP}) of the NAND gate as a result of wearout was found to be nearly 8% to the left, as shown in Figure 10.



Configuration 1-3 **Configuration 2-1**

Fig. 9. NAND gate V-t measurements as a result of wearout in one pMOSFET indicated by Configuration 1-3 or Configuration 2-1.

The decreased performance of the NAND gate circuit shown in the V-t and VTC



Configuration 1-3 **Configuration 2-1**

Fig. 10. NAND gate VTC measurements as a result of wearout in one pMOSFET indicated by Configuration 1-3 or Configuration 2-1.

graphs is contributed to the degradation of the pMOSFET indicated in Fig. 8. The device parameters have proven to consistently decrease with increased wearout time. These changes include a decrease in $I_{DRIVE,MAX}$ (Fig. 11) by 40% to 47%, an increase in V_{TH} (Fig. 12) by 14% to 18%, and a decrease in $G_{M,MAX}$ (Fig. 12) by 21% to 30%. Additionally, a decrease in I_{OFF} (Fig. 13) by 45% to 62% is observed.

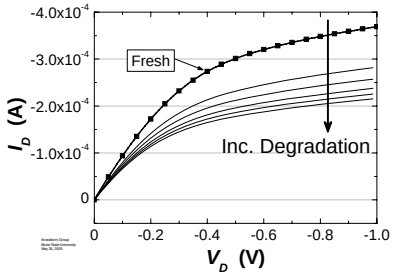


Fig. 11. Typical results showing a decrease in drive current with increasing wearout in one pMOSFET of the NAND gate.

Similar to our previous work with inverter circuits, an increase in pMOSFET channel resistance is the possible cause for the observed increase in t_r for the NAND gate. Ultimately, the increase in rise time may affect the critical timing path of digital logic circuits such as clocked registers, which depend on precise timing to function properly.

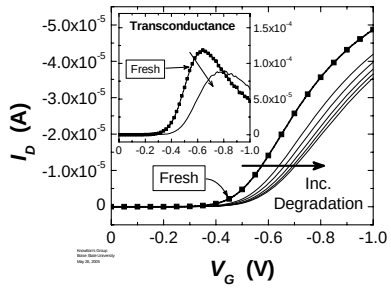


Fig. 12. Typical results showing an increase in threshold voltage with increasing wearout in one pMOSFET of the NAND gate. The inset illustrates the corresponding decrease in the maximum transconductance response.

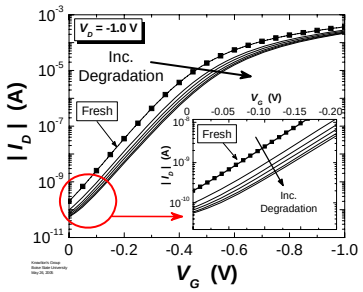


Fig. 13. Typical results showing a decrease in off current with increasing wearout in one pMOSFET of the NAND gate. The inset illustrates the corresponding decrease in the I_{OFF} regime.

High-Speed Input Buffer Design for RF Signal Transmission in the Presence of Interference

High speed input signals can travel through a transmission cable and get distorted or experience interference prior to reaching the a CMOS chip. The input buffers take the chip's input signal with imperfections such as slow rise and fall times and convert them in to full logic voltage levels which can be used in the chip's main logic circuit. Typically these input buffers are used after the ESD protection circuit. The design of these input buffers here has been processed in 0.5um CMOS processes with a die size of 1.5 x $1.5\,mm^2$ and a supply voltage of 5V with a scale factor of 0.3um. This section describes input buffer designs using NMOS (Fig. 14), PMOS (Fig. 15), and parallel combination of both the topologies (Fig. 16).

For buffers employing inverters in series, the switching point of the inverter varies due to the attenuation of the amplitude of the input signal. To overcome this problem, the mean of the input signal is given to the reference input of the differential amplifier. When the input is just above the reference voltage, the output transition will be logic high. If the input is below the reference voltage, the output will be logic zero.

The buffer topologies used in this design, have a differential amplifier, which amplifies the difference between the reference voltage, transmitted on a different signal path, along with data and input pulse on other signal paths. It is a self-biased circuit because no external references are used to set the current in the circuit. It also has an enable circuit having a PMOS and NMOS as seen in the schematic. When

thesetransistors are OFF, the output of the circuit will be in high impedance state and the input to the inverter driving the signal will not have a valid logic. So there is a large amount of current flows in the circuit which might damage the chip. To eliminate this

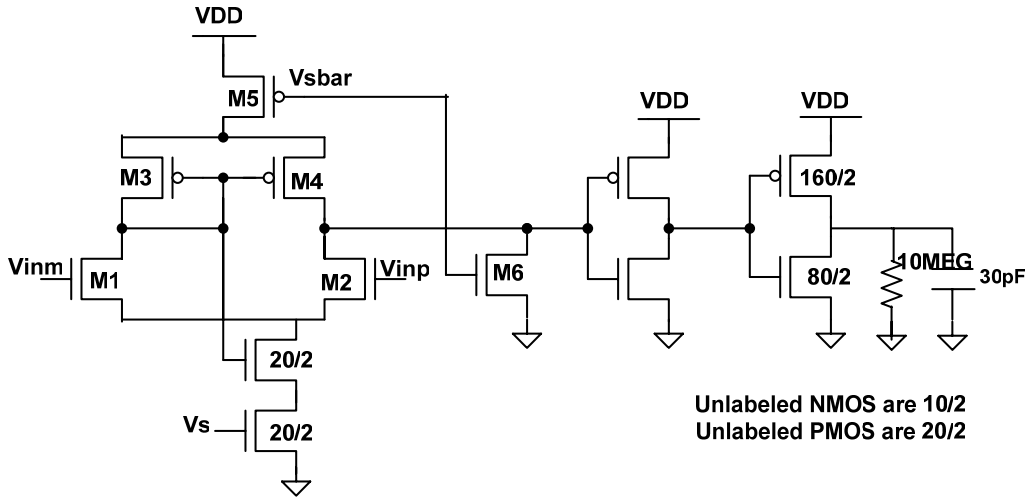


Fig. 14. An NMOS self-biased input buffer.

problem, an NMOS switch M8 is connected at the output of the differential amplifier. The gate of the NMOS switch is connected to VSbar as shown. 160/80 size inverter is added to drive the large capacitive load. 30pF load capacitor is used in parallel with 10MEG resistor taking the probe cable and oscilloscope in to consideration. GSG (ground-signal-ground) pads are used in the layout with a pitch of 150um.

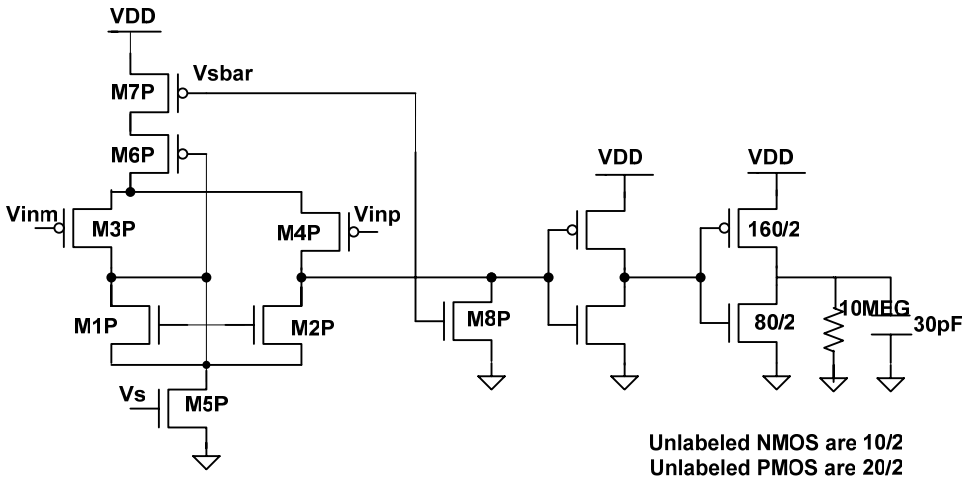


Fig. 15. An PMOS self-biased input buffer.

In the Fig. 14, when Vinp is larger than Vinm, the current in M2 is greater than the current in M1. Due to the current mirror action, the currents in M3 and M4 are same i.e. M1, M3 and M4 have same

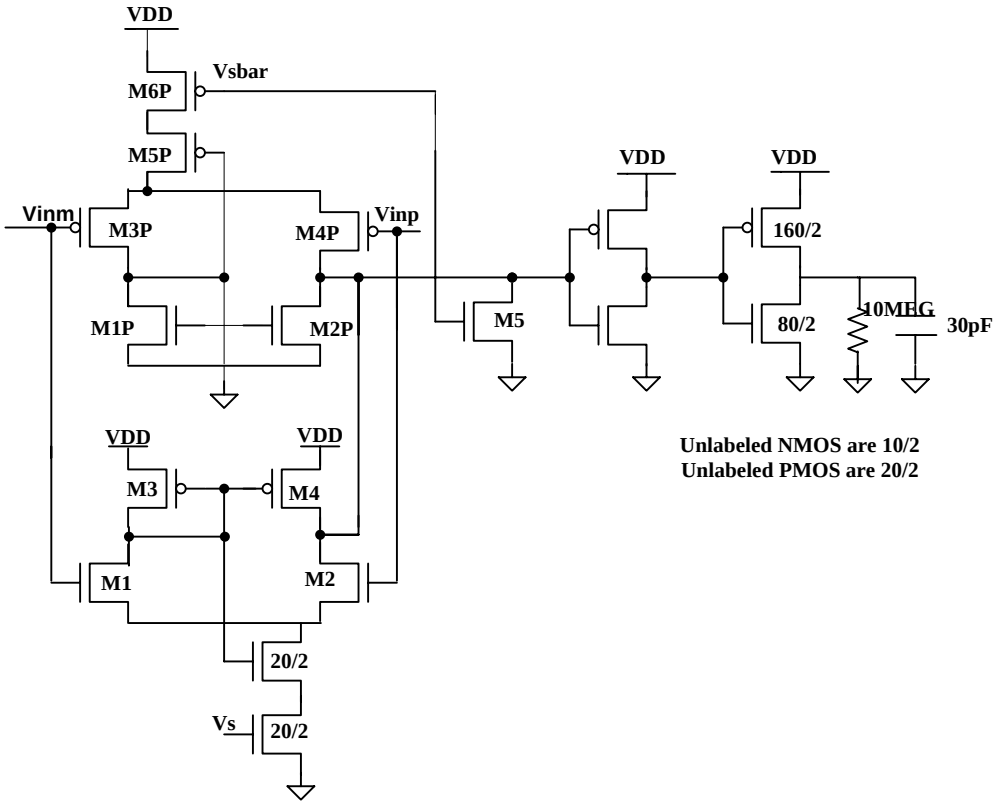
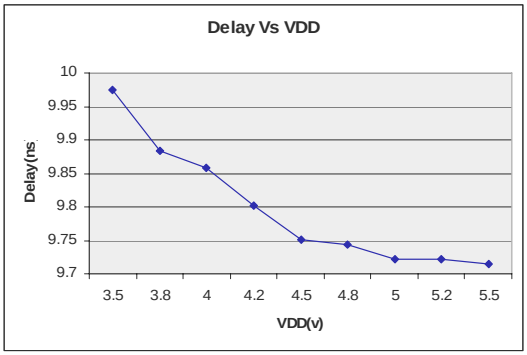


Fig. 16. Parallel input self-biased input buffer.

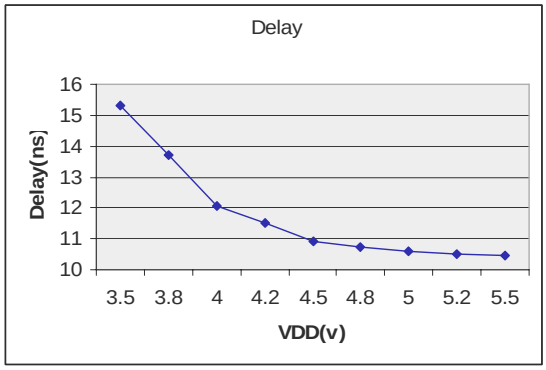
currents. In order to have the same currents in M4 and M2 the transistor M2 pulls the output V1 to ground giving a good logic at the output of the buffer.

During the operation of the buffer circuit, both M7 and M6 are ON. The problem with this topology is it cannot work for the lower input signals. PMOS version of the buffer can be used for lower input signal amplitudes. But with PMOS buffers, there is a problem with offset which can be eliminated by using NMOS in parallel with PMOS version shown in the schematic. The parallel buffer works over a wide range of operating voltages in which NMOS for offsets and PMOS for operating when the signals are low or VDD.

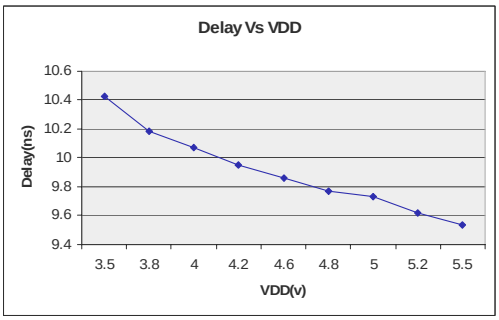
Simulations have been performed using the SPICE simulator to check the changes in delays with the variations of supply voltage, temperature, reference voltage, and rise and fall times. Different spice model parameters like fast-fast, slow-slow and typical are used and simulated to see the performance of the input buffers. These are less sensitive to variation in processing, temperature and supply voltages which are desirable in several applications in digital CMOS integrated circuits where precision, high speed and high production yields are required. Ideally these delays are independent on these performance issues. The measured data showing the variations in delay with the changes in the supply voltage and reference voltage, for the various buffers is seen in Fig. 17.



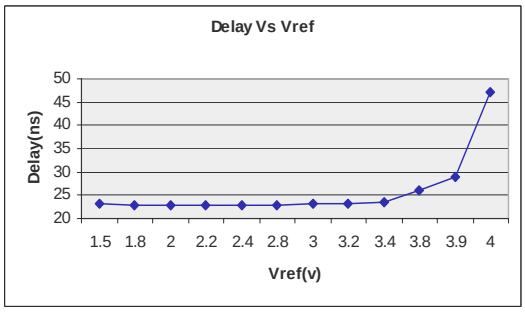
(a) NMOS input buffer measured data



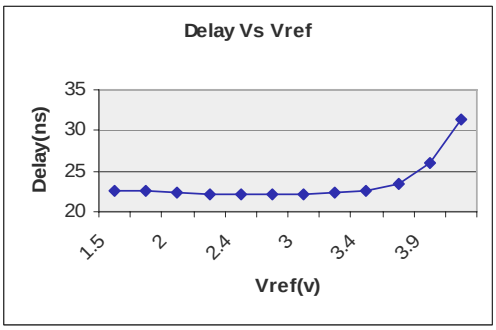
(b) PMOS input buffer measured data



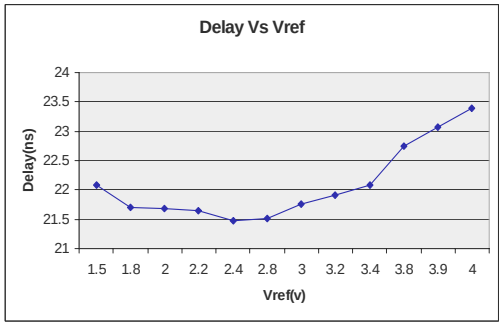
(c) Parallel input buffer measured data



(d) NMOS input buffer delay vs Vref



(e) PMOS input buffer delay vs Vref



(e) Parallel buffer delay vs Vref

Fig. 17 Measured delays of various input buffers.