A Simple Finite-Difference Frequency-Domain (FDFD) Algorithm for Analysis of Switching Noise in Printed Circuit Boards and Packages

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***Abstract*—Simultaneous switching noise (SSN) compromises the integrity of the power distribution structure on multilayer printed circuit boards (PCB). Several methods have been used to investigate SSN. These methods ranged from simple lumped circuit models to full-wave (dynamic) three-dimensional Maxwell equations simulators. In this work, we present an efficient and simple finite-difference frequency-domain (FDFD) based algorithm that can simulate, with high accuracy, the capacity of a PCB board to introduce SSN. The FDFD code developed here also allows for simulation of real-world decoupling capacitors that are typically used to mitigate SSN effects at sub 1 GHz frequencies. Furthermore, the algorithm is capable of including lumped circuit elements having user-specified complex impedance. Numerical results are presented for several test boards and packages, with and without decoupling capacitors. Validation of the FDFD code is demonstrated through comparison with other algorithms and laboratory measurements.**

***Index Terms*—Delta-I noise, EMC, EMI, finite-difference frequency-domain, packaging, power distribution networks, power planes, simultaneous switching noise.**

I. Introduction

TWO CRITICAL advances in digital electronics development have heightened the importance of careful analysis of power plane noise. As the clock frequency increases, the interconnects and board impedance increases. Consequently, these effects lead to an increase in the voltage drop across the board resulting in appreciable differentiation in the voltage levels across power planes. As the threshold of digital logic decreases, fluctuations in the voltage level across the power planes makes the electronic circuitry more susceptible to false logic switching. These developments highlight the importance of developing software tools that enable accurate simulation of power planes in multilayer printed circuit boards (PCBs) under various switching situations. The voltage disturbance caused by high-speed switching of electronic devices is referred to as simultaneous switching noise (SSN), ground/power bounce noise, or Delta-I noise.

A simple, yet insightful model for understanding the effect of SSN or the voltage disturbance on the power distribution network assumes predominantly inductive impedance for power planes. This assumption leads to the familiar relationship between the voltage and current in an inductor, given by

$$v_{\text{noise}} = L_{\text{eff}} \frac{\partial i}{\partial t} \tag{1}$$

where v_{noise} is the voltage drop between the power and reference planes, $i(t)$ is the current drawn by the switching device, and L_{eff} is an effective inductance that can be considered as an equivalent inductance of the power distribution network.

The model represented by (1) is simple yet is important in establishing the link between high-speed switching and its effect on the power distribution network. Notice that as the switching time decreases, the magnitude of v_{noise} increases. Furthermore, a reduction of board impedance, namely inductance, can help mitigate the effect of high-speed switching. However, what is not represented in this simple model is the nonuniformity and nonlinearity of the board inductance, L_{eff}.

The inductance is a nonintrinsic property of the copper boards, and it strongly depends on two primary factors: the current path, and board topology (power distribution physical layers). It is important to realize that these two factors are not mutually independent. Board artifacts and construction that directly affect the current path will not be considered in this work. In this work, we focus on prediction of SSN due to the effect of PCB topology and the effect of placement of real-world decoupling capacitors.

Fig. 1 shows a schematic (side view) of a PCB with two layers (two power planes sandwiching a dielectric slab). Also shown on the schematic, several vias representing either the connection of devices to the power layers, or part of the signal trace as it traverses the power layers from one side of the board to the other). Considering Fig. 1, when a device connected to via A switches, it induces a quasiradial wave that propagates within the two layers. This wave affects the constant voltage difference between the two layers, thus increasing the susceptibility of other devices connected to the circuit board to experience false logic switching. For instance, if a device is connected to a trace with a via crossing the power layers, as would be the case in via C, noise will be coupled on this trace. The active device, shown in Fig. 1, will experience a perturbed voltage supply. Notice

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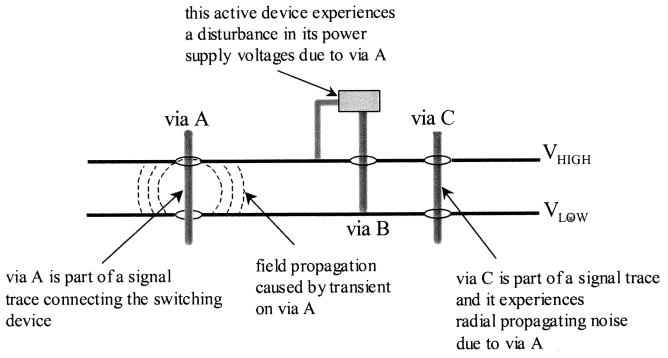

Fig. 1. Schematic of a two-layer PCB showing the effect of switching on the power distribution network and signal vias.

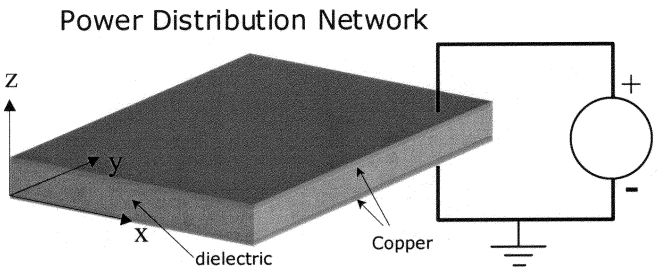

Fig. 2. Power distribution network showing the supply dc voltage and power planes.

that any device connected to via C will experience a high-frequency noise component due to the outgoing quasiradial wave, in addition to the lower-frequency components arising from the bouncing back and forth of the waves as they reflect off the boundary.

The voltage ripple, which is caused by high-speed switching, is guided by the two-layer planes, in a manner highly similar to the mechanism of propagation in a parallel plate waveguide [1]. If the voltage disturbance reaches the end of the plates (resembling the open-ended waveguide), then reflection occurs, which consequently leads to board resonance. Signal harmonics coinciding with board resonance can be severely degraded. This may jeopardize the operation of sensitive integrated circuits on the PCB. (Field penetration through the copper plates can induce resonance in adjoining layers [2], [3]. This effect, however, will not be discussed in this work.)

Resonance in parallel plate printed circuit boards has been investigated earlier. In [4] and [5], the power distribution system is considered as a dynamic electromagnetic system in which the propagation effects are included. Power planes of a PCB strongly resemble a parallel plate waveguiding system [1], [4], [5]. Much of the electromagnetic energy associated with transients is captured within the planes, thus resembling high Q resonant cavities [3], [6]. Several methodologies have been used to model these resonant cavities. For instance, [2] uses a method to extract circuit models for these planes and simulate SSN. The circuit model approach is extended in [3] by combining the circuit and transmission line models to simulate noise in a multilayered board and package. In [7], a distributed circuit model is used to effectively simulate high frequency resonance that can be used to model arbitrarily shaped planes with decoupling capacitors. The Method of Moments (MoM), which is based on the integral equation formulation, is used in [8]. But the MoM, which involves construction of the Green's function, becomes complicated when used to model a complex structure [9]. In [6] it is shown that traces and power plane structures in packages behave more like transmission lines with impedance and delay rather than lumped inductors. The transmission line method (TLM), is used to model such power plane pairs in [10].

The partial element equivalent circuit (PEEC), which is a derivative of the MoM, is used for quasistatic partial element calculations [9]. The model includes all retardation effects and is compatible with circuit simulators [11]. The PEEC technique has the capability to include a large number of lumped circuit elements for decoupling analysis [12]. The finite-difference time-domain (FDTD) method, which is a direct time domain Maxwell equations solver [9], [13], has been used effectively to model infinite and finite power plane resonances in [1]. This technique can be used to model complex designs of PCBs and one simulation can be used to study a broad spectrum of frequencies [14], [15].

Three-dimensional full-wave electromagnetic field solvers such as the MoM and PEEC can accurately simulate power/ground plane structures but they are not suitable for fast simulation of practical designs with numerous vias and multiple power planes because of their enormous computer memory requirements. These methods are based on the full-wave description of the radiation phenomenon, and, expectedly, are extremely inefficient and may take up to several hours to model a single PCB over a narrow band of frequency.

In this work, our objective is to develop a simple algorithm to analyze SSN based on the finite-difference frequency-domain (FDFD) method. The algorithm should have the following features.

1) It should be numerically efficient to allow faster simulation times than the present three-dimensional full-wave models.
2) It should be able to incorporate user specified impedance for lumped elements such as decoupling capacitors and terminations.
3) It should be able to predict (calculate) physically measurable quantities such as S-parameters.

In recent work, the FDFD method was used to solve for the eigensolutions characterizing the propagation of the electromagnetic waves in power planes [4]. In this work, we extend the FDFD capabilities to find the resonant frequencies of power planes, and to calculate the S- parameters for selected circuit ports. Furthermore, we incorporate real-world and user-specified lumped capacitors in our FDFD model, and study the effects these real-world capacitors have on board resonance. Finally, we study power plane resonance in chip packages, especially the effect of including lead inductance in decoupling capacitors.

II. Mathematical Model Development

Power planes used in multilayer circuit boards consist of parallel plates that are stacked while sandwiching a dielectric material between them. Fig. 2 shows a schematic for power distribution network including the power planes. Each plane is intended to have a constant voltage across its entire area. For most

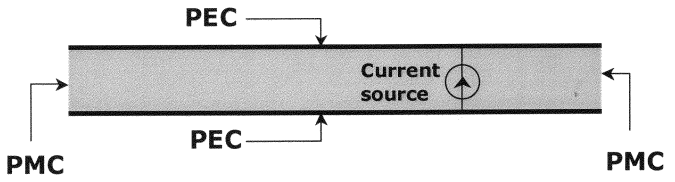

Fig. 3. PMC used as a boundary condition to terminate the FDFD computational domain.

practical applications, the separation of the two planes is in the millimeter or sub-millimeter range, which is much less than the wavelength corresponding to the highest harmonic of clock frequencies of present-day technology. (Note that for clock frequencies in the range of 2–10 GHz, and for FR4 board material having a dielectric constant of approximately 4, the wavelength ranges from 1.5 cm to 7.5 cm.) Because of the electrically short dimension of the board's separation (dielectric thickness), the electromagnetic fields within the boards can be approximated as constant in the z-direction (see Fig. 2). With this approximation holding, the z-component of the electric field within the board, E_z, satisfies the two-dimensional Helmholtz equation given by

$$\nabla^2 E_z(r) + k^2 E_z(r) = \delta(r - r_0) \tag{2}$$

where r_0 represents the location of the current source in cylindrical coordinates $k = \omega\sqrt{(\mu\varepsilon)}$ is the wave number in the dielectric material (between the two conducting plates), and (μ, ε) represent the constitutive parameters of the dielectric medium. The function $\delta(r - r_0)$ is the Dirac-Delta function.

In this mathematical model, the current source is positioned at a fixed location within the board and it consequently gives rise to two-dimensional wave propagation within the board. The physical source of energy that gives rise to SSN is typically a fast-switching transistor having internal impedance higher than the power plane impedance [16]. Therefore, the ideal *impressed* current source used in (1) is considered an effective model for this source. A physical interpretation of our model is shown in Fig. 3 in which the current source represents the fast-switching transistor.

Since the two power planes have finite dimensions, the two-dimensions validity of the model can be maintained only up to the boundary of the plates where the board interfaces with the surrounding area, which is typically air or free space. Because of the electrically-small separation between the boards, the board-air junction at the end of the board strongly resembles an open-ended transmission line termination. Therefore, a boundary condition that is effective in terminating the computational domain is a magnetic wall, or a perfect magnetic conductor (PMC). The PMC mimics the behavior of an open-ended transmission line (here, the power plane plates can be considered as open-ended parallel plate waveguide). Fig. 3 illustrates where the PMC boundary condition is applied. The magnetic wall boundary condition is expressed as

$$\left.\frac{\partial E_z}{\partial n}\right|_{\text{boundary}} = 0 \tag{3}$$

where n is the normal direction to the dielectric-air interface, corresponding to either the x or the y directions.

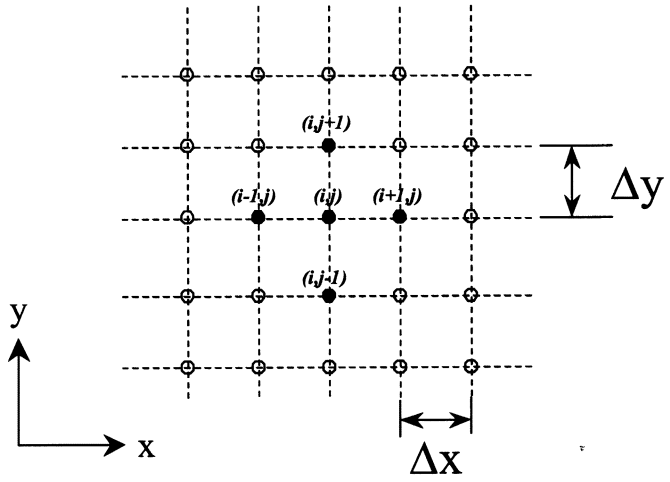

Fig. 4. Grid used for the finite-difference frequency-domain method.

The PMC boundary condition model is expected to be effective as long as the electrical separation between the two power planes is much smaller than the wavelength at the highest frequency of operation (see [1] for a comprehensive look at the effectiveness and validity of the PMC boundary condition model in the dynamic simulation of power planes).

The solution of (2) requires the division of the power plane's computational domain over which the solution is sought into grid in the $x - y$ plane as shown in Fig. 4, with grid spacing in the x- and y-directions given by Δx and Δy, respectively. For simplicity, we consider $\Delta x = \Delta y = \Delta$. Applying the FDFD scheme to the free-space Helmholtz equation at an interior node (i, j), we have

$$E_z(i-1,j) + E_z(i+1,j) + E_z(i,j+1) + E_z(i,j-1) + \left(k^2\Delta^2 - 4\right) E_z(i,j) = 0. \tag{4}$$

Equation (4) leads to a matrix system that is highly sparse, thus facilitating the use of sparse matrix solver that stores only the nonzero elements. This solution procedure leads to significant savings, not just in memory allocation but also in execution time.

The strength of the FDFD method lies in its simplicity and both formulation and implementation. A complete algorithm can be easily developed and implemented in few hours and solved using sparse matrix solvers on Matlab or other platforms. A key advantage, however, in using the FDFD schemes lies in its accommodation of loads that can have any complex combination of R, L, and C components. This advantage is primarily due to the time-harmonic formulation, which would preclude complicated convolution procedure typically needed when translating the time-harmonic characterization into time-domain formulation, as would be needed when using the FDTD method or its variants [1]–[3], [10], [17], [21]. This advantage of the FDFD method is highlighted, discussed and used in Section III.

III. Power Planes With Lumped Circuit Elements

The placement of lumped capacitors is typically considered one of the first lines of defense against the corrupting influence

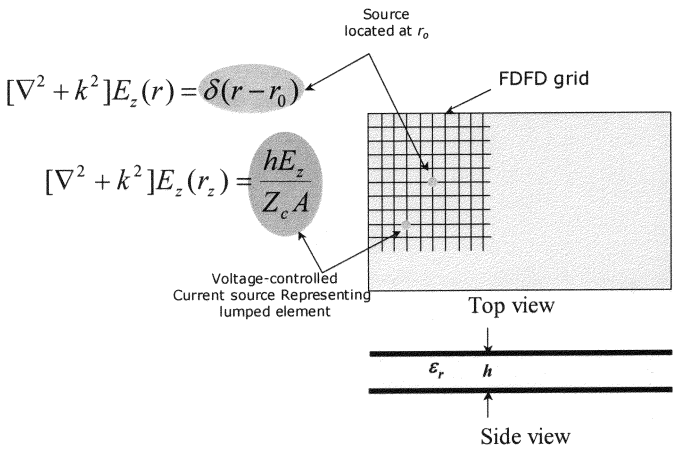

Fig. 5. FDFD grid showing the location of source and lumped element and their mathematical inclusion in Helmholz equation.

of SSN. From a classical, low frequency, circuits point of view, the placement of lumped capacitors across the board has the effect of "shorting" any surges of currents, or, viewed differently, reducing the inductance, and hence the overall impedance of the board. However, recent publications and reports [12], [18] have unequivocally demonstrated that the leads of capacitors introduce a small, yet significant amount of resistance and inductance that can no longer be ignored, especially when the frequency increases beyond 500 MHz.

To include lumped impedance into our FDFD model, we adopt the method presented in [19] by simply modifying (1) and inserting a field-controlled (or equivalently, voltage-controlled) current source at the location of the lumped element. This model, in effect, represents the voltage-current relationship in the impedance that describes the capacitor. (In classical electromagnetic terms, the lumped element is considered as a boundary condition).

The resulting equation for a given impedance location is given by

$$\nabla^2 E_z(r) + k^2 E_z(r) = \frac{hE_z}{Z_c(\omega)A}\delta(r - r_z) \tag{5}$$

where h is the dielectric thickness, $Z_c(\omega)$ is the total impedance of the capacitor, r_z is the location of the lumped element, and A is the area of the FDFD cell.

Equation (5) has the flexibility to incorporate any user specified lumped element. For example, using a series R-L-C circuit as a load, we have

$$Z_c(\omega) = R + j\omega L + \frac{1}{j\omega C}$$

which leads to the following system equation:

$$\nabla^2 E_z(r) + k^2 E_z(r) = \frac{hE_z}{A}\left(\frac{j\omega C}{1 - \omega^2 LC + j\omega CR}\right) \times \delta(r - r_z). \tag{6}$$

Fig. 5 shows the FDFD Cartesian grid indicating the location of the current source and lumped element and their corresponding representation in Helmholz equation.

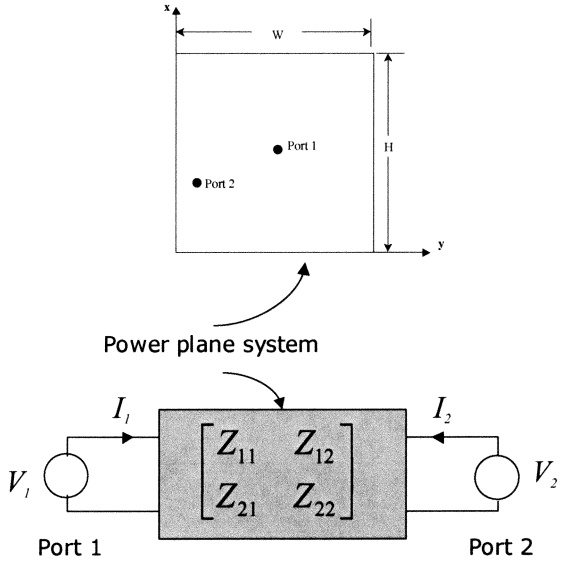

Fig. 6. Two-port network representation of the power plane system.

IV. Numerical Simulation

One of the key fundamental parameters that influence the total effective inductance of the board is the topology of the board. The effect of topology on inductance is gauged by measuring the resonant frequencies of the board. These resonant frequencies indicate the potential of the board to trap electromagnetic energy at specific frequencies. For instance, if the clock frequency or one of its major harmonics falls into a resonant frequency of the board, then the potential for significant cross-talk and interference increases. These resonant frequencies can be calculated directly by solving for the eigenvalues and eigenfunction of the open cavity structure. However, the validity of the numerical model can be better substantiated if the model is constructed to produce calculations that can be directly correlated to experimental laboratory measurements.

S parameter measurements can easily be performed in the laboratory using vector network analyzers and are typically used as a reliable procedure to find the resonant frequencies. For instance, let us assume that we have two ports, a feed (source) port which represents the switching device, and a receive port, representing the load. Then the S_{12} represents the capacity of the board to transfer power from the feed port to the receive port. Clearly, at resonance, this capacity increases substantially.

The calculation of the S parameters cannot be performed directly using a two-dimensional solver such as the FDFD method presented in this work. Therefore, we employ the procedure reported in [19], [20]. To this end, we represent the power plane structure as a two-port impedance network as shown in Fig. 6, where the Z parameters are first calculated for two designated ports (feed port and receive port), and then we make the conversion to S parameters based on a 50-Ω transmission line system.

Let us assume that we are interested in the S_{12} parameter between two specific ports, located at (x_1, y_1) and (x_2, y_2), then the Z parameters are first calculated by carrying out two separate simulations for two different source locations while recording the voltage at the receive and feed ports simultane-

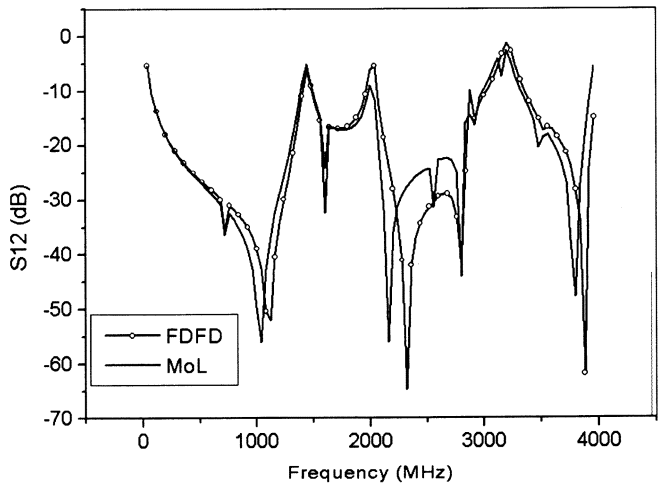

Fig. 7. Magnitude of S_{12} for the 10 cm × 10 cm board obtained using our FDFD model (FDFD) and the methods of lines (MoL) [19].

ously. The S_{12} parameter, for instance, is calculated from the Z parameters using

$$S_{12} = \frac{2Z_{21}Z_0}{(Z_{11}+Z_0)(Z_{22}+Z_0) - Z_{12}Z_{21}} \tag{7}$$

where Z_0 is the characteristic impedance of the feed and receive systems.

For the boards considered in this work, comparison is made to S_{12} measurements where the feed and receive ports are connected to a 50-Ω system. To maximize the compatibility between our numerical models and measurements, we place four 200-Ω resistors around the feed and receive ports in order to simulate the 50-Ω input impedance of the coaxial cables used for measurements at both the feed and receive ports.

The first board considered in this work measures 10 cm × 10 cm, with a dielectric of $\varepsilon_r = 4.4$ and thickness $h = 1.54$ mm. This board was chosen to facilitate comparison with the recently reported method of lines (MoL) [19]. The feed port is located at the center of the boards having the coordinate (5 cm, 5 cm) and the receive port is located at (5 cm, 2 cm). Fig. 7 shows the S_{12} parameter for a frequency range of dc to 4 GHz. A strong agreement is observed between the results obtained using our FDFD algorithm and those obtained using the MoL [19].

A second experiment is considered in which we study a larger board having dimensions 25 cm × 30.5 cm. The feed port is at (12.5 cm, 15 cm) and the receive port at (2.5 cm, 2.5 cm). This board is tested first for SSN without any decoupling capacitors. To test the validity of the FDFD model with respect to lumped elements, we consider the board and populate it with 99 capacitors that are uniformly distributed across the power plane. This example was fully discussed in [12], [18] and was therefore chosen here to enable comparison with laboratory measurements. The capacitors used have $C = 10$ nF, $L = 2$ nH and $R = 50$ mΩ.

The FDFD results for the bigger board, compared to experimental measurements conducted by Archambeault *et al.* [12] are all shown in Fig. 8(a). These results present excellent agreement with other numerical techniques as well as with measurements, thus validating our FDFD model. Fig. 8(b) shows the S_{12} parameter for the lumped elements case while comparison is made to the experimental measurements [12]. We note here that the board losses stemming from the finite conductivity of the copper plates and from the dielectric material are not accounted for in our model. It is highly likely that these losses account for the Q reduction observed in the experimental results.

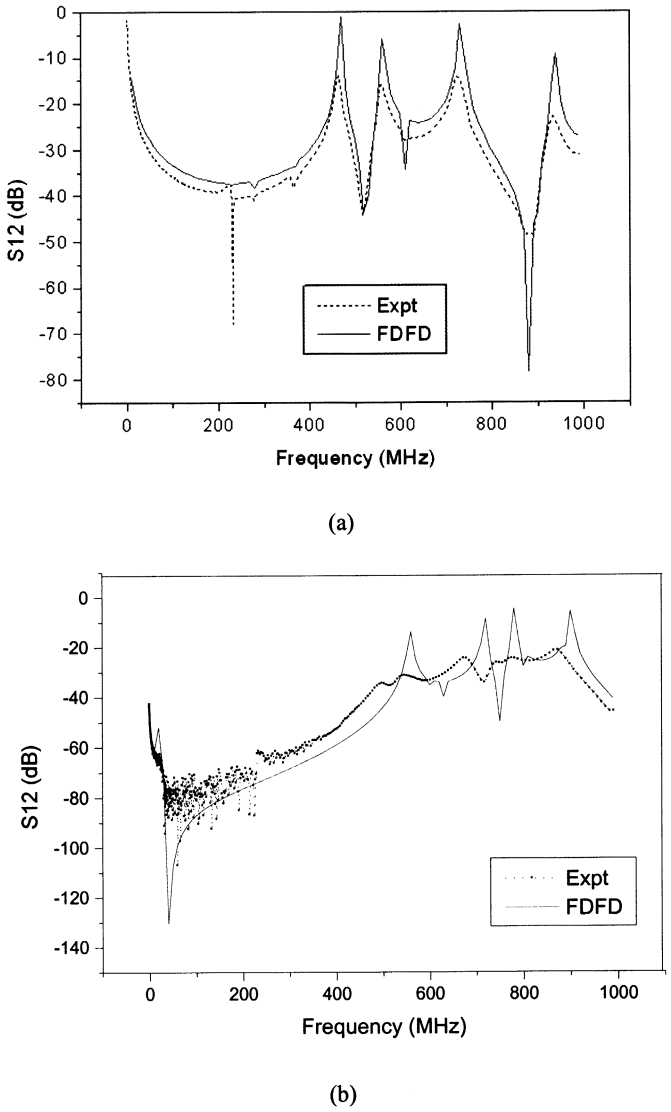

Fig. 8. Magnitude of the S_{12} parameter for the 25 cm × 30.5 cm board obtained using measurements (Expt) and using our FDFD code (FDFD). (a) Without capacitors. (b) With 99 uniformly distributed capacitors of $L = 2$ nH, $R = 50$ mΩ and $C = 10$ nF.

From the simulation results presented, we concluded that the FDFD model including lumped elements compares very favorably with empirical measurements. The model is very simple to implement and can be optimized, as was the case in this work, to run on a sparse matrix solver, thus reducing the solution time considerably. For instance, on a Pentium III microprocessor, 100 frequency points generated for Fig. 7 required only 1.5 h of execution time.

The suppression of the resonant peaks in the power plane due to the introduction of decoupling capacitors is evident by inspection of Fig. 8(a) and (b). But this is true only for frequen-

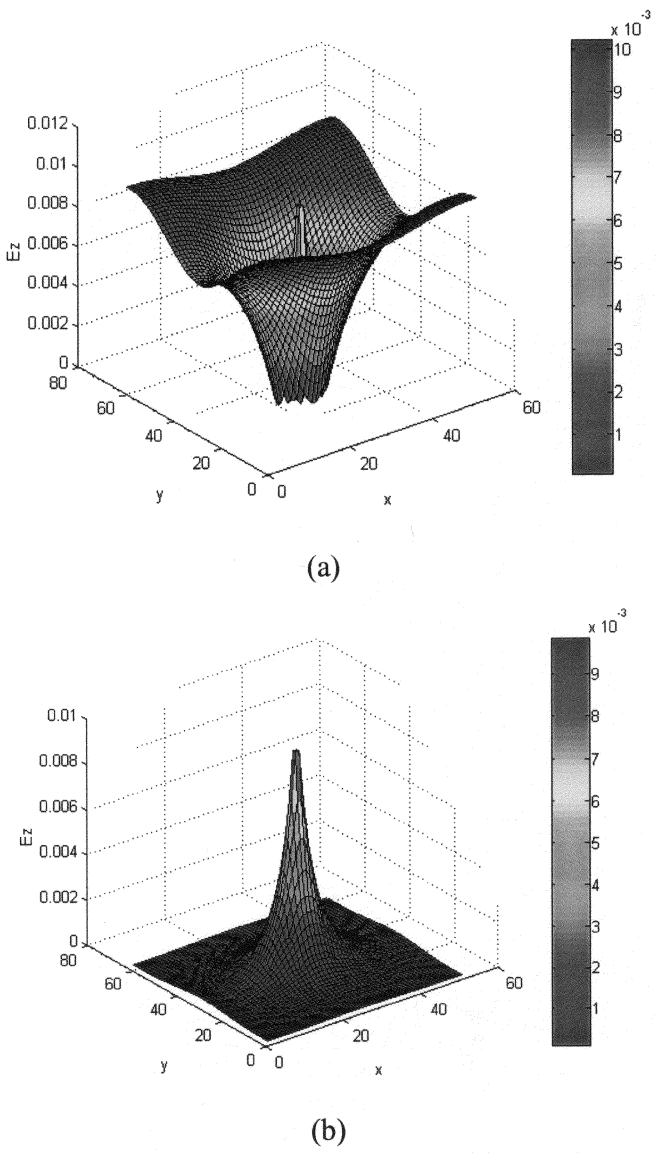

Fig. 9. Electric Field Distribution for the 25 cm × 30.5 cm board at 200 MHz. (a) Without capacitors. (b) With 99 uniformly distributed capacitors of $L = 2\ \mathrm{nH}$, $R = 50\ \mathrm{m\Omega}$ and $C = 10\ \mathrm{nF}$.

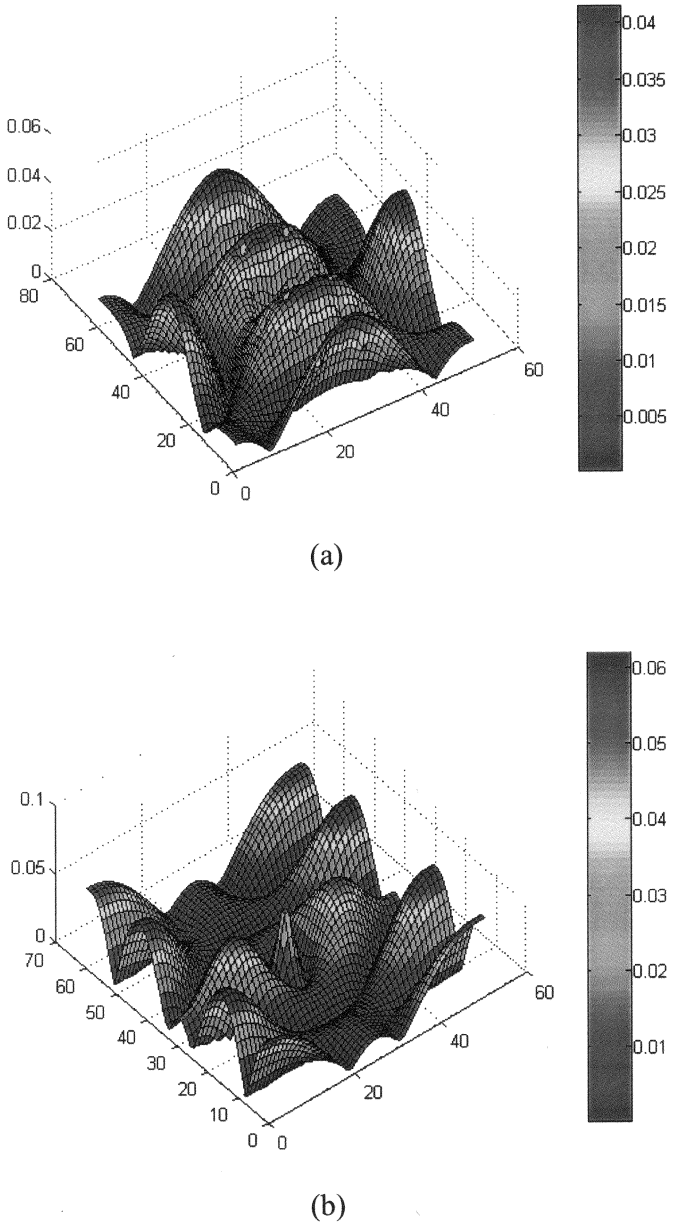

Fig. 10. Electric Field Distribution for the 25 cm × 30.5 cm board at 1 GHz. (a) Without capacitors. (b) With 99 uniformly distributed capacitors of $L = 2\ \mathrm{nH}$, $R = 50\ \mathrm{m\Omega}$ and $C = 10\ \mathrm{nF}$.

cies up to 450 MHz. The addition of lumped capacitors has little effect on damping the resonant frequencies over the higher frequency range. This is attributed to the lead inductance, which dominates the capacitor impedance as the frequency increases. To highlight the capacitor limitation over the higher frequency bands, we show a contour plot of the field distribution for two frequencies for the 25 cm × 30.5 cm board. Fig. 9 shows the field distribution within the board at 200 MHz for the cases with and without the capacitors. Clearly, these plots reveal a significant reduction in the field values across the board except, of course, where the source is located. The case for a higher frequency point, selected at 1 GHz, however, reveals a completely different outcome. Fig. 10 shows that for the 1 GHz frequency, the effect of the 99 distributed capacitors seems to be very minimal, aside from shifting the peaks of the field to different locations.

Two techniques that have been used previously to mitigate switching noise are considered here. The first consists of using a wall of capacitors that encircle the noise source [1]. The second consists of surrounding the entire perimeter of the board with capacitors, while connecting each capacitor with a resistor in series [21]. To study the effectiveness of these technique on the case of the 25 cm × 30.5 cm board, first, we placed a wall of 40 capacitors having the same values as before ($L = 2\ \mathrm{nH}$, $R = 50\ \mathrm{m\Omega}$ and $C = 10\ \mathrm{nF}$) on a $2'' \times 2''$ square perimeter surrounding the feed port located at (12.5 cm, 15 cm). In the second case, a total of 110 capacitors were placed uniformly along the perimeter of the board. The series resistance used is $5\ \Omega$.

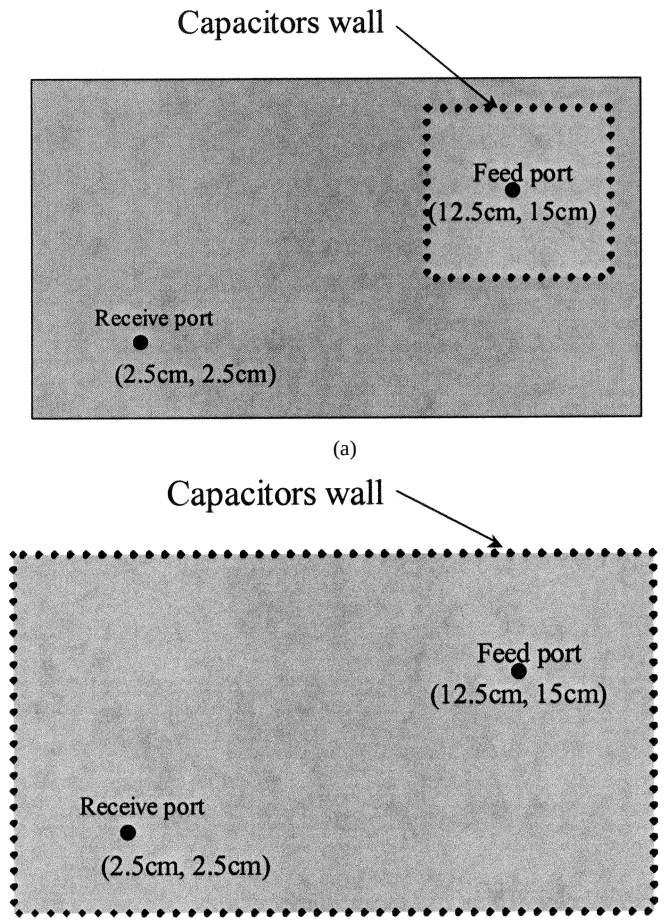

Fig. 11. (a) Wall of capacitors placed around the switching source at port 1. (b) Wall of capacitors placed around the perimeter of the board.

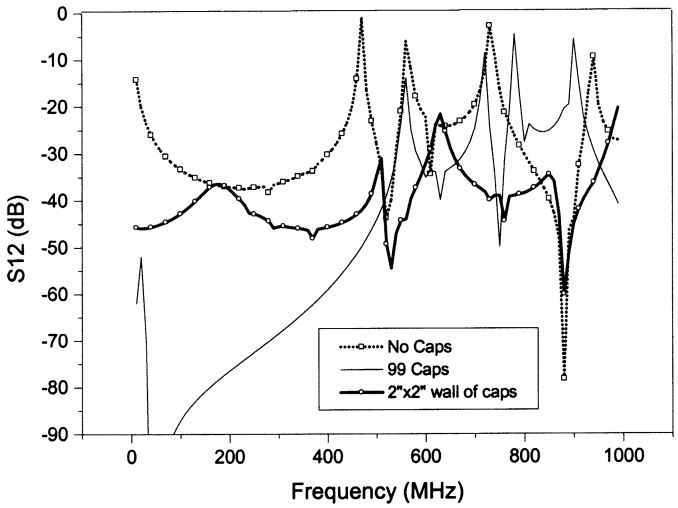

Fig. 12. Magnitude of the S_{12} parameter for the 25 cm × 30.5 cm board using FDFD for the case with no capacitors (No Caps), 99 uniformly distributed capacitors (99 Caps), and a $2'' \times 2''$ wall of capacitors around the source ($2'' \times 2''$ wall of caps).

Fig. 11(a) and (b) show the capacitor placements for each of these two different techniques. Figs. 11 and 12 show the results from each of these techniques while comparison is made

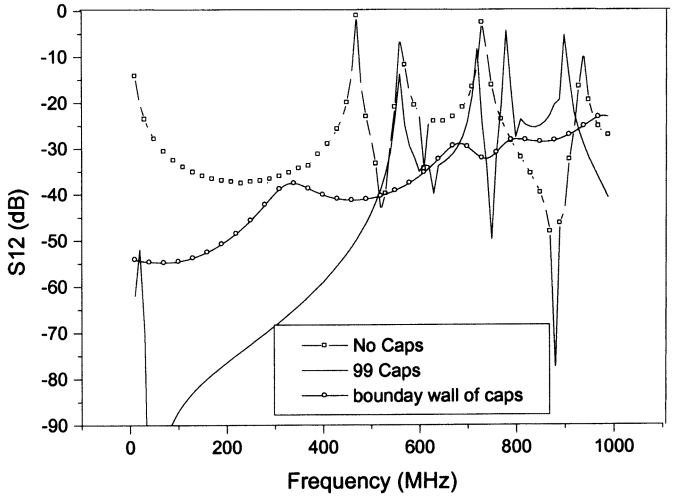

Fig. 13. Magnitude of the S_{12} parameter for the 25 cm × 30.5 cm board using FDFD for the case with no capacitors (No Caps), 99 uniformly distributed capacitors (99 Caps), and a wall of capacitors that is placed on the perimeter of the board (boundary wall of caps).

to the cases of board without capacitors and board with the 99 distributed capacitors. Observation of these results indicates that the placement of 110 perimeter capacitors gives more uniform suppression of resonance in comparison to the cases of 99 distributed capacitors and the internal wall of 40 capacitors. It should be noted that the placement of 110 capacitors also calls for the placement of additional 110 resistors, which increases the cost of this technique. On the other hand, however, the placement of capacitors on the external boundary of the wall frees the board space for placement of other components (see Fig. 13).

V. Conclusion

A simple and efficient FDFD algorithm was developed that can simulate simultaneous switching noise effects and predict the performance of decoupling capacitors in mitigating switching noise. The model was developed to include lumped elements and was optimized to take advantage of the sparse structure of the FDFD matrix. The FDFD model results in simulation time that is considerably faster than required by full-wave three-dimensional algorithms such as the FDTD method. The code was validated by comparison to other numerical techniques and to laboratory measurements.

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