Effects of Microwave Interference on MOSFETs, Inverters, and Timer Circuits

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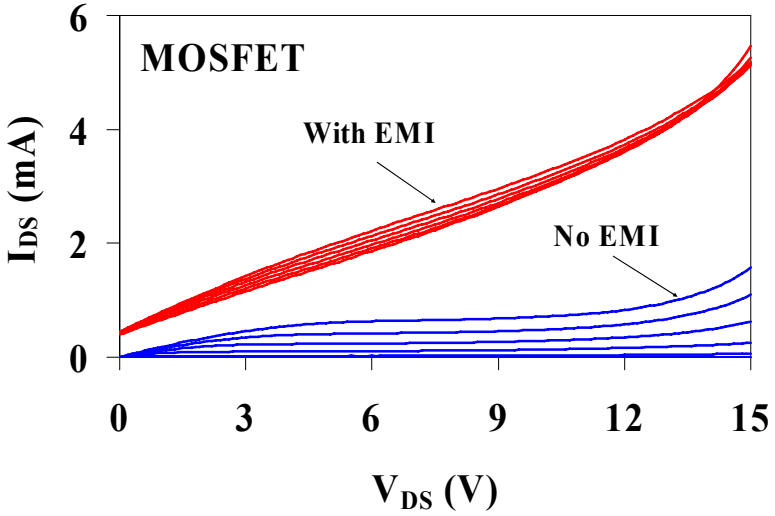
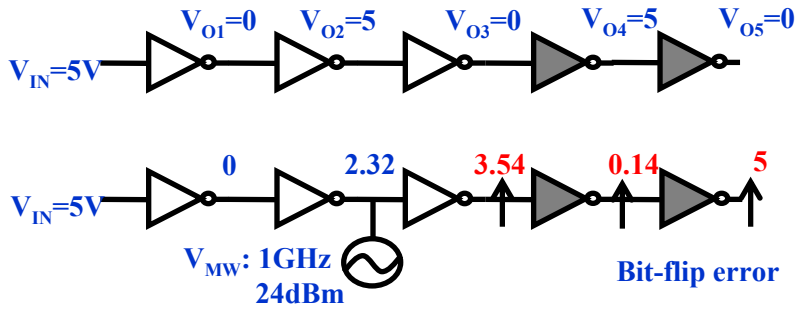
- **Designed and fabricated** individual MOSFETs, inverters, cascaded inverters, and timer circuits used in automotive and aircraft industry. Studied the effects of microwave interference from 0-24dBm and 1-5GHz.
- **MOSFET Effects**: All parameters ($I_{D,}$ g_m, r_O, breakdown) severely affected.
- Most effective ***frequency*** region 1GHz. Intrinsic gate and drain capacitances become a ***by-pass path*** to ground at higher frequencies.
- ***Hard failure*** in sub-micron devices due to ***gate oxide failure*** at levels >18dBm.
- **INVERTERS:** ***Noise margins*** compressed, increased power dissipation. ***Bit errors*** due to noise margin compression. ***Power dissipation*** at stand-by due to incomplete ON-OFF function affects power distribution from power rails and causes local soft or hard errors with entire system failure.
- **INVERTER DYNAMIC OPERATION:** Increased propagation delays, increased short-circuit currents, and dynamic power dissipation.

  Analytical Parameter extraction method developed to extract output voltages/currents, delays, and dynamic power dissipation from measured load-line characteristics.

  Dynamic power dissipation increased by 184% due to increased short circuit current during switching. Results in soft/hard errors and hard failure from excess current on device contacts and interconnects not designed to handle increase.





CASCADED INVERTERS: ***Bit-flip errors*** due to loss of noise immunity in the digital system.

Pulsed Microwave Interference

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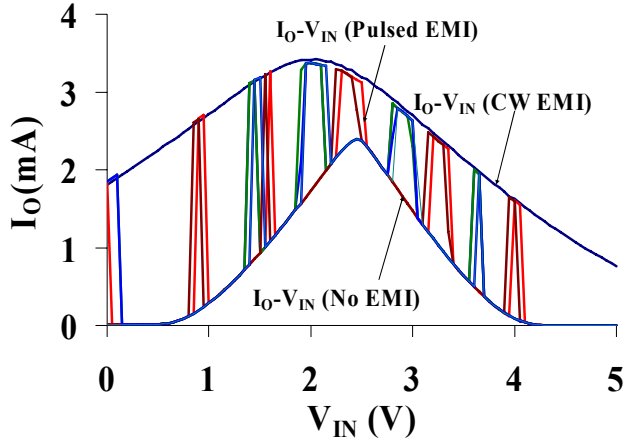
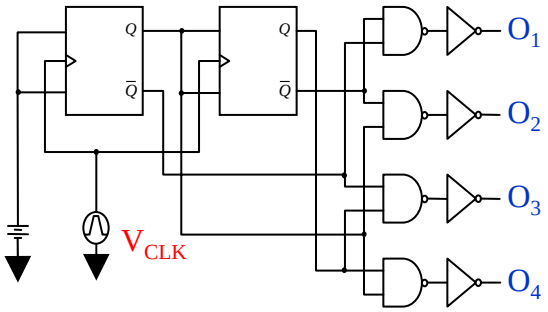
- **INVERTERS:** New ***bit-flip*** errors observed when V_{IN} approaches the threshold voltage (V_{THN}) of the n MOS transistor. Output voltage ***latch-up*** to 1.24V and ***parasitic bipolar action,*** is observed .
- Comparison between pulsed and CW measurements showed no significant thermal contribution from microwave interference.
- **TIMER CIRCUITS:** Microwave interference resulted in reduced pulse width, period, and irregular timing at the output voltages giving critical soft errors, due to substantial degradation of the dynamic operation (output voltage swing and propagation delay changes) of the CMOS inverters, and NAND gate that the *CLK* port of the timer consists of. (collaboration with J. Volakis)
- **SUMMARY:** Fundamental units of electronic IC's were studied and operational parameters identified that revealed critical vulnerabilities under interference. On the basis of our findings a main component of automotive IC, a timer circuit, was studied and characterized. Larger IC systems will be examined to fully understand the effects of interference.



Microwave pulse, 1.5ms of width, and 200ms of period.



Timer circuit