EM Effects on Semiconductor Devices
Gates and Integrated Circuit Interconnects

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EM Effects on Semiconductor Devices
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Goal: Through modeling and experiment characterize microwave coupling on integrated circuits and its effect on device and circuit performance.

Method: Develop modeling tools to analyze and predict effects on devices, fundamental circuit blocks, and interconnects. Base modeling tools on Semiconductor Equations and Schrödinger Equation and Maxwell's Equations.

Verify with experiments: Chips fabricated through MOSIS
Outline

EM Coupling: Levels Investigated
Task 1: Device Level
Task 2: Gate Level (Inverters)
Task 3: Interconnects and Passive Elements
Task 1: EM Coupling to Semiconductor Devices

- EM coupling may induce large voltages on semiconductor device terminals inside IC’s.
- Large terminal voltages can damage devices permanently and cause upsets.
- Most modern IC’s are composed of MOSFETs.
- Pentium IV contains 40 million nanoscale MOSFETs.
- MOSFETs are exceptionally vulnerable.
- Task 1 focuses on detailed modeling of MOSFETs to understand their internal mechanisms of EM induced failure.
MOSFET Cross-Section and Illustration of Vulnerabilities: Oxide and Avalanche Breakdown

Problems:
- Scaling to the nanometer gate length requires oxides less than 20 Angstroms.
- Such thin oxides give rise to such large gate current that devices will not function.
- Large internal fields cause impact ionization, avalanching and damaging filaments.
- Problems especially important for EM coupling, which can induce large voltages to Gate and Drain Electrodes!
Developed Quantum Device Simulator to Investigate Internal MOSFET Subject to Large Coupled EM Terminal Voltages

Solve QM Device Equations Numerically. Inputs are device structure, doping profile & basic physics.

Device Doping Profile

Electron Transport Physics Include:
- Acoustic & Optical Phonons
- Band Structure
- Ionized Impurities
- Impact Ionization & Breakdown
- Surface Roughness
- Gate Current and Oxide Breakdown
Quantum Device Modeling Gives Internal Fields, Currents and Problem Spots:

Internal MOSFET Avalanche Rate

Using the new simulator to model EM induced avalanche breakdown
- Results indicate 2V on drain of 0.1µm causes excessive electron-hole pair generation peak in channel.
- Simulations agree with experiment on resulting substrate current
- Excessive substrate current causes permanent filament damage

Resulting Parasitic Substrate Current
The final gate leakage current will be the summation of the tunneling and thermionic current

\[ J_{\text{gate}}(x) = J_{\text{tu}}(x) + J_{\text{th}}(x) \]

Where tunneling current

\[ J_{\text{tu}}(x) = \int_{0}^{E_{\text{peak}}} f(\xi, x) g(\xi) v_{\perp}(\xi) T_{\text{tun}}(\xi, x) d\xi \]

And thermionic current

\[ J_{\text{ther}}(x) = \int_{E_{\text{peak}}}^{\infty} f(\xi, x) g(\xi) v_{\perp}(\xi) T_{\text{ther}}(\xi, x) d\xi \]

\[ J_{\text{gate}} = \text{Gate Current Density} \]
\[ f = \text{Distribution Function} \]
\[ g = \text{Density of States} \]
\[ T_{\text{tu}} = \text{Tunneling Probability} \]
\[ T_{\text{ther}} = \text{Thermionic Probability} \]
Boltzmann-Schrödinger/Spherical Harmonic Device CAD
Results: Gate Current (WKB Method)
Gate Tunneling Current
I_g vs. Time
DC and Transient

Transient does not increase
gate current density, and
thus probably does not
increase probability of
breakdown.
Resulting Electrostatic Potential inside 0.14µm MOSFET: Bias Conditions for Oxide Breakdown

\[ V_G = 2.8\text{V} \quad V_D = 1.4\text{V} \quad V_S = V_B = 0\text{V} \]

If \(|E_y| > 7\text{MV/cm}\) => Oxide Breakdown

Device Simulations predicts induced gate voltage of 2X supply causes MOSFET oxide damage
Experimental Chip for EM Coupling and Gate Current Measurements.

Designed at UMD Fabricated by MOSIS

NFET, 150 µ by 60 µ (100 times minimum size)
Task 2. EM Effects on Gates

Differential equation based modeling of EM effects on inverter circuits

- Stage 1: Develop simulation tool.
- Stage 2: Use tool to analyze distributed effects of EM GHz range coupling on fundamental computer chip circuit elements.
Developed Distributed Circuit Simulator
Applied to Inverters

**DD Equations**
\[ \nabla^2 \phi = -\frac{q}{\varepsilon_{Si}} (p - n + D) \]
\[ \frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n - R_n + G_n \]
\[ \frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \vec{J}_p - R_p + G_p \]

**Supplementary DD Equations**
\[ \vec{J}_n = -q\mu_n n \nabla \Phi + q\mu_n V_T \nabla n \]
\[ \vec{J}_p = -q\mu_p p \nabla \Phi - q\mu_p V_T \nabla p \]

**Coupled Discretized DD Equations**
Coupled Discretized DD Equations are solved at each mesh point

**CMOS Inverter (CMI)**
Lumped KCL equation check at the output node and using the KCL equation, the output guess is updated for the next iteration, \( V_o^{i+1} \):

\[ I_{DN} - I_{DP} + I_{R_L} + I_{C_L} = 0 \]
\[ A_n + B_n V_o^{i+1} + A_P + B_P V_o^{i+1} + \frac{V_o^{i+1} - V_{SS}}{R_L} + \frac{V_o^{i+1} - V_o^i}{\Delta t} = 0 \]
\[ V_o^{i+1} = \frac{V_{SS} + V_o^i \frac{R_L C_L}{\Delta t} - (A_n + A_P)R_L}{1 + \frac{R_L C_L}{\Delta t} + (B_n + B_P)R_L} \]
Modeling 20GHz, 1V Coupled to 0.1µm Inverter
- Output follows input reduced by 20%
- Enough to cause bit errors.

Simulated Coupled Input

Simulated Coupled Output
Modeling 20GHz, 1V Coupled to 0.1μm Inverter
- 1pF & 10pF Load Caps.
- Output does not follow input
- Inverter transitions to average output voltage state (C discharge)
Modeling 20GHz, 1V Coupled to 0.1µm & 0.25µm Inverters

- Output follows input but with reduced amplitude in 0.25
- Bit errors can still occur in larger device but may be less likely
Task 3. Interconnects and Passive Elements

Developed Finite Difference Time Domain Alternating Direction Implicit Method (FDTD-ADI) for Solving Maxwell’s Equations on Chip.
Model Verification

- 2D guided-wave propagation
- Excitation frequency = 50 GHz;
- Metal conductivity = $3.9 \times 10^7$ S/m.
- Able to resolve skin current wave pattern inside metal

$$\propto \cos(k_z z + y/\delta) \exp(-y/\delta)$$

$\delta$: Skin depth.
- Y axis unit is 0.1um;
  Z axis unit is mm.
Simulating Signal Propagation along Metal-Insulator-Silicon-Substrate (MISS) Interconnect

Cross Section of Simulated MISS Structure

- Metal
- SiO2
- Vacuum
- Lossy Silicon Substrate

Dimensions:
- 555 um
- 6 um
- 555 um
- 500 um
- 1.8 um
- 2 um
- 500 um
Simulation Performance

• Non-uniform grid in the cross section; smallest grid size in the cross section is 0.1 um. Uniform grid = 25 um in the propagation direction.

• Simulation $\Delta t = 2\times10^{-13}$ sec. Courant’s limit is $\Delta t < 0.33\times10^{-15}$ sec

• Simulation time is 3-4 hour on a PC for 1000 step simulation.

• Outer boundary condition: Mur’s first order
Voltage observed at different Z locations along the MISS Strip

- A fast 1V, 20psec digital pulse of risetime = 2ps is excited
- Substrate doping $n = 10^{17} \text{/cm}^3$
- Metal conductivity = $5.8 \times 10^7 \text{ S/m}$.
- Shows digital signal losses and dispersion.
Cross Section of $E_y$ field

- Electric field concentrates inside the SiO$_2$ layer.

Cross Section of Current $J_z$ inside Metal

- X, Y units are 0.1 um.
- Skin depth effect.
- Metal edge effect.
Snap-shot of Substrate Current

Top view

- Red and blue shade correspond to rising and falling of the signal.
- Top view shows potential interference and coupling in lateral direction (tenth mm scale).

Side view

- Side view shows current penetration to the substrate.
Signal Propagation with Different Substrate Doping

- $n_1 = 10^{18} \text{ /cm}^3$ (solid)
- $n_2 = 10^{16} \text{ /cm}^3$ (dashed)
- At the skin-effect mode, higher substrate doping conforms signal better.
Simulating EM Coupling between Interconnect Lines in Metal-Insulator-Silicon-Substrate (MISS) Structure

Results: New simulator allows for resolving large variations in grid points. Induced voltage 20% of applied signal even at 20µm apart.
Simulations show extensive coupling through substrate currents.

Substrate Current: Horizontal x-section

Substrate Current: Vertical x-section
EM Coupling Mechanisms in IC

Noise Injection:
- Capacitive Injection
- Hot Electron Injection

Noise Coupling:
- Resistive Coupling
- Inductance Coupling

Noise Reception:
- Capacitive Reception
- Threshold Voltage Modulation
IC Chip Layout
Coupling Measurement

Frequency: 50MHz 100MHz 500MHz

Phase Noise:
- 50MHz: -1.5dBC/Hz
- 100MHz: -1.8dBC/Hz
- 500MHz: -2.2dBC/Hz

- 50MHz: 35.4dBC/Hz
- 100MHz: 29.1dBC/Hz
- 500MHz: 12.8dBC/Hz
On-Chip EM Coupling

- Coupling between On-chip Inductors

**Left:** Results from literature and circuit model for coupled on-chip inductors

**Right:** Our test structure (in fab) for measuring coupling between inductors on different metal layers

**Below:** Modeled mutual inductance rising with frequency
On-Chip EM Coupling

- Coupling between On-chip Inductors and Transistors

*Top and left:* Literature results and circuit model for inductor/transistor coupling

*Right:* Our test structure (in fab) for probe-station inductor/transistor gate coupling measurements with two different transistor layouts (transistors are circled in the picture).
On-Chip EM Coupling

**Left:** Layout details for inductor/transistor gate coupling measurements and two different transistor layouts

**Below:** Results of our preliminary test structure (measurements taken with a network analyzer from chip-on-board).
Planar inductor vs. Multilayer inductor

Same net length $\Rightarrow$ same net resistance, but higher inductance.
(four-level multilayer)
Planar inductor vs. Multilayer inductor

Layouts for planar inductor (left) and multilayer inductor (right), in fabrication for probe-station measurements. The total length of the inductors are the same, and the two pictures are of the same scale. Note the much smaller footprint of the multilayer inductor.
Accomplishments

- Task 1: Developed quantum device modeling code
  - Used code to ascertain internal MOSFET vulnerable spots.
  - Found MOSFET drain junction area especially susceptible to avalanching, which can cause breakdown and filament formation leading to permanent device failure.
  - Developed method for modeling gate current and oxide breakdown
  - Calculations predict that induced voltages as little as 2.6V can cause device failure in current device technologies.
  - Voltages necessary for damage will decrease as device dimensions reduce according to semiconductor roadmap.
Accomplishments

• Task 2: Developed distributed CAD tool for modeling multi-transistor circuits.
  – Applied the new tool to modeling inverter switching due to GHz range coupled signals.
  – Simulations show details of fields and current densities of switching inside devices.
  – Simulations show current technology inverters (0.1µm) follow input signal of 20GHz which can cause bit errors. Larger devices (0.25 µm) are less likely to cause bit errors at 20GHz.
  – Capacitive loading (1 – 10 pF) causes inverter circuits to reach indeterminate average state causing bit errors with RC time constant.
Accomplishments

• Task 3: Developed Maxwell Equation based CAD tool for modeling on-chip interconnects and passive structures.
  – New tool overcomes Courant limit and is thus well suited for analyzing chips where resolving mm and µm size structure simultaneously.
  – Applied the new tool to modeling propagation of pulses along IC interconnect transmission lines.
  – Simulations show details of fields and current densities inside semiconductor substrate and metal interconnects
  – Simulations indicate significant losses and dispersion which depend on the doping density of the semiconductor substrate. Higher doping gives rise to less losses.
  – Simulations indicate extensive coupling between interconnect lines. 20% percent coupling is seen on lines as much as 20µm apart.
• Numerous test IC’s designed and fabricated to EM effects on interconnects and devices. Experiments currently being set up.
Publications

Future Work

• Use new device CAD tool to further assess oxide breakdown effects in new and existing technologies.
• Use new circuit distributed CAD tools to further investigate microwave induced switching performance of digital building blocks. Investigate entire microwave spectrum and a wide range of CMOS technologies.
• Apply interconnect CAD tool to further investigate coupling of external microwaves to chip.
• Perform measurements on test chips to further quantify EM – IC coupling. Model experiments with newly developed CAD tools.
• Combine Device and EM CAD tools to develop comprehensive IC distributed simulator.