Experimental Studies of Microwave Interference Vulnerabilities in IC Devices

Agis A. Iliadis

Electrical and Computer Engineering Department

University of Maryland, College Park, MD 20742

Tel:301-405-3651/agis@eng.umd.edu

Graduate Students: Kyechong Kim, L. Liu, X. Wen

Collaboration: T. Firestone, J. Rodgers, N. Goldsman, S. Anlage,

Acknowledgements

Support from AFOSR-MURI is gratefully acknowledged

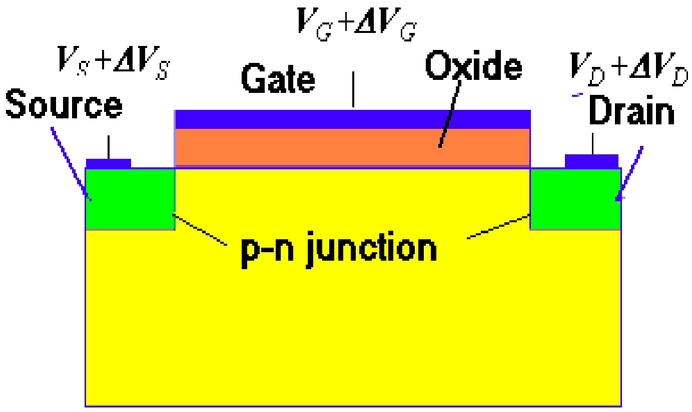
Introduction

- EMI can couple into electronic modules intentionally or unintentionally from high power microwave (HPM), ultra-wide band (UWB), and other sources and cause significant "soft" reversible errors (operational disruption, gain degradation, bit flipping, delay/response, and noise/distortion) and "hard" irreversible errors (gate oxide break-down, junction filamentation, avalanche break-down, metallization, interconnect peel-off and others).
- Protecting by shielding can reduce this hazard but still, connecting wires, micro-slits, and the input/output leads of packaged chips, can become effective inputs to couple the EMI into the integrated circuit, while ESD protection from such sources is not effective enough and in some cases it may even enhance the RF effects on IC devices.
- The project focuses on identifying the effects of high power microwave interference on the fundamental components of integrated circuits (IC's) such as MOSFETs, CMOS inverter gates, and CMOS differential amplifiers, in order to identify vulnerabilities for upset and failure and develop EMI-hardened devices, circuits, and architecture.

N-channel Enhancement-mode MOSFETs

Parameters affected:

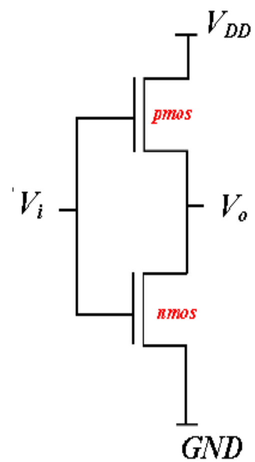
- *Electronic:* I-V, Q point, gm, gain, delay times, ft, fm, s, impedences
- *Physical:* Gate oxide, junction boundaries, metallizations.

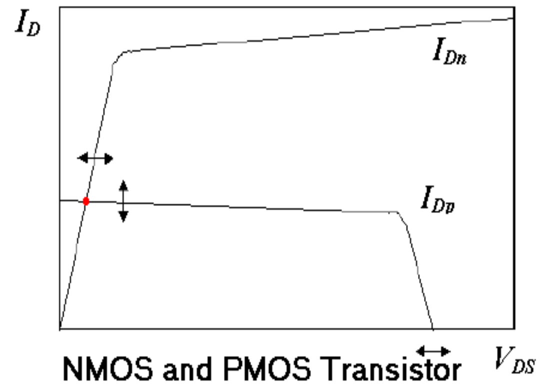


MOSFET-Schematic Diagram

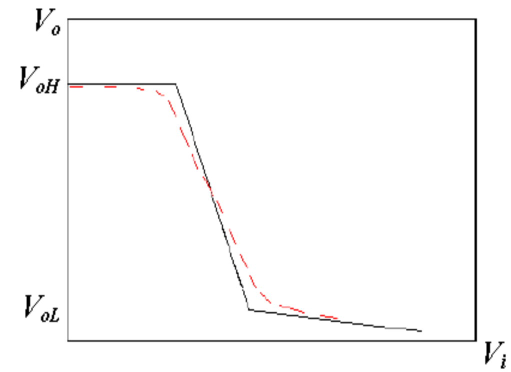
CMOS Inverter Gates

- *Parameters affected*:
- *Electronic:* Affects points of intersection of the I-V lines, transfer characteristic gate, response time and gate performance.
- *Physical:* Gate oxides, junction boundaries, metallizations.





NMOS and PMOS Transistor Characteristics



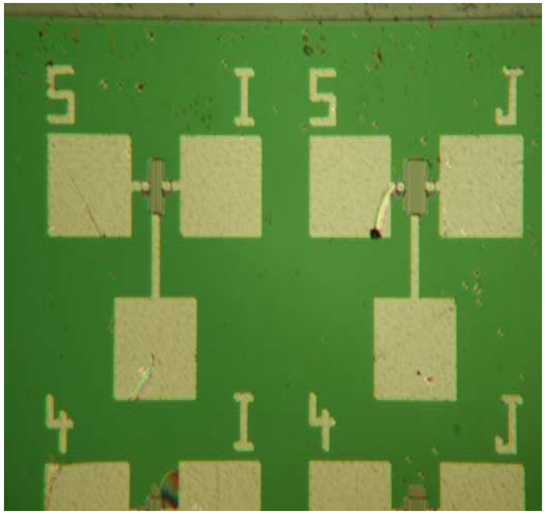
Inverter Transfer Characteristics

Experimental Approach

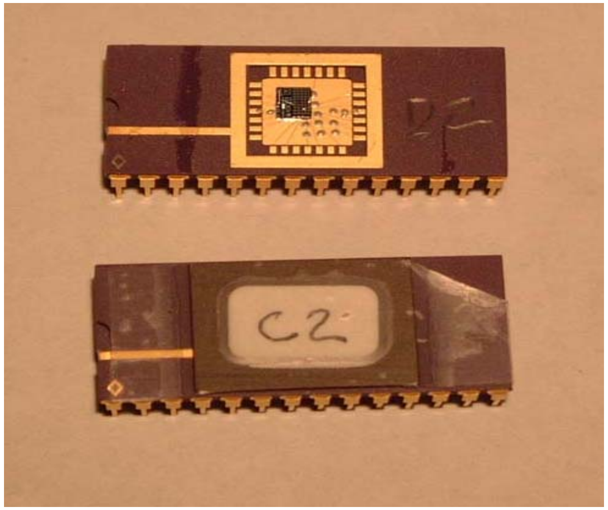
- We focus first on n-channel enhancement mode MOSFETs where microwave interference is injected directly into the input/output leads, and then on inverter gates, gate clusters, and diff. amps (on-going).
- Individual micron gate (2-20 μm) NMOS on (100) 3’ p-type Si wafers were examined at power levels up to 30dBm, after packaging and mounting on board for testing.
- Submicron gate (0.5 μm) NMOS devices were examined at moderate power levels up to 20dBm by direct on-wafer probing, and their I-V and s-parameters were measured.
- A controlled microwave signal of 1 to 20 GHz and 0 to 30 dBm was injected first into the gate, and then into the drain. Output characteristics and s-parameters were measured using a HP 4145 semiconductor device parameter analyzer and HP8510C network analyzer respectively.

Micron Gate NMOS Devices on Chip: Packaged for Microwave Test

Microwave interference injected into the input/output leads of devices



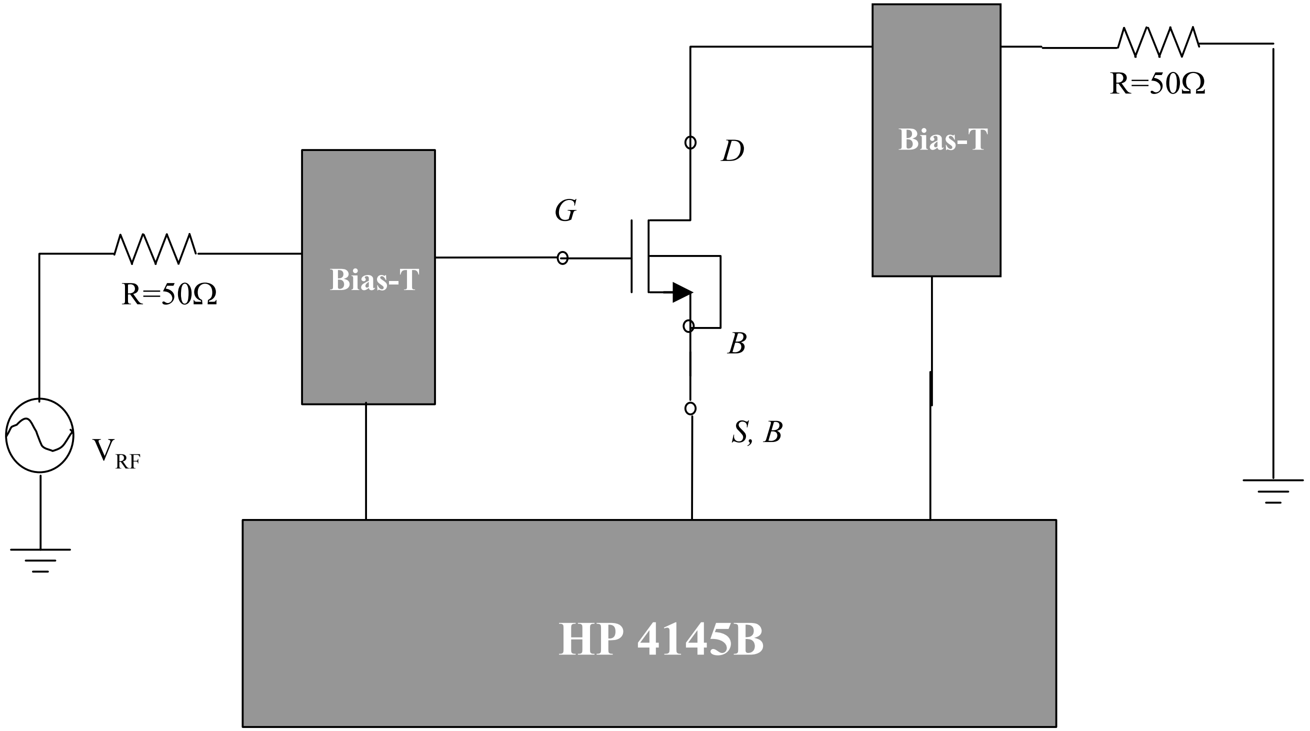
IC Chip Section with MOSFETs



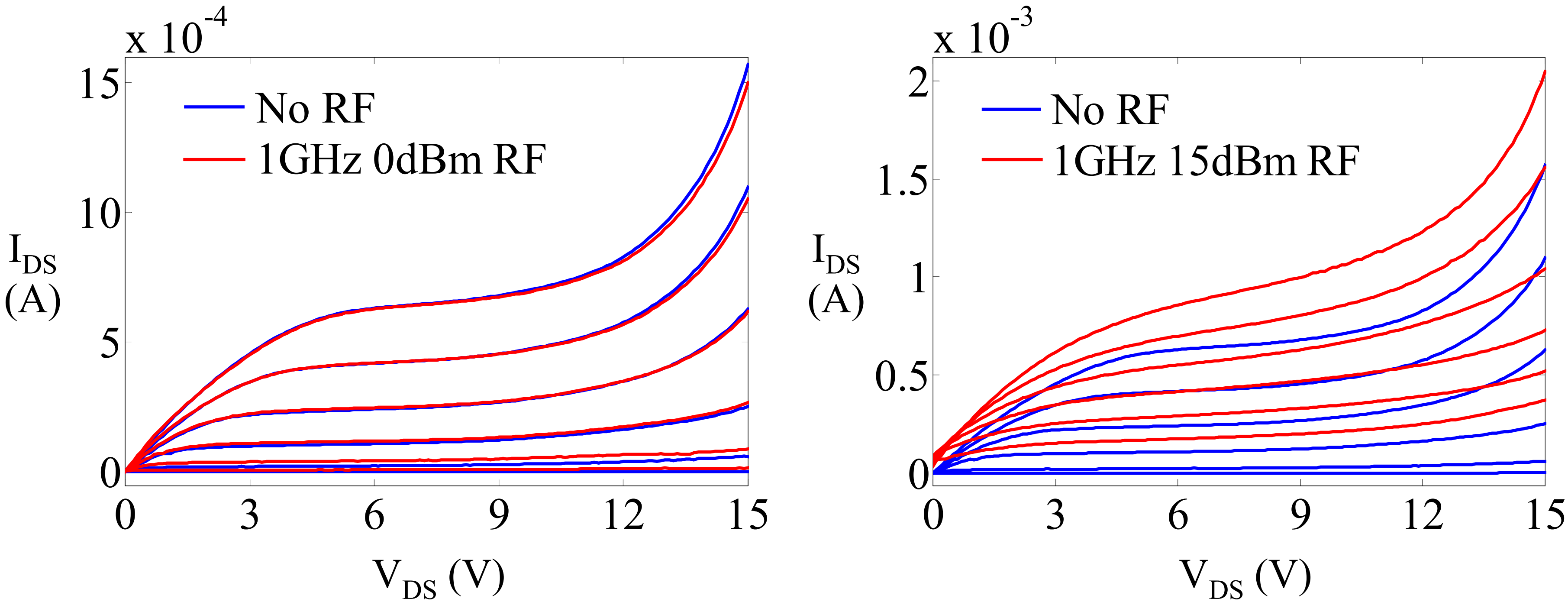
Bonded and packaged IC Chip

- Individual MOSFETs with gate lengths of 2 to 20 um
- Typical operating conditions: V_{GS}=5 V, V_{DS}=7 V
- Packaged chip on PC board for microwave direct injection

Test Set-Up for Direct Injection

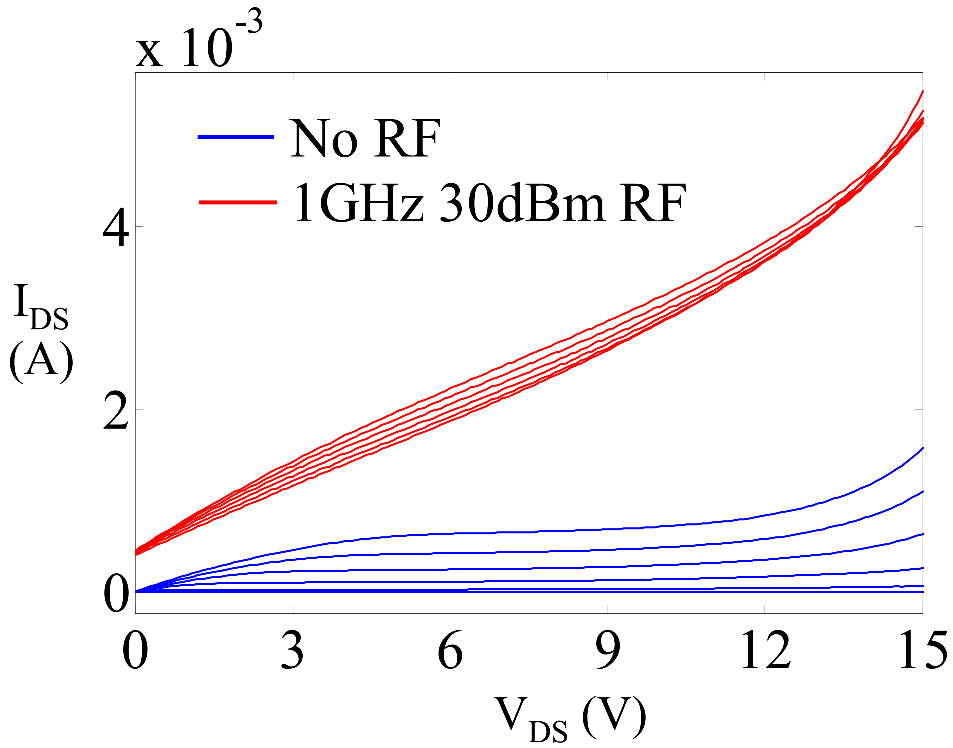


$I_{DS} - V_{DS}$ Output Characteristics Injection to Gate RF Power Effect : 1GHz



- 1GHz 0dBm (1mW) RF injection to Gate : No significant change.
- 1GHz 15dBm RF injection to Gate : I_{DS} current increases significantly & zero point shift is observed to positive I_{DS} current.
- g_m and r_O decrease, g_O increases.
- RF power increase results in I_{DS}, zero point, and g_O increase & g_m and r_O decrease.

I_{DS} – V_{DS} Output Characteristics RF Injection to Gate No RF & 1GHz 30dBm



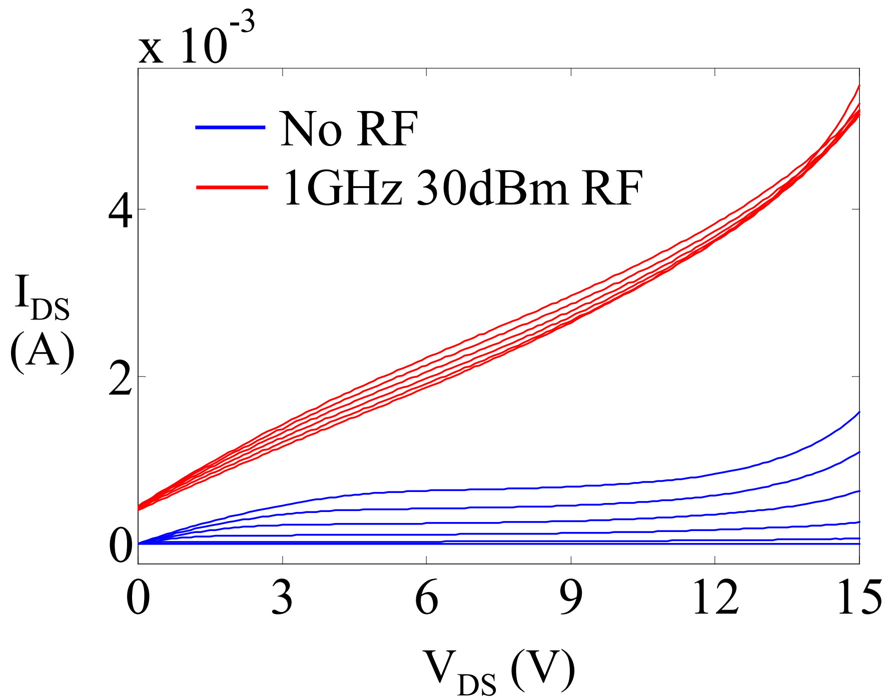
$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}} \quad g_o = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}} \quad r_o = \frac{1}{g_o}$$

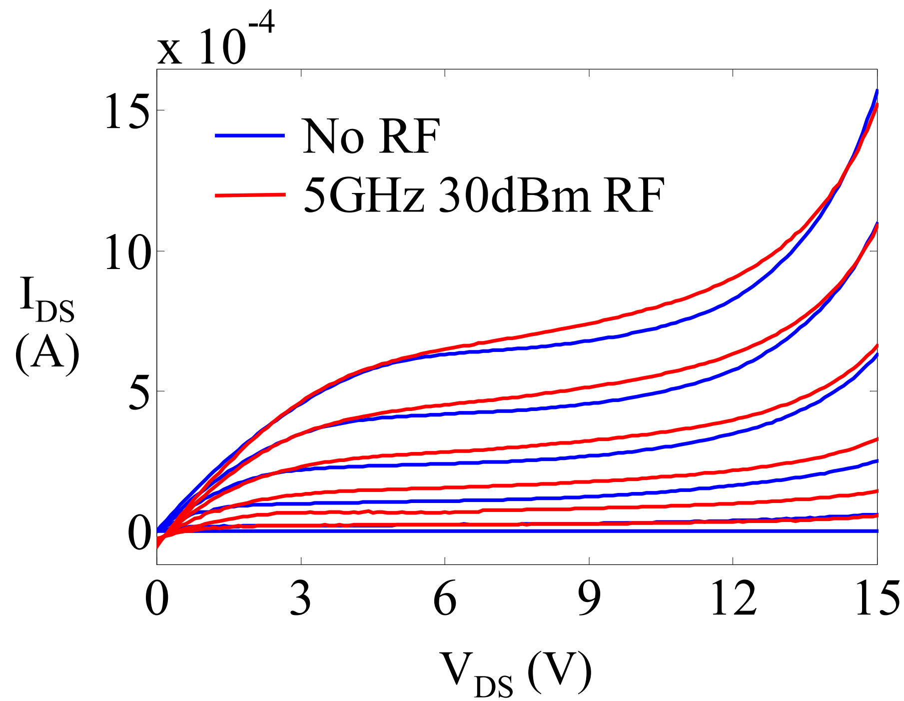
$$g_m \downarrow \quad g_o \uparrow \quad r_o \downarrow$$

- g_m decreases and g_O increases.
- Zero point is raised to significant positive current.
- Saturation severely degraded.
- At higher frequency 5 GHz, power effect is suppressed.

- g_m (Ω^{-1}) : 2.1856×10^{-4} (DC), 9×10^{-5} (1GHz 30dBm), 2.1×10^{-4} (5GHz 30dBm)
- g_O (Ω^{-1}) : 2.0325×10^{-5} (DC), 2.45×10^{-4} (1GHz 30dBm), 3.35×10^{-5} (5GHz 30dBm)
- r_O (Ω) : $49.2K\Omega$ (DC), $4.0816K\Omega$ (1GHz 30dBm), $29.8K\Omega$ (5GHz 30dBm)

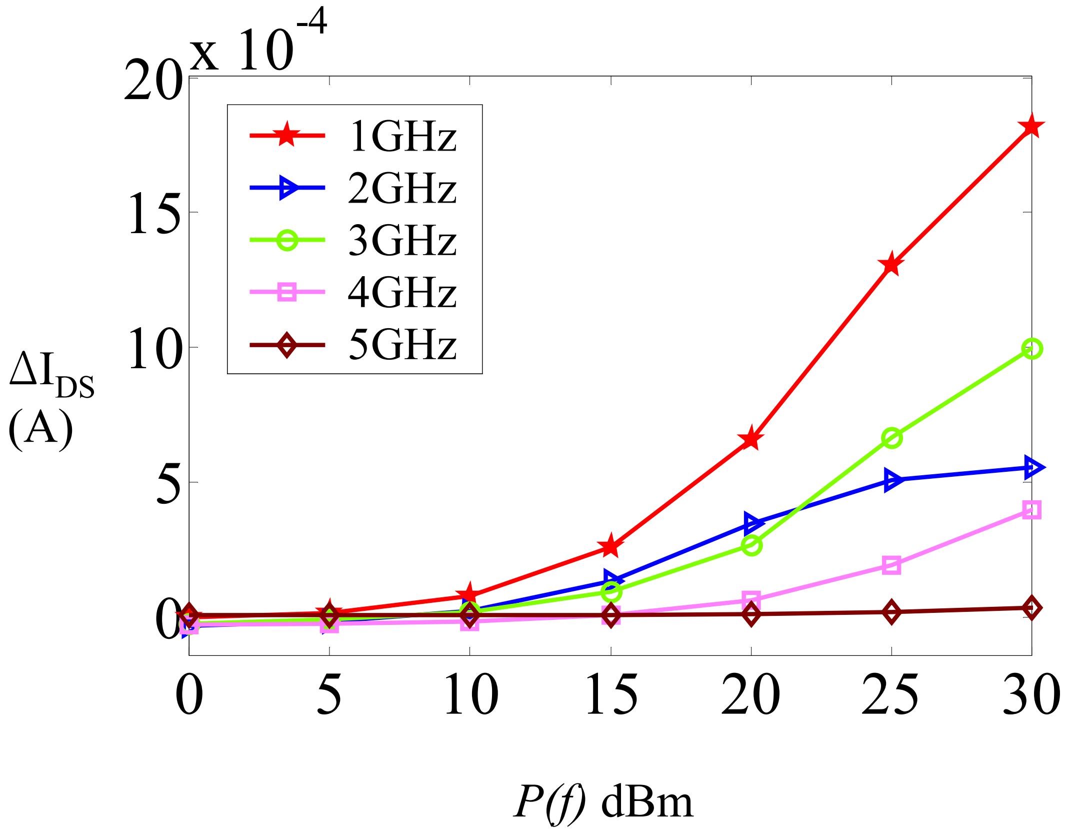
$I_{DS} - V_{DS}$ Output Characteristic Injection to Gate Frequency effect at 30dBm





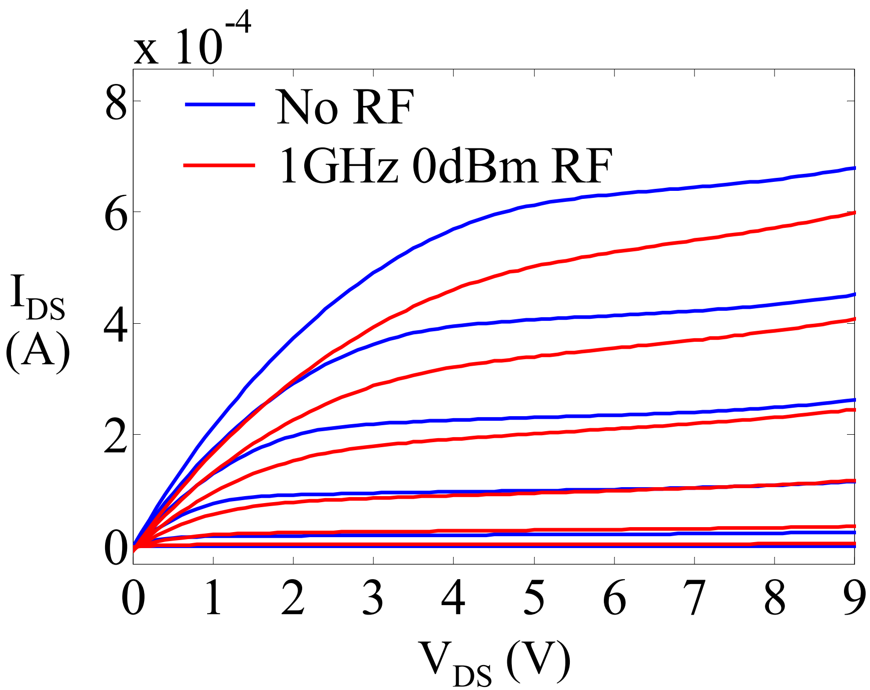
- 5GHz 30dBm RF injection : g_m, r_O ↑ & g_O, zero point, breakdown ↓
- Negative zero point and decrease in I_{DS} at Triode region are observed.
- Frequency increase results in suppressing power effect.

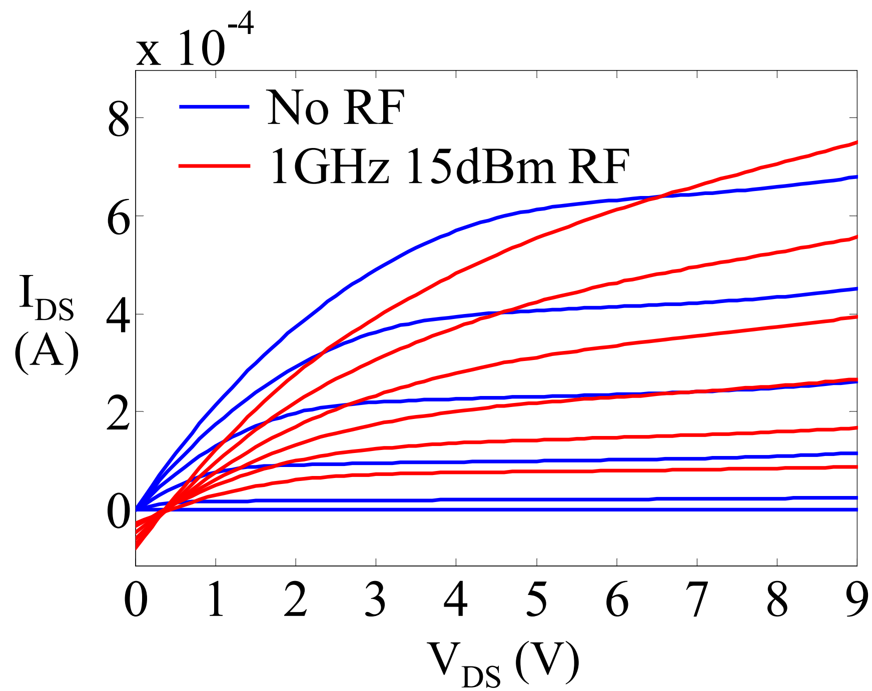
RF Injection to Gate
Drain Current vs Power & Frequency



- ΔI_{DS} vs Power (Frequency).
- RF power range of 0 to 30 dBm with 5dBm step and frequency 1 to 5 GHz. ($\Delta I_{DS} = \Delta I_{DS(RF)} - \Delta I_{DS(DC)}$)
- RF Power effect : ΔI_{DS} increases with RF Power.
- RF frequency effect : ΔI_{DS} reduces with increasing frequency.
- Power effect suppressed above 5 GHz.

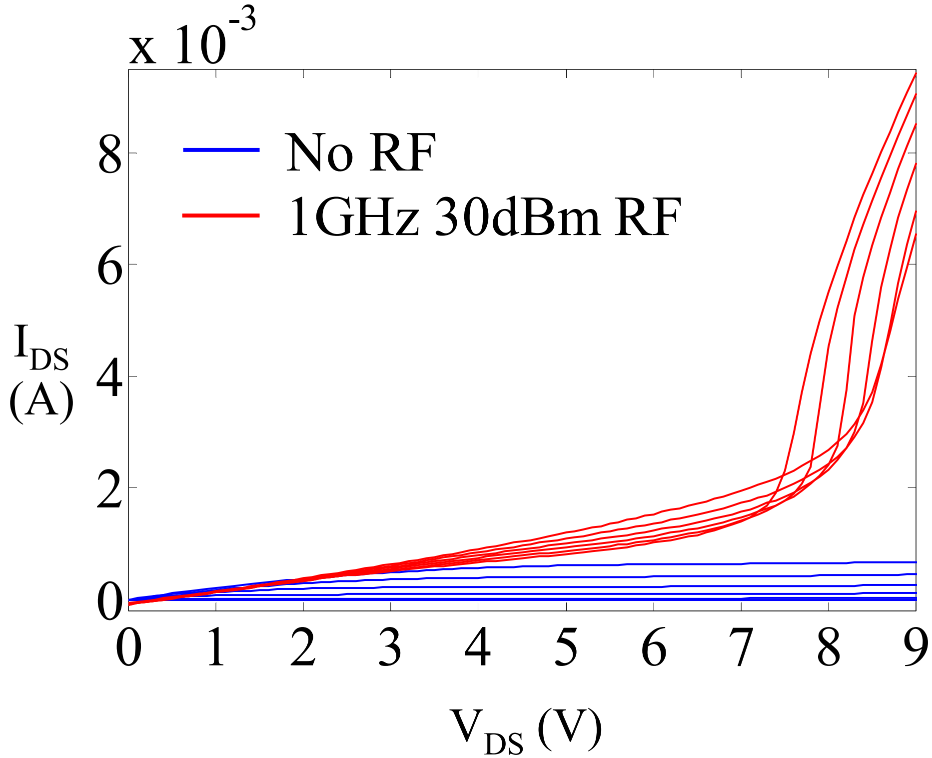
$I_{DS} - V_{DS}$ Output Characteristic Injection to Drain RF Power effect : 1GHz





- 1GHz 0dBm (1mW) RF injection to Drain : I_{DS} decrease observed.
- 1GHz 15dBm injection to Drain : g_m decreases & g_O increases.
- I_{DS} decreases at Triode region, but increases at Saturation region with saturation degradation evident.
- Negative zero point and cross-over is observed.

I_{DS} – V_{DS} Output Characteristic Injection to Drain No RF & 1GHz 30dBm



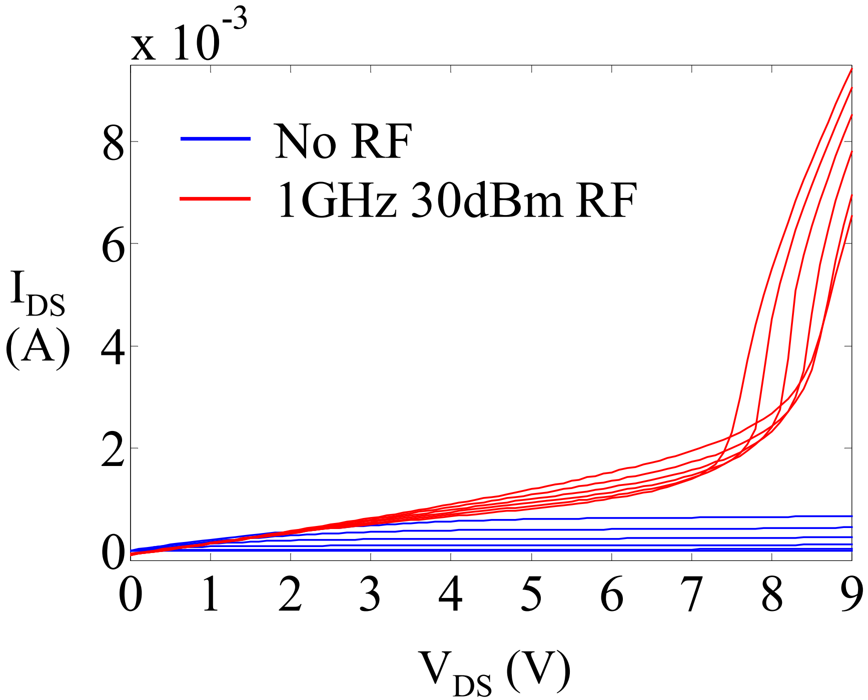
$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}} \quad g_o = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}} \quad r_o = \frac{1}{g_o}$$

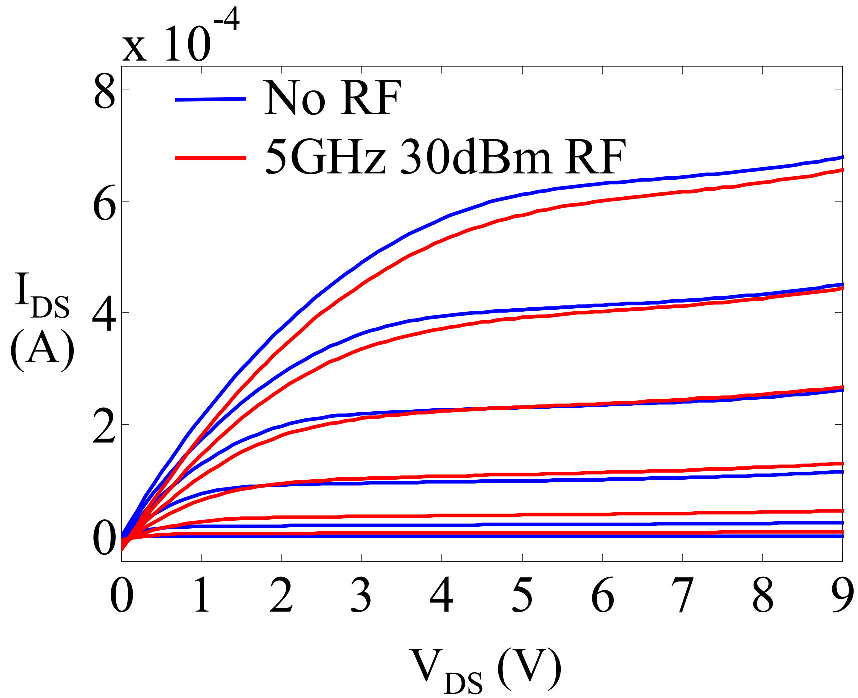
$$g_m \downarrow \quad g_o \uparrow \quad r_o \downarrow$$

- g_m increases close to breakdown and decreases at lower biases.
- g_O increases.
- Zero point goes to negative value.
- I_{DS} decreases at Triode region, but increases at saturation region.
- Saturation Degradation evident.
- Breakdown effects substantially increased with reduced breakdown voltage starting at V_{BD}=7.3V.

- g_O (Ω^{-1}) : 1.581×10^{-5} (DC), 3.75×10^{-4} (1GHz 30dBm), 2.05×10^{-5} (5GHz 30dBm)
- r_O (Ω) : 63.251$K\Omega$ (DC), 2.67$K\Omega$ (1GHz 30dBm), 48.78$K\Omega$ (5GHz 30dBm)

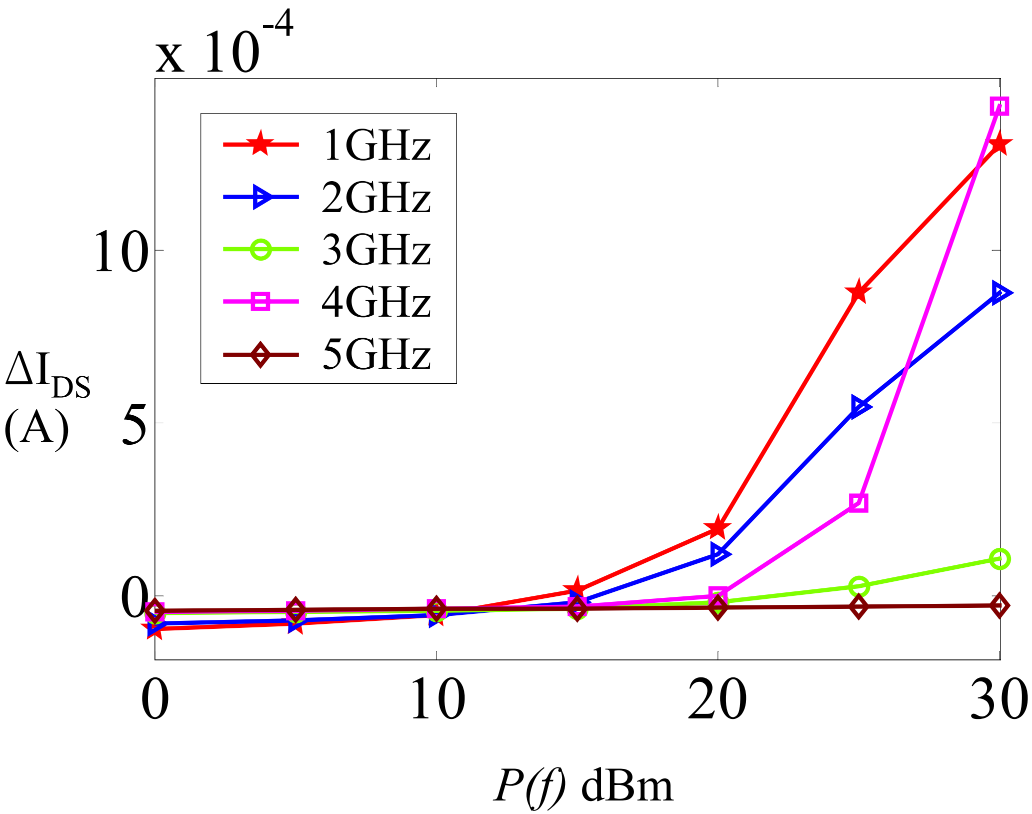
$I_{DS} - V_{DS}$ Output Characteristic Injection to Drain Frequency effect at 30dBm





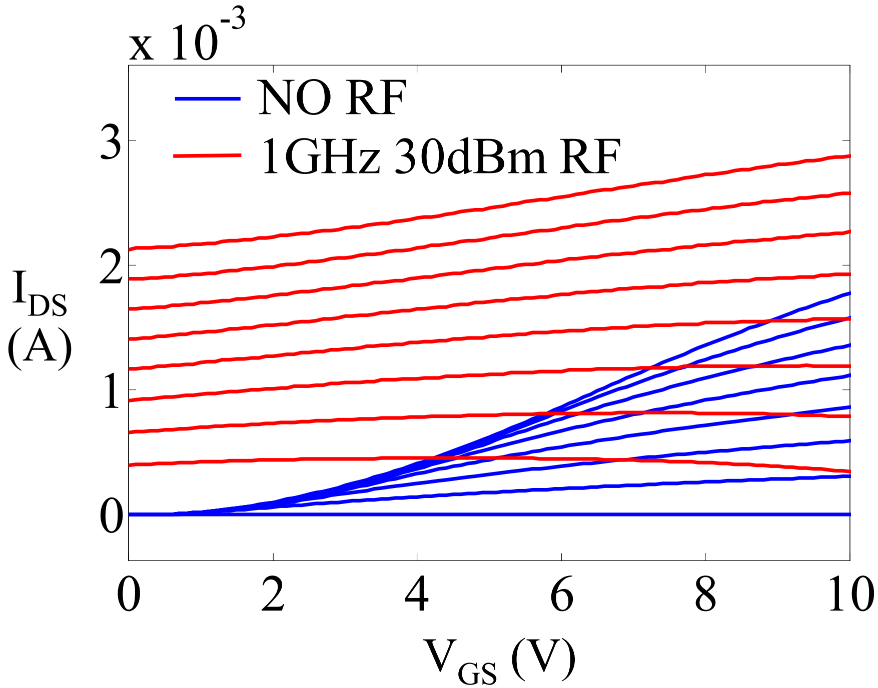
- 5GHz 30dBm RF injection : g_m, r_O ↑ & g_O, breakdown effects ↓
- Zero point from–100μA to –20 μA.
- RF power effect is reduced with RF frequency increases.

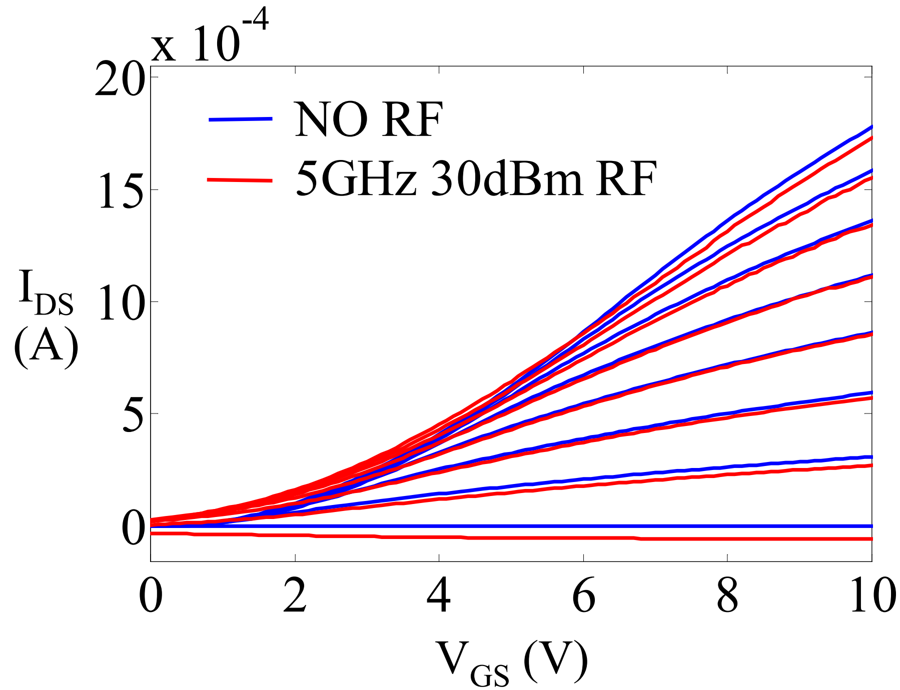
RF Injection to Drain
Drain Current vs Power & Frequency



- ΔI_{DS} vs Power(Frequency).
- RF power 0 to 30 dBm with 5dBm steps and frequency 1 to 5 GHz.
  ($\Delta I_{DS} = \Delta I_{DS(RF)} - \Delta I_{DS(DC)}$)
- Negative ΔI_{DS} is observed with Power up to 10 dBm for all frequency ranges and for frequency above 4GHz for all power ranges.
- Power effect : ΔI_{DS} increases with power.
- Freq. effect : suppresses power effect at or above 4 GHz.

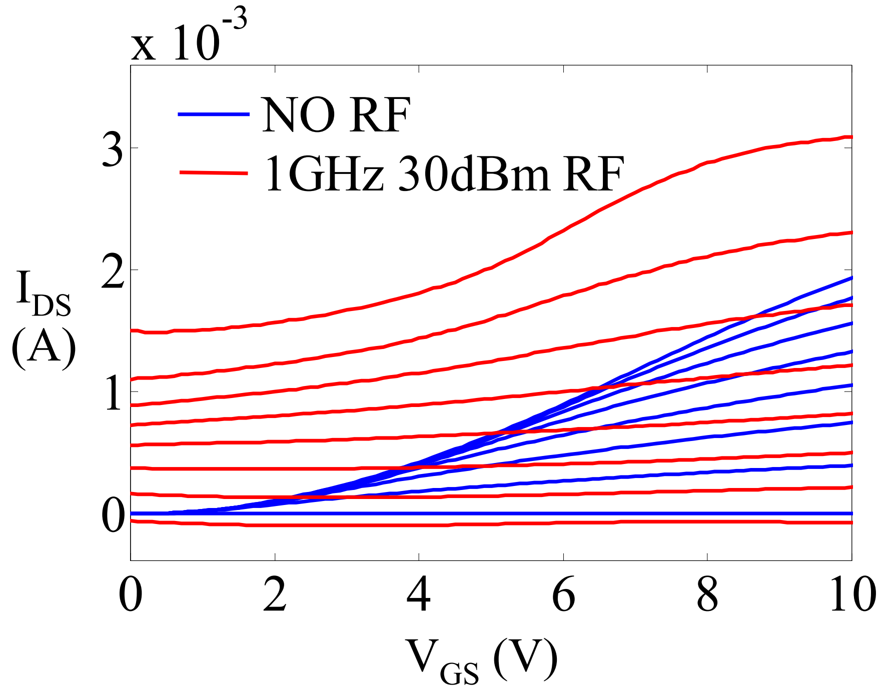
$I_{DS} – V_{GS}$ Output Characteristic
Injection to Gate
1GHz & 5GHz 30dBm

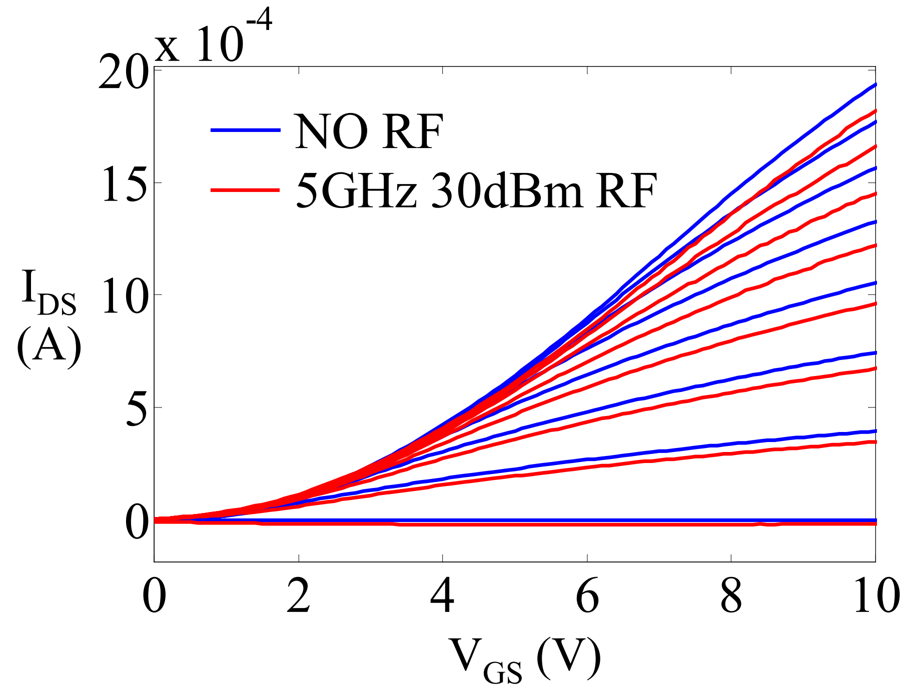




- 1GHz 30dBm injection : significant increase in I_{DS} current and $V_{TH} \rightarrow -\infty$.
- 5GHz 30dBm injection : no significant change.
- Power effect dominant at frequencies lower than 5 GHz

$I_{DS} - V_{GS}$ Output Characteristic
Injection to Drain
1GHz & 5GHz 30dBm

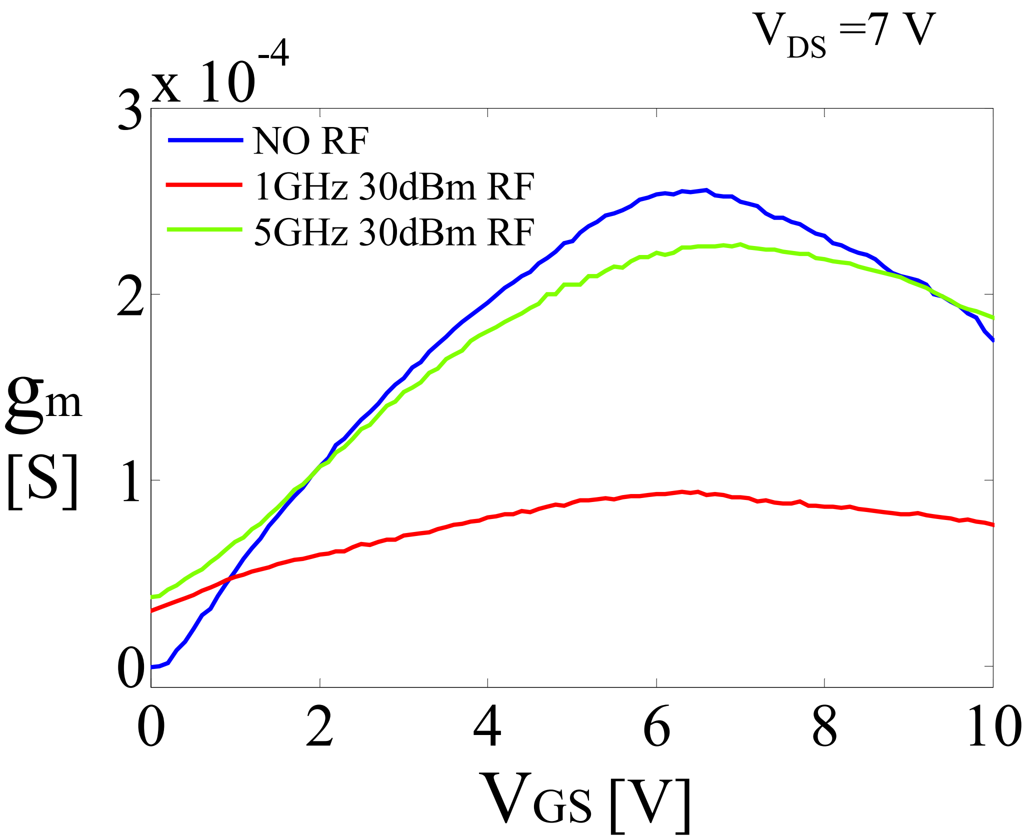




- 1GHz 30dBm RF injection : $V_{TH} \rightarrow -\infty$.
- 5GHz 30dBm RF injection : no significant change.
- Frequency increase suppresses power effect here also.

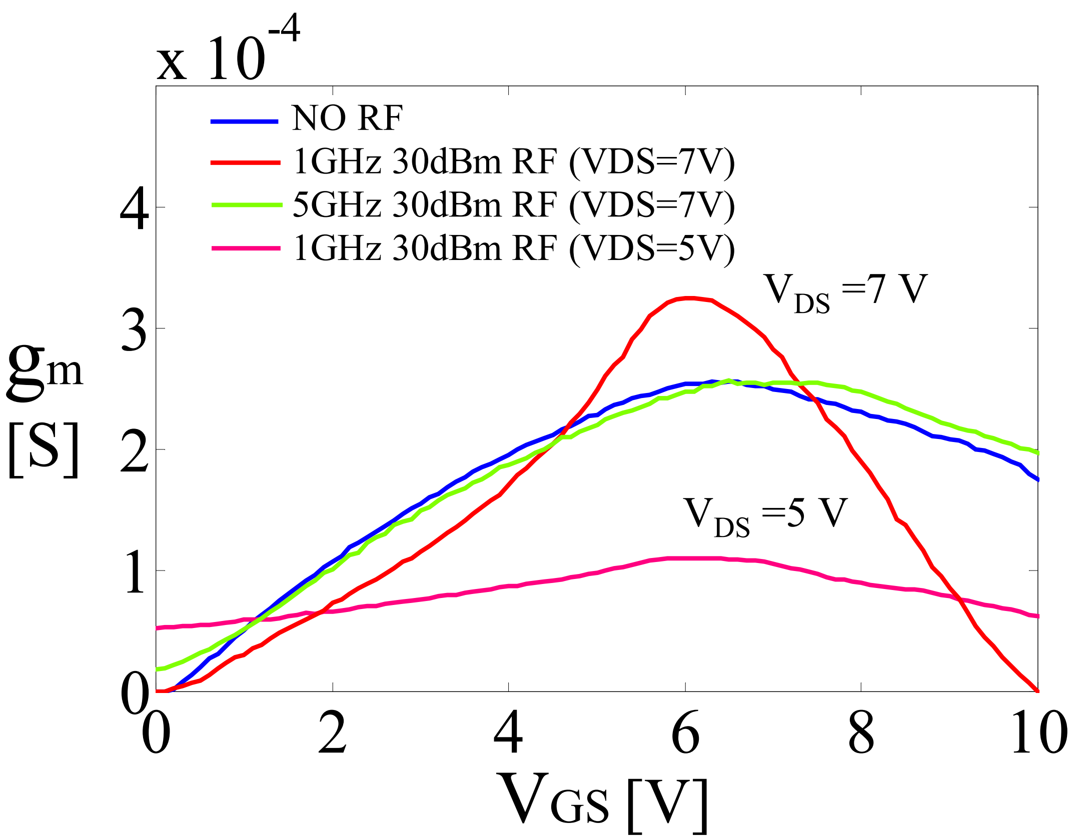
Effect on Transconductance Injection to Gate

- Transconductance gm vs gate bias with and without injection.
- Significant decrease in gm is observed at 1GHz at 30dBm.
- Higher frequency at 5GHz suppresses the effect of power at 30 dBm and produces similar gm value as without RF.

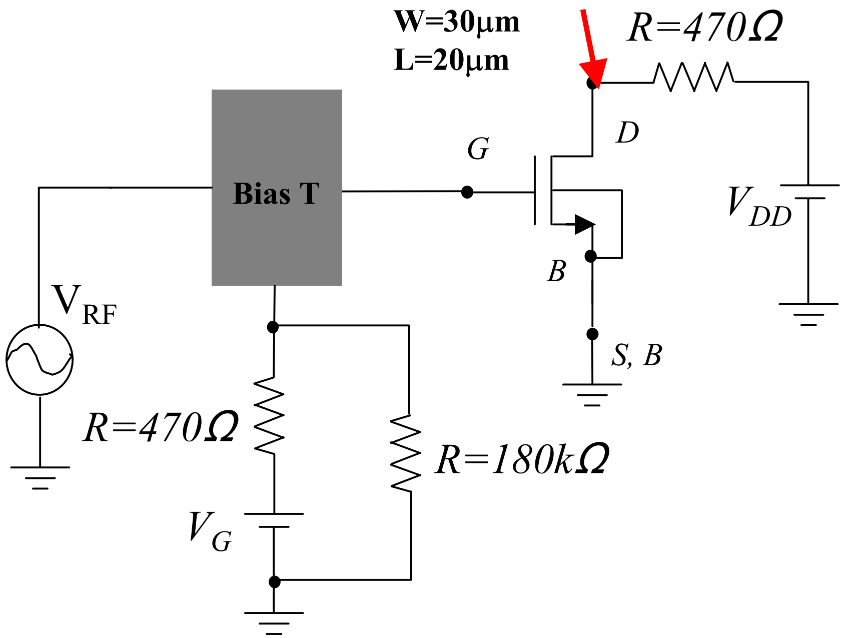


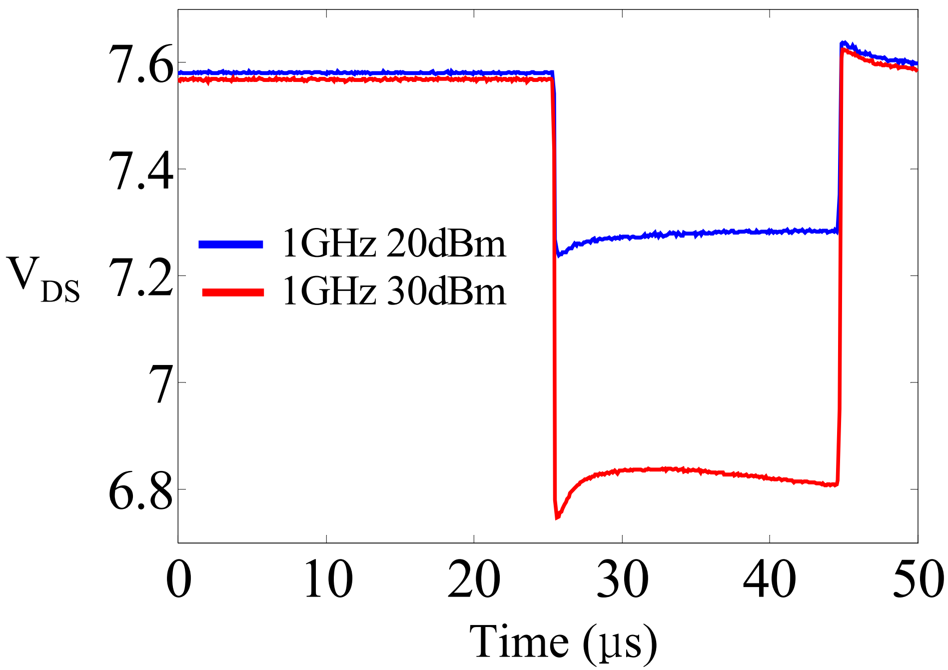
Effect on Transconductance Injection to Drain

- gm vs gate bias for injection at Drain has different behavior.
- An increase is observed for drain bias close to breakdown (7 V) then decrease at lower drain biases at 1GHz at 30dBm.
- Higher frequency (5GHz) suppresses the effect of power at 30 dBm and produces similar gm value as without RF.



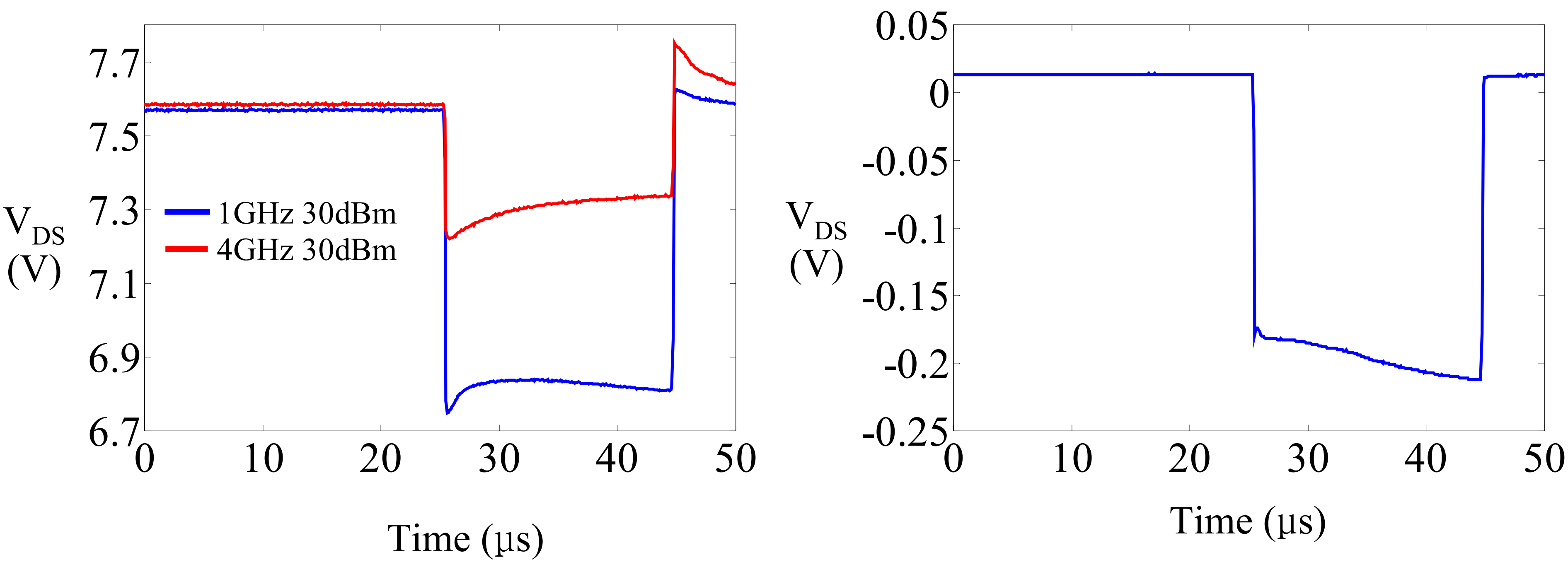
RF Pulse Injection to Gate Power Effect





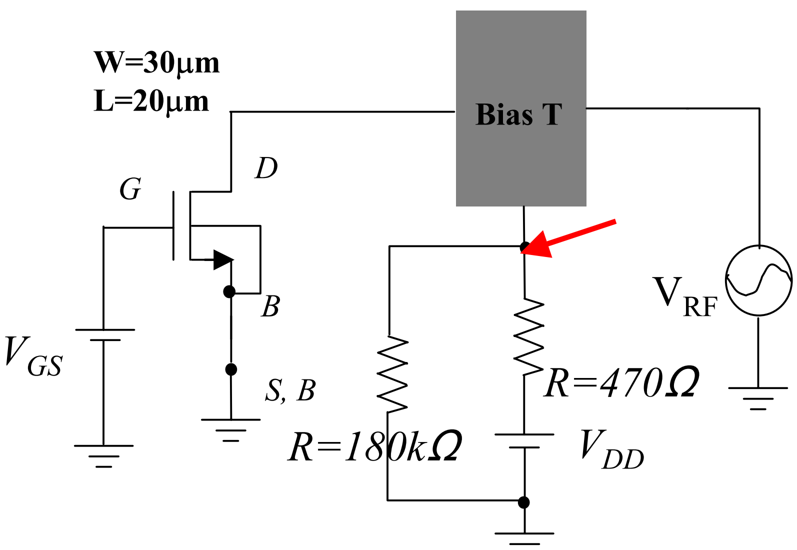
- RF Pulse: 1GHz or 4GHz, 20µs pulse width, 100Hz duty cycle.
- Bias : V_G=6V, V_{DD}=8V, V_{DS}=7.6V, V_{GS}=5.6V (saturation region)
- RF Pulse injection to Gate reduces Drain voltage, hence Drain current I_{DS} increases.
- Increased RF Power results in increased I_{DS}.

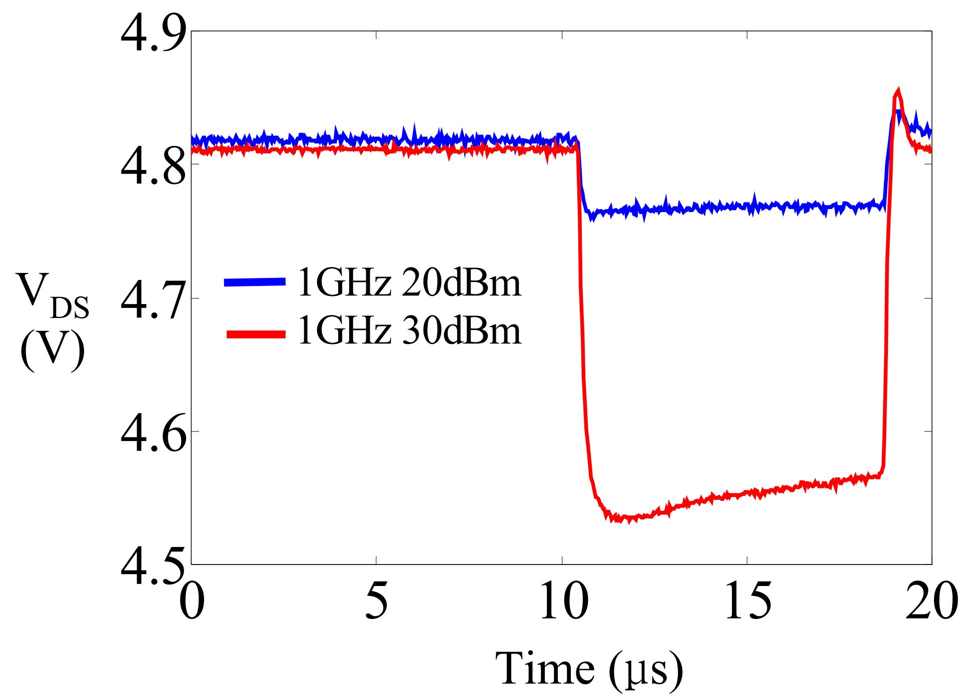
Power Effect Suppression with RF Frequency& Zero Point



- RF frequency increase results in suppressing power effect: 1GHz to 4GHz 30dBm.
- Bias : V_G=6V, V_{DD}=8V, V_{DS}=7.6V, V_{GS}=5.6V (saturation region)
- Zero bias conditions and 1GHz 30dBm RF pulse injection to Gate, Drain voltage is negative causing positive I_{DS} at zero point, as seen in the I-V characteristics.

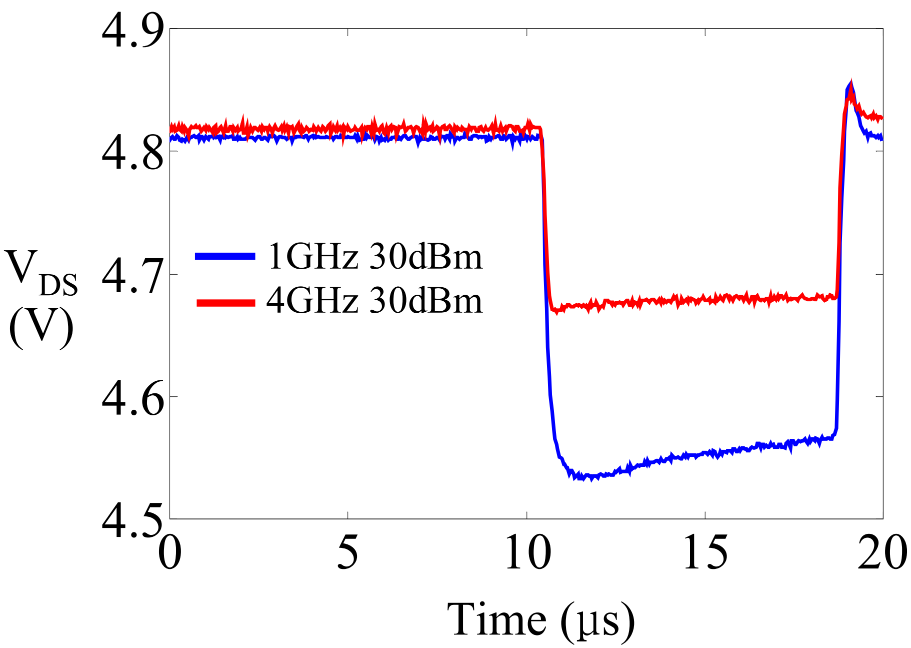
RF Pulse Injection to Drain Power Effect

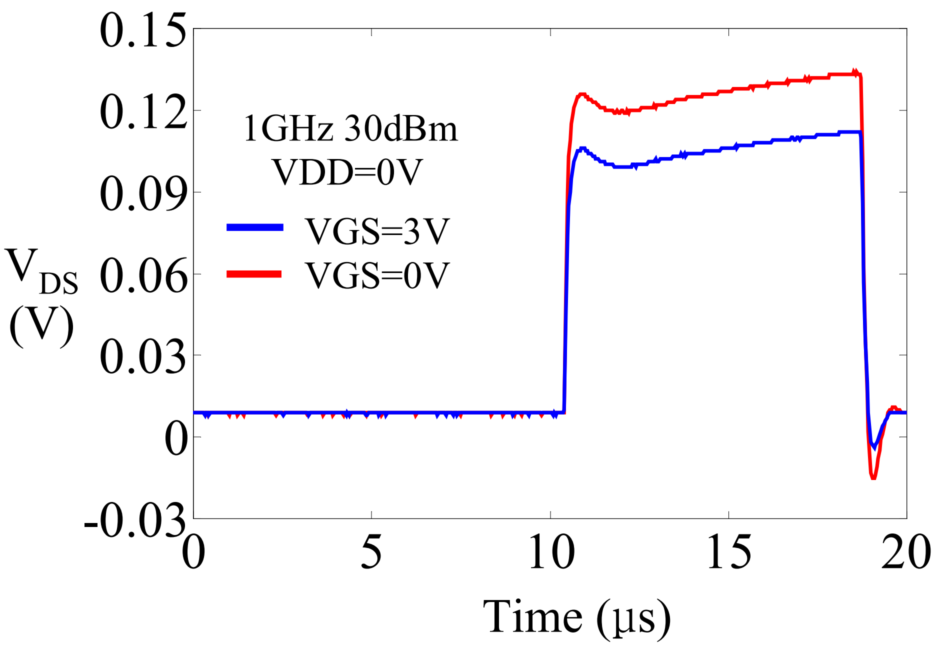




- RF Pulse: 1GHz, 9μs pulse width, 100Hz duty cycle.
- Bias : V_G=3V, V_{DD}=5V, V_{DS}=4.8V, V_{GS}=3V (Saturation region)
- Pulse injection to Drain in Saturation: Drain voltage V_{DS} decreases, hence I_{DS} increases with RF power increasing.

Power Effect Suppression with Frequency Zero Point & Triode Region





- RF Pulse: 1GHz, 9µs pulse width, 100Hz duty cycle.
- RF frequency increase results in suppressing power effect: 1GHz to 4GHz 30dBm.
- At zero bias and 1GHz 30dBm RF pulse injection to Drain, output Drain voltage becomes positive indicating negative I_{DS} (Offset), and in Triode region, I_{DS} becomes less negative.

Discussion of Results for Micron Gate NMOSFETs

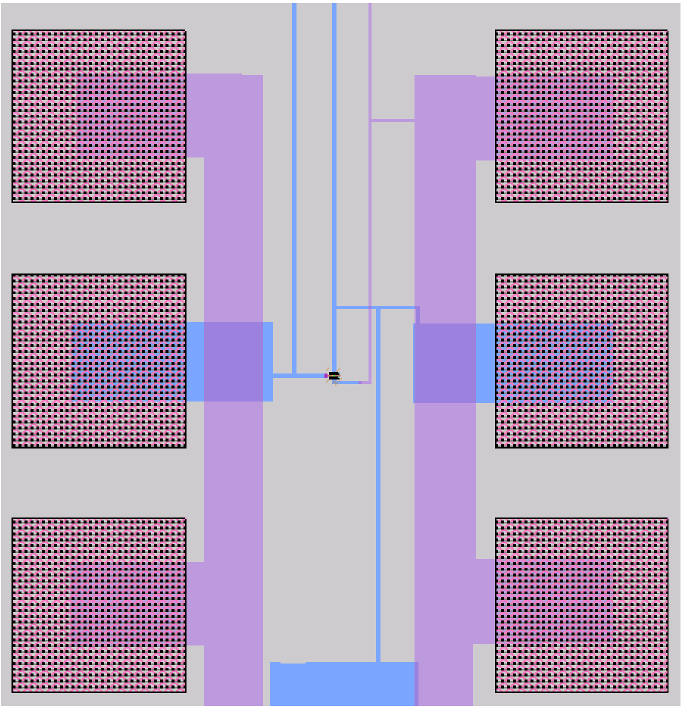
- Injection at the gate had a profound effect on the output I-V characteristics for power levels above 10dBm, and made the devices inoperable at 30dBm (soft errors).
- Device characteristics show a gradual increase in output drain current, loss of saturation, and a positive offset current at zero drain bias, suggesting that the induced RF field at the gate drives the channel into deep inversion to an approximately uniform channel that reaches no pinch-off at the drain.
- The collapse of the characteristic allows no effective gate modulation, and the substantially increased current levels, render the device well outside the set operational limits for the circuit.
- At frequencies > 5 GHz the power effects were found to be strongly suppressed.

Discussion of Results for Micron Gate NMOSFETs

- Continued…
- Injection at the drain resulted in a decrease in drain current (i.e. negative ΔI_{DS}) for power levels up to 15 dBm, and then an increase (positive ΔI_{DS}) at higher power levels.
- I-V lost saturation, and showed a significant reduction in break-down voltage ($< V_{DS} = 8V$). Negative current offset at zero drain bias is evident, indicating the device starts operating at accumulation, before going into inversion at $V_{DS}=0.5V$.
- At higher frequencies the power effect is strongly suppressed.
- The lack of convergence of the characteristics observed in I_{DS} vs V_{GS} plots under RF injection at the gate and drain indicates a fully-on channel with a high concentration of electrons where a threshold voltage cannot be defined.

Submicron NMOS Devices under Direct Injection at Moderate Power "Soft" & "Hard" Errors

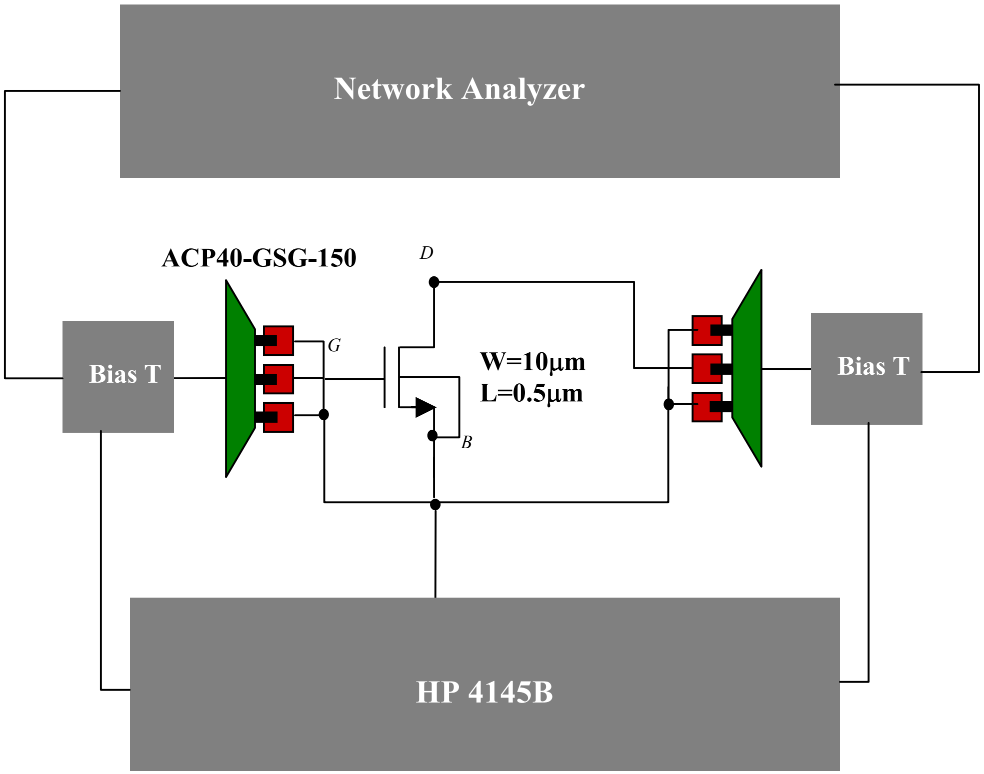
- Examine effects on submicron devices using microwave cascade probes directly on IC chip
- Gate Length varies between 0.5 μm -1.0 μm, W=5-10 μm.
- Operating conditions: V_{GS}=5 V, V_{DS}=7 V
- Cascade probe configuration: 150 μm pitch for s-parameter measurement and RF injection.



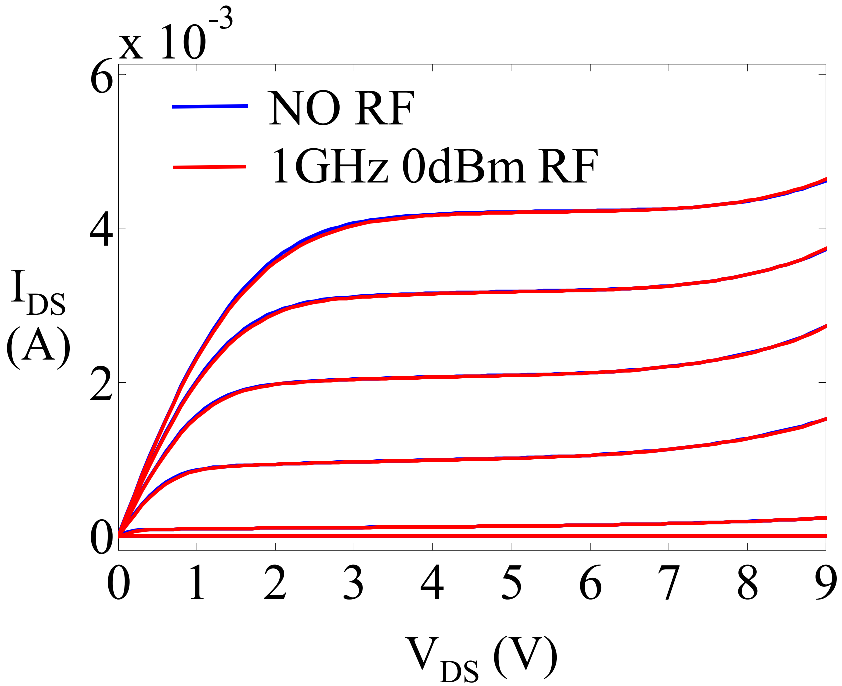
Layout of individual Enhancement-Mode N-channel MOSFET device on IC Chip

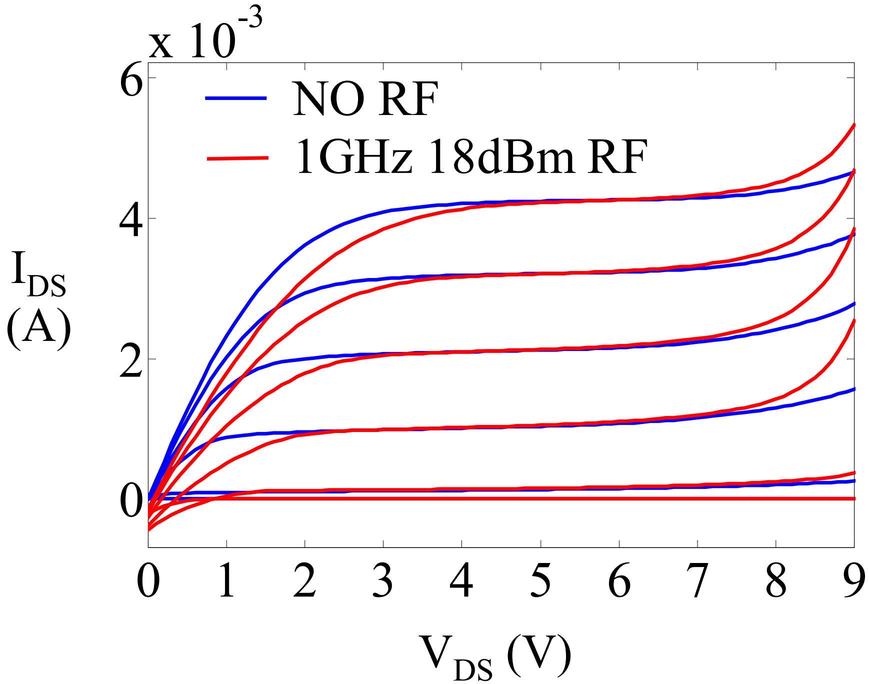
Direct Wafer Measurement Set-Up for Submicron MOSFETs and Inverter Gates

- RF direct injection up to 20dBm at 1-20GHz
- Cascade Probe on-wafer measurement.



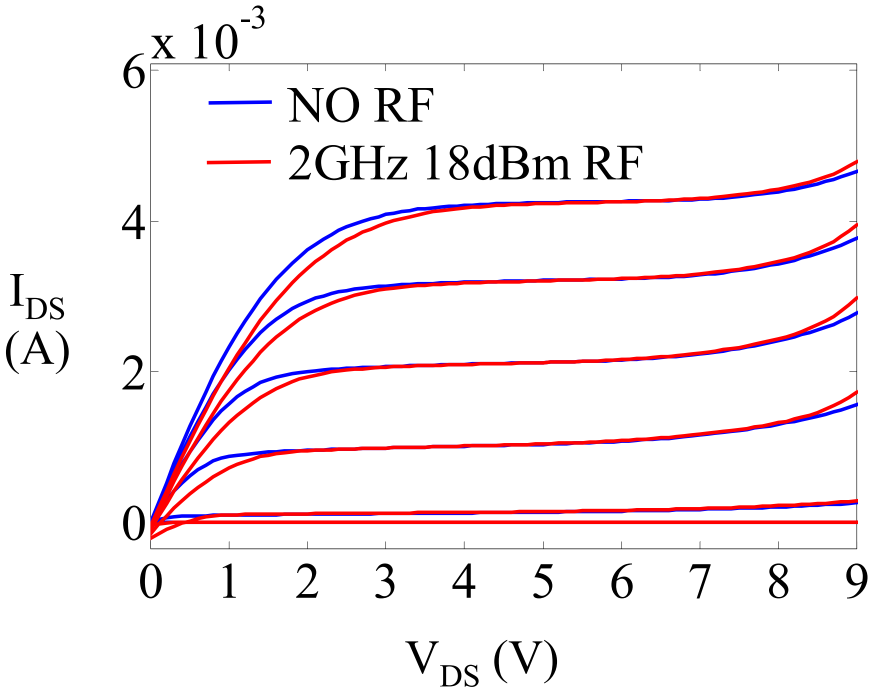
$I_{DS} - V_{DS}$ Output Characteristic Injection to Drain 1GHz 0dBm & 18dBm

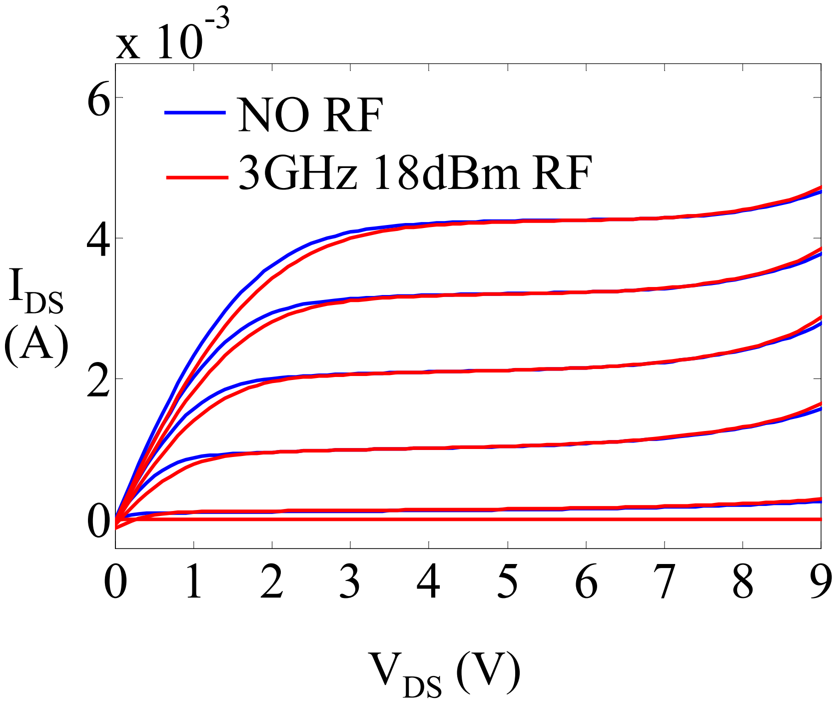




NMOSFET W/L=10µm/0.5µm

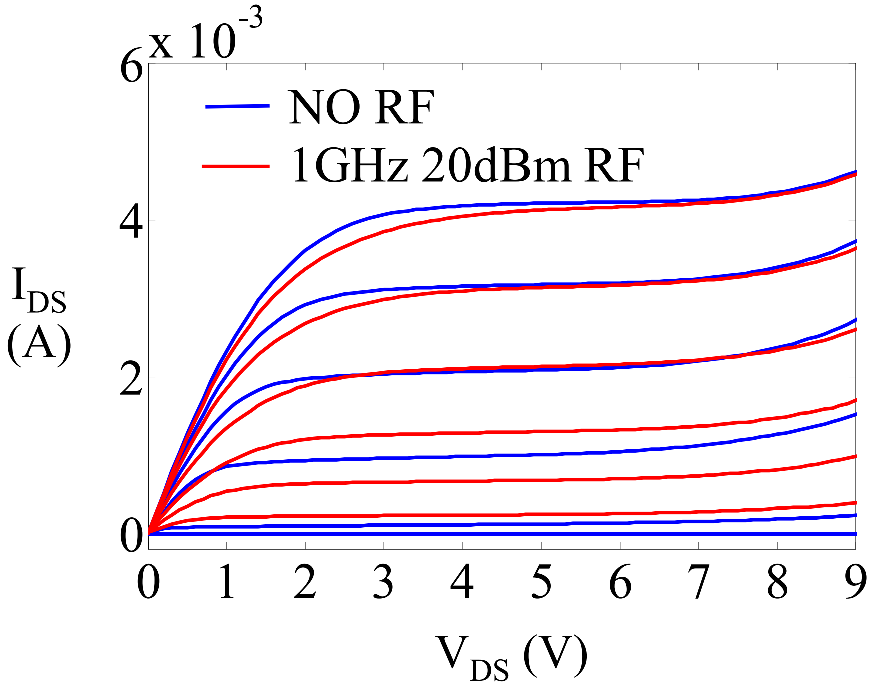
I_{DS} – V_{DS} Output Characteristic Injection to Drain 2 & 3 GHz at 18dBm

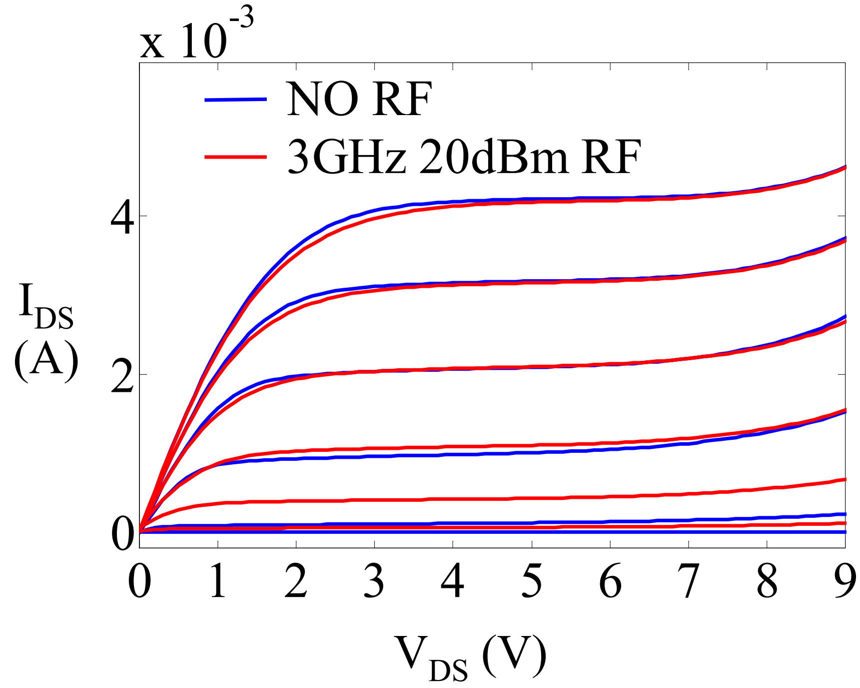




NMOSFET W/L=10µm/0.5µm

$I_{DS} - V_{DS}$ Output Characteristic Injection to Gate 1 & 3GHz at 20dBm

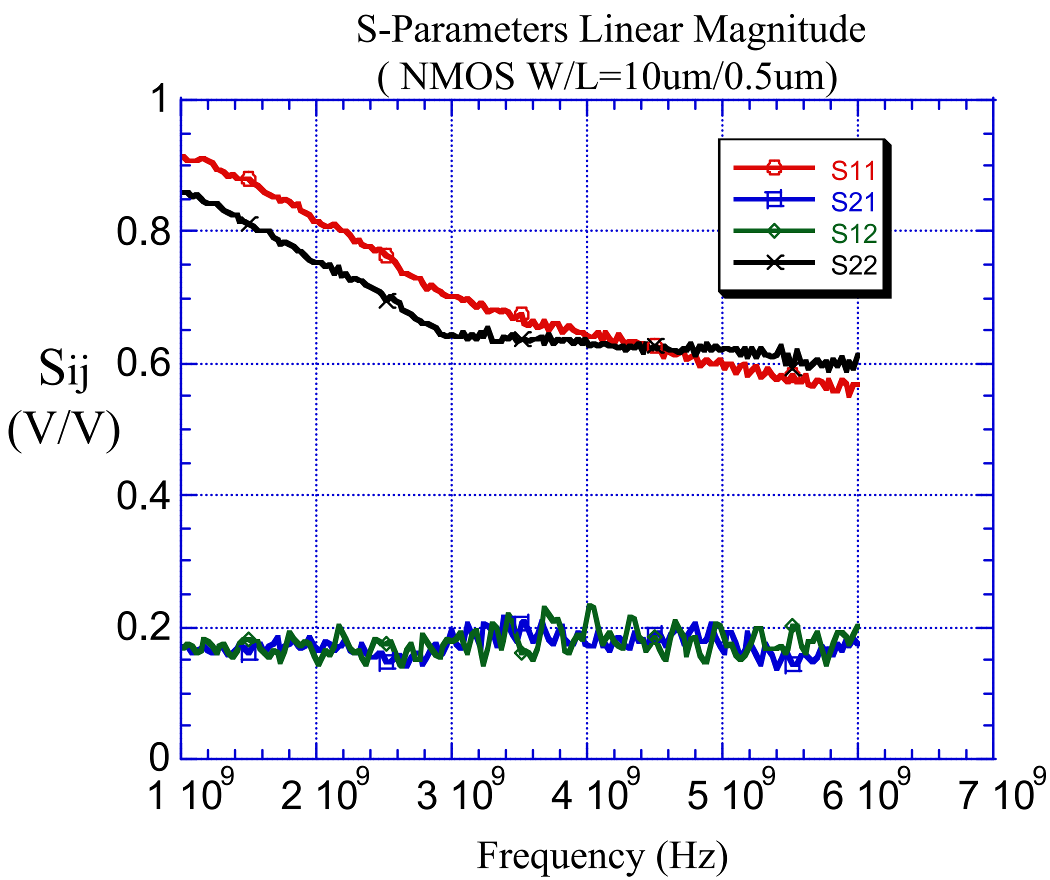




Power suppression effect with increasing frequency

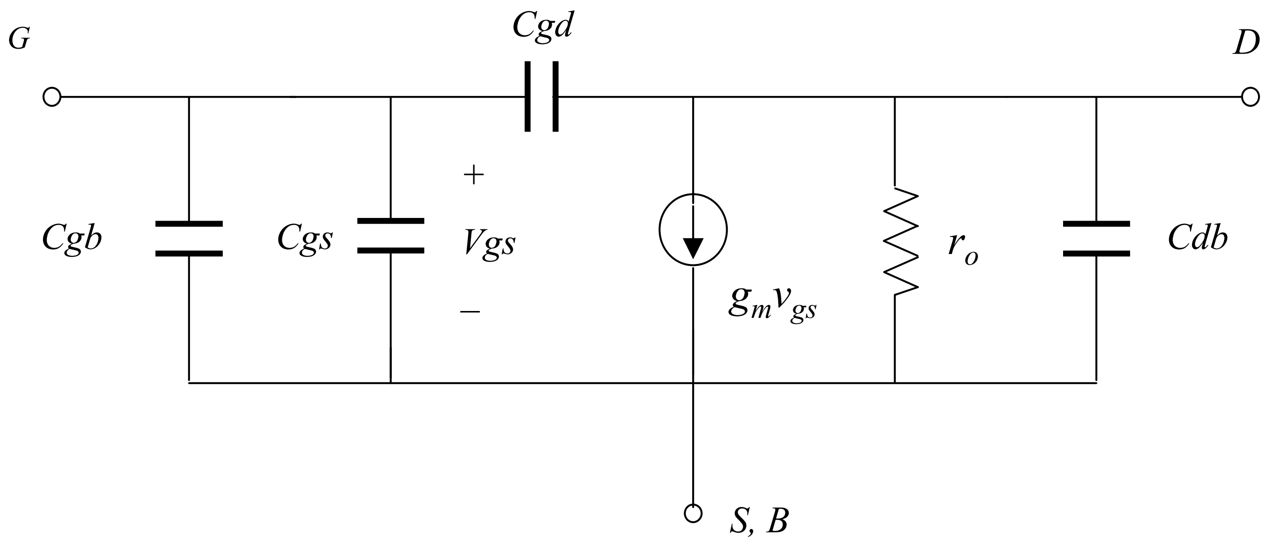
NMOSFET W/L=10µm/0.5µm

S-Parameter Measurements



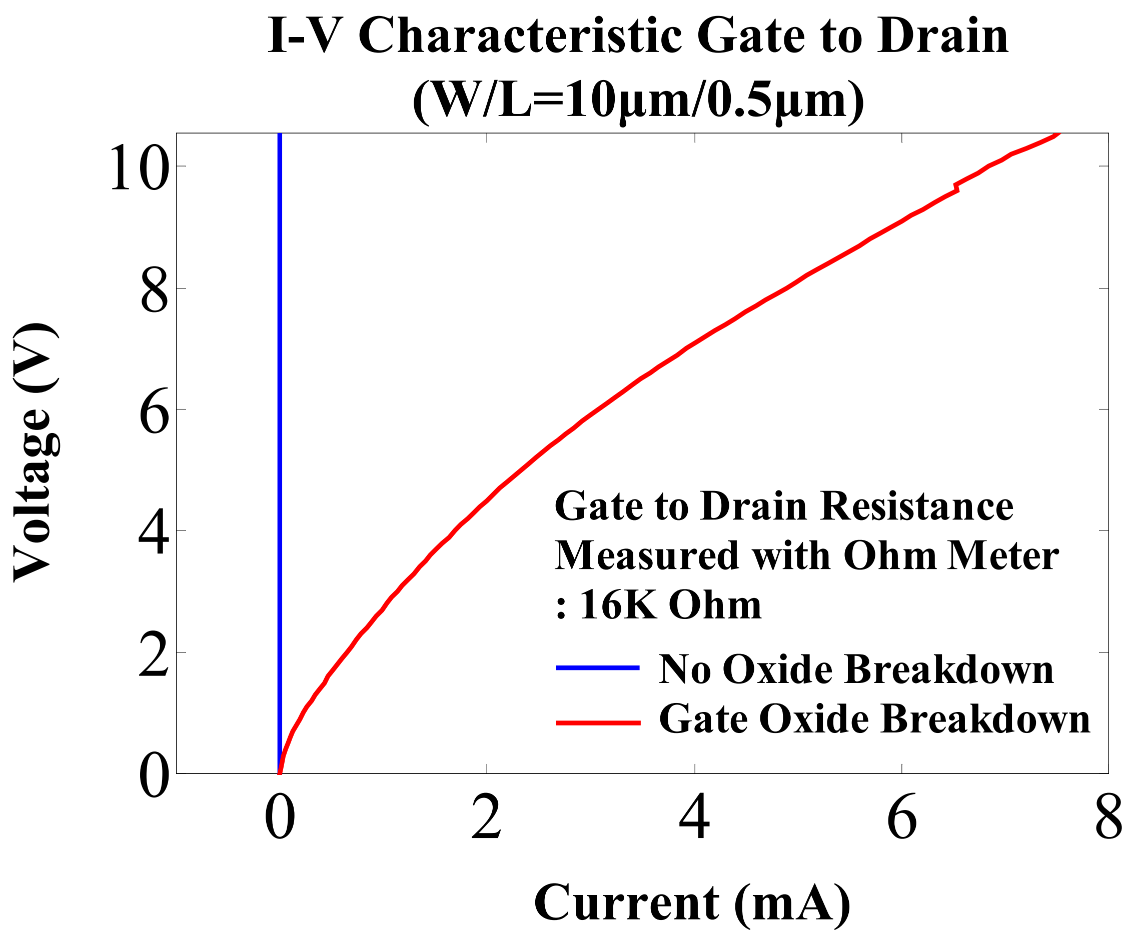
- S-parameter measurement from 3MHz to 6GHz.
- NMOSFET W/L=10μm/0.5μm
- S11 and S22 indicate the reflection of power at port 1 and 2 is decreasing with frequency increasing while little power is transmitted through the device (S12, S21)
- This indicates that at higher frequencies power dissipates in the device!?

Power Dissipation at Higher Frequencies: Capacitive Coupling to Ground through Intrinsic Capacitors



	Off	*Triode*	*Saturation*	f_T
Cgs	*2.33 fF*	*6.079 fF*	*8.106 fF*	*9.57GHz*
Cgb	*7.984 fF*	*0.5 fF*	*0.5 fF*	
Cgd	*2.33 fF*	*6.079 fF*	*2.33 fF*	
Cdb	*6.463 fF*	*6.463 fF*	*6.463 fF*	

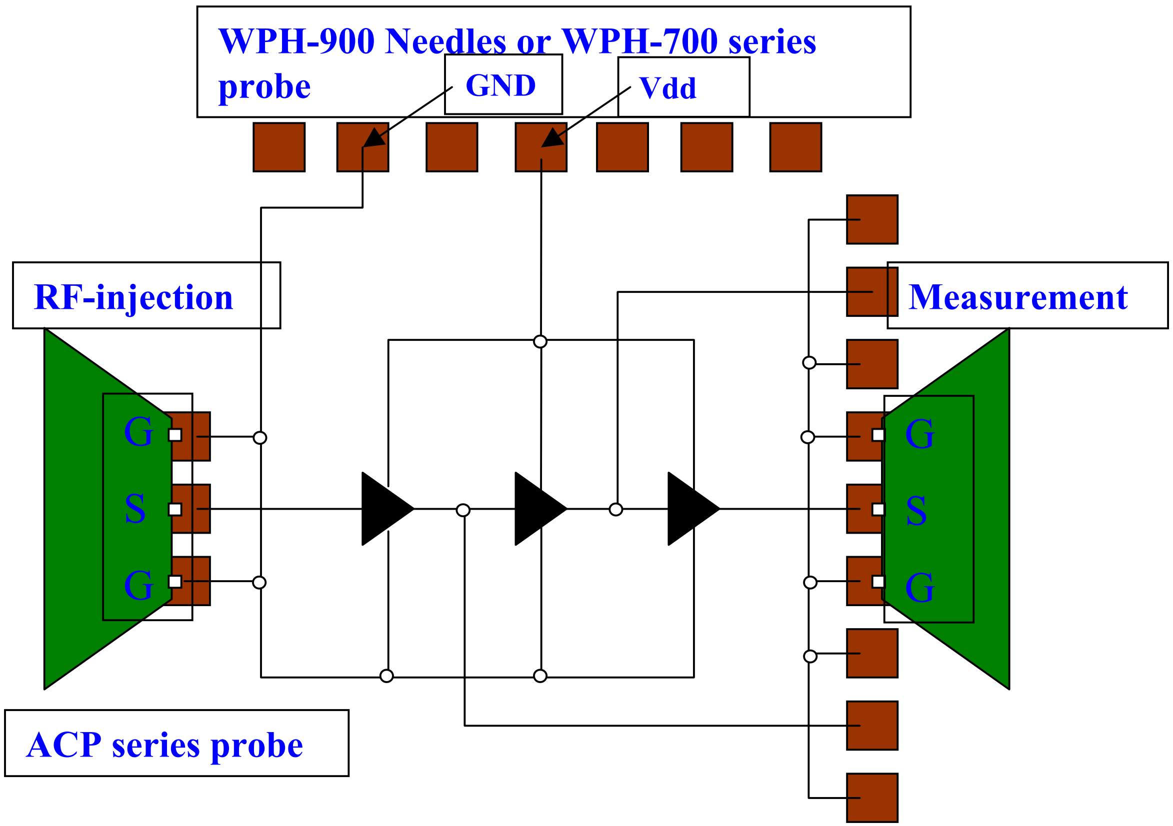
Catastrophic Failure (Hard Error) under CW Microwave Injection to Drain

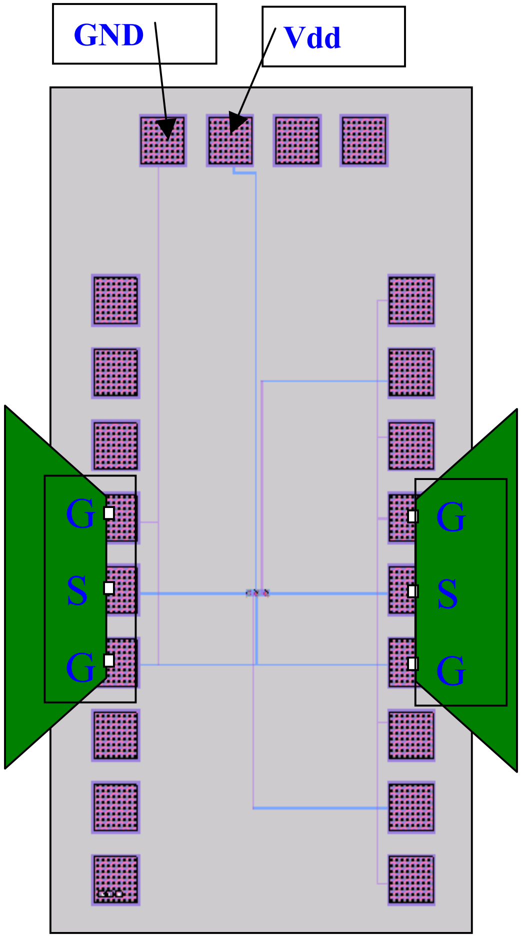


Discussion of Results for Sub-micron NMOSFETs

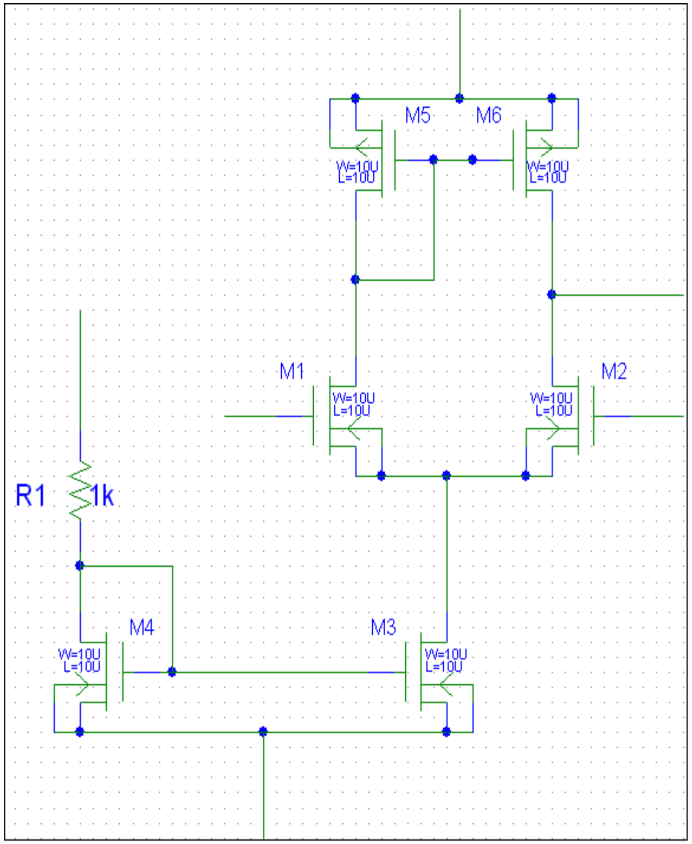
- 0.5µm gate N-MOS devices have been measured under microwave injection and I-V characteristics and s parameters were measured.
- Results show similar effects as those observed previously but to a lesser extend due to lower power and levels of transmission.
- Increased frequencies suppressed power effect also.
- Device catastrophic failure (hard error) observed for injection to Drain (more prone to failure than injection to gate due to reduced break-down voltage) >18dBm.
- The low level of power transmission through the devices is probably due to the by-pass effects of gate and drain capacitances at higher frequencies as the s-parameter and equivalent circuit model investigation showed.

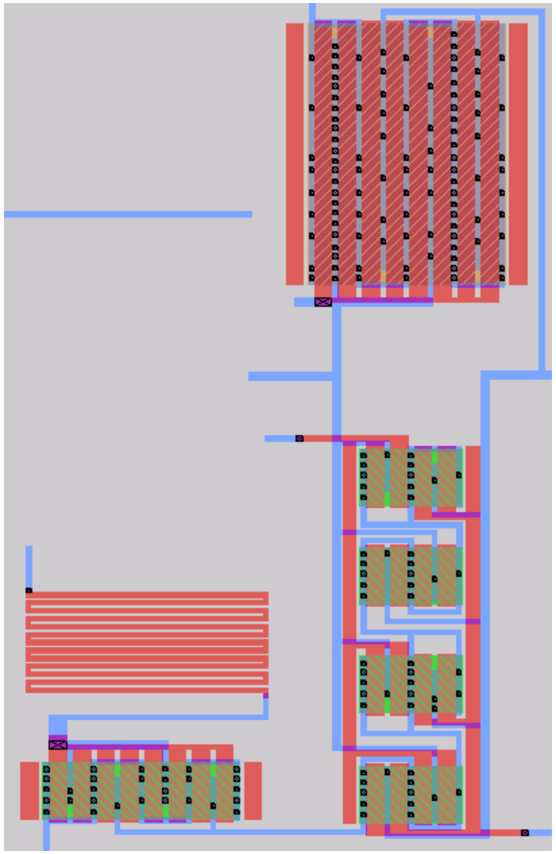
Individual and Clustered Inverter Gates Design & RF Probe Measurement Pattern

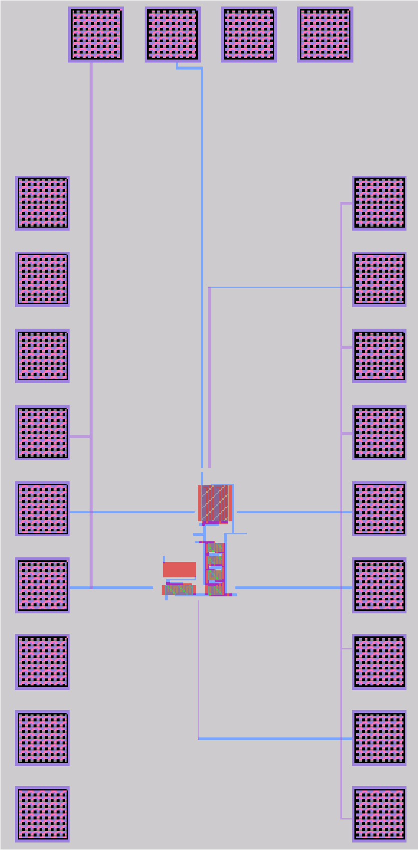




Differential Amp Design & Measurement Pattern







Conclusions

- Injected microwave power significantly affects output currents, g_m, g_O, and breakdown voltages (V_{BD}) for power levels above 10 dBm between 1 and 20 GHz.
- Effects result in loss of switching-off capability, loss of saturation, linearity, development of DC offset currents at zero drain bias, and substantial reduction in V_{BD}.
- The power effects were observed to be suppressed above 5 GHz, and s-parameter measurements indicated a by-pass path to ground through the intrinsic gate and drain capacitances for the injected power.
- Catastrophic (hard error) failure was observed in the sub-micron devices through gate oxide failure at levels >18dBm

Recent Publications/Presentations/Patents:

1. **6th Annual Directed Energy Symposium (DEPS), Albuquerque, NM, October 2003**
2. **International Semiconductor Device Research Symposium (ISDRS'03), Washington DC**
3. **IEEE-EDS Distinguished Lecture, NJ Inst. of Technology (NJIT), Newark, NJ, Nov. 2003**
4. **"High Power Microwave Effects on the operational parameters on MOSFET devices in IC's" Solid State Electronics, in preparation.**
5. **"Microwave interference on-chip sense and protect circuit", US Patent 2002, Pending.**

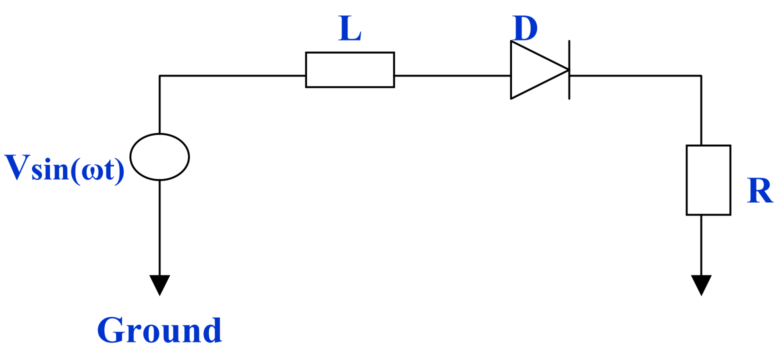
Continuing and Future Work

- Clusters of gates and differential amps are currently being measured to identify coupled effects.
- RF Pulse injection will determine the effects with pulse characteristics and isolate the impact due to avalanche and/or thermal effects.
- Examine vulnerabilities due to the intrinsic capacitive elements of the devices and model capacitances for large signal operation.
- Apply to the study of the inverter gates and inverter gate clusters for coupled effects and differential amplifiers.
- Design and fabricate small area individual p-n junction IC diodes with inductor-resistor elements to examine experimentally “chaos” effects.
- Model effects into MOSFET/Gate parameters for vulnerability prediction.
- Use MOSFET devices as on-chip sensing and protecting elements (Patent).
- Develop nanocomposite coatings for IC on-chip protection. The first polymer based nanocomposite coatings have been produced.

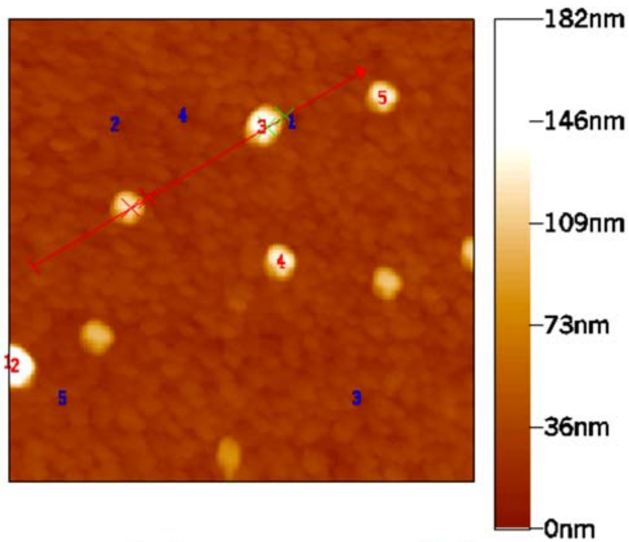
Future Experiments:

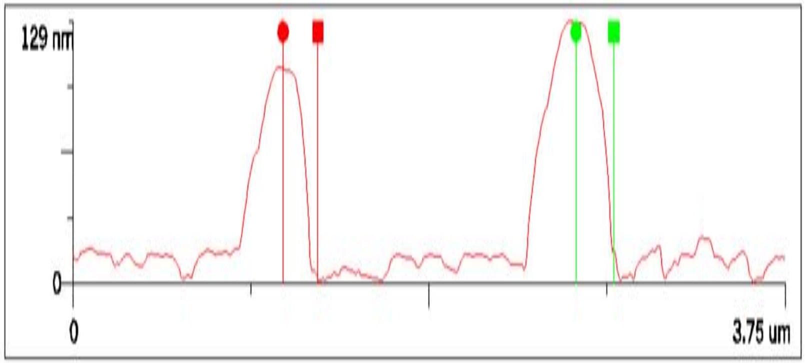
•Small p-n Junction Diode for Chaos

- Design and fabricate small area individual p-n junction IC diodes and test with inductor-resistor circuit.
- Apply sinusoidal input and measure current I without perturbing circuit.

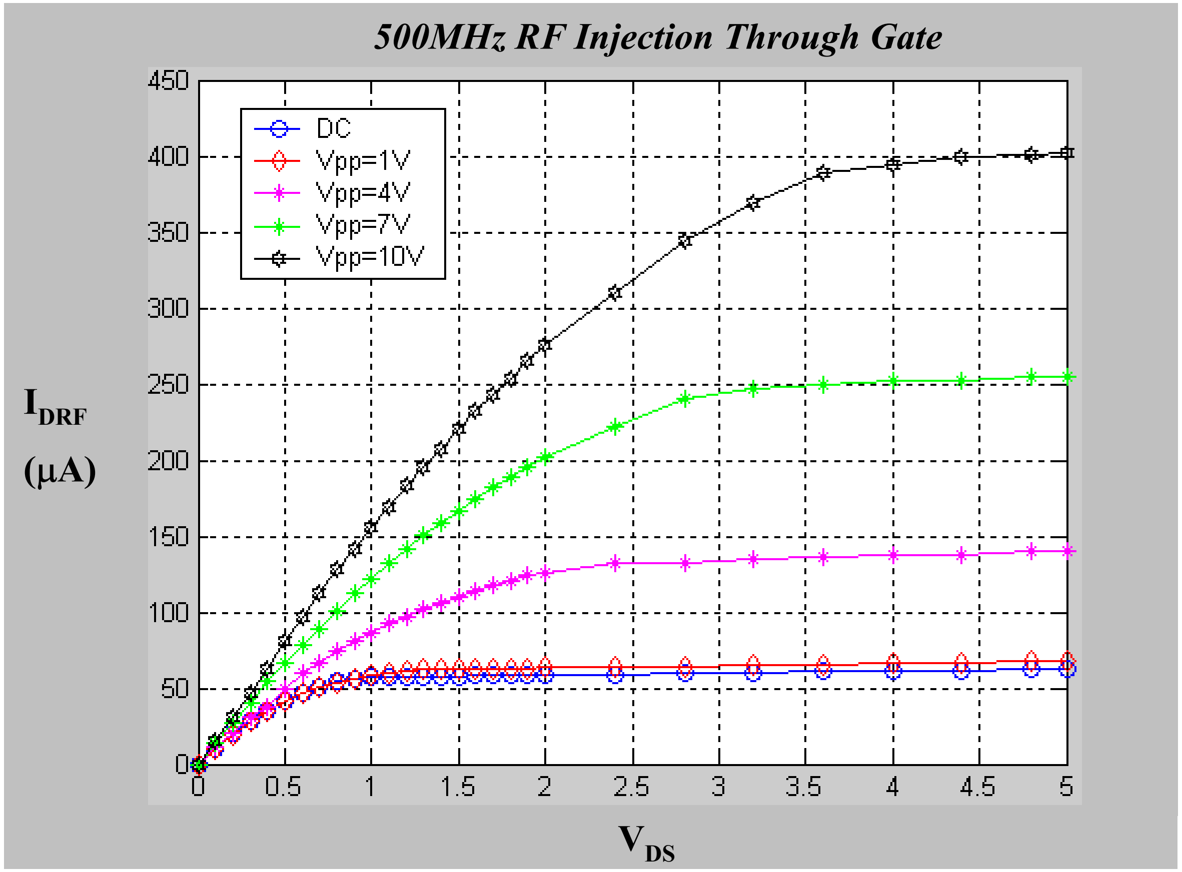


•Nanocomposite Coatings for IC Protection





Calculated RF Injection to Gate



$I_{DRF} = I_D + \Delta I_{DRF}$

Where :

I_D : DC biased current

ΔI_{DRF} : increase of drain current due to RF injection

Family of I-V characteristics at DC and 500 MHz for RF p-p voltages ranging from 1 to 10 V. The DC gate bias per characteristic is at V_{GS}=2 V.

Equations for RF Injection Analysis

(1) $$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) = g(V_G)$$

(2) $$\Delta V_G = V_o \sin \omega t$$

(3) $$V_G = V_{Go} + V_o \sin \omega t$$

(4) $$I_D + \Delta I_{DRF} = \frac{\mu_n C_{ox} W}{2L}(V_G - V_S - V_T)^2(1 + \lambda V_{DS})$$

(5) $$I_D + \Delta I_{DRF} = I_D + \left(\frac{\partial g}{\partial V_G}\right)_{V_{GO}} \Delta V_G + \frac{1}{2}\left(\frac{\partial^2 g}{\partial V_G^2}\right)_{V_{GO}} \Delta V_G^2 + \ldots$$

(6) $$\Delta I_{DRF} = \left(\frac{\partial g}{\partial V_G}\right)_{V_{GO}} (V_o \sin \omega t) + \frac{1}{2}\left(\frac{\partial^2 g}{\partial V_G^2}\right)_{V_{GO}} (V_o^2 \sin^2 \omega t) + \ldots$$

(7) $$\langle \Delta I_{DRF} \rangle = \frac{1}{2}\left(\frac{\partial^2 g}{\partial V_G^2}\right)_{V_{GO}} \left(\frac{V_o^2}{2}\right)$$

(8) $$\left(\frac{\partial^2 g}{\partial V_G^2}\right)_{V_{GO}} = \frac{\mu_n C_{ox} W}{2L}(1 + \lambda V_{DS})$$

Injected Power Conversion

$$P_{in} = \frac{V^2}{R} \quad V = \sqrt{2P_{in}R} \quad (\times 2 \quad worst\ case)$$

$$P_{dBm} = 10\log_{10}\frac{P_{in}}{1mW} \quad P_{in} = 1\times 10^{-3}\times 10^{P_{dBm}/10}$$

	0dBm	5dBm	10dBm	15dBm	20dBm	25dBm	30dBm
Pin	1mW	3.2mW	10mW	31.6mW	100mW	316.2mW	1W
V	0.3162	0.5657	1	1.76	3.1623	5.6232	10
$V_{worst\ case}$ (x2)							