EM Effects on Semiconductor Devices, Gates and Integrated Circuit Interconnects

Dept. of Electrical and Computer Engineering, UMCP

Neil Goldsman

Collaborators:

Omar Ramahi, John Rogers, Bruce Jacob, Agis Iliadis

Xi Shao, Parvez N. Guzdar

Akin Akturk, Zeynep Dilli, Bo Yang, Todd Firestone

EM Effects on Semiconductor Devices, Gates and Integrated Circuit Interconnects

Goal: Through modeling and experiment characterize microwave coupling on integrated circuits and its effect on device and circuit performance

Method: Develop modeling tools to analyze and predict effects on devices, fundamental circuit blocks, and interconnects.
-Base modeling tools on Semiconductor Equations and Schrodinger Equation and Maxwell's Equations

Verify with experiments: Chips fabricated through MOSIS

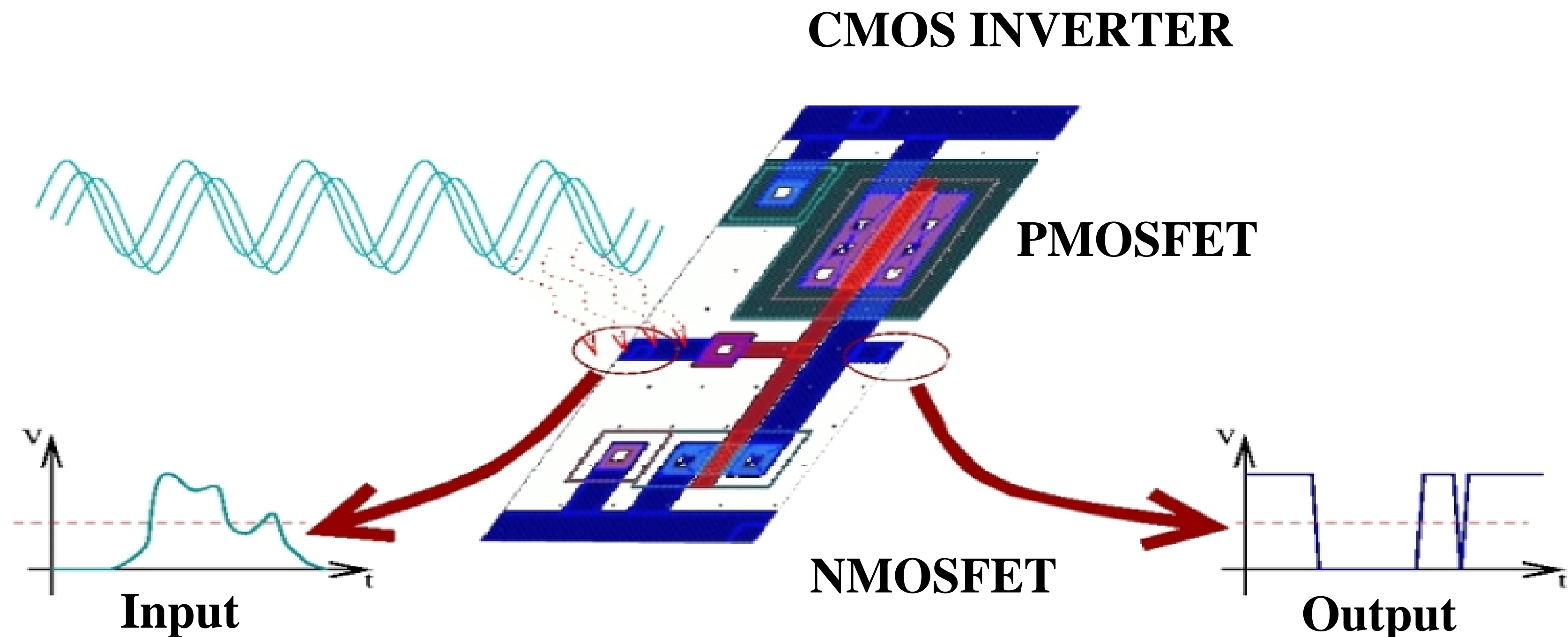
Outline

EM Coupling: Levels Investigated

Task 1: Device and Gate Level Modeling

Task 2: EM Modeling of On-Chip Transmission Lines

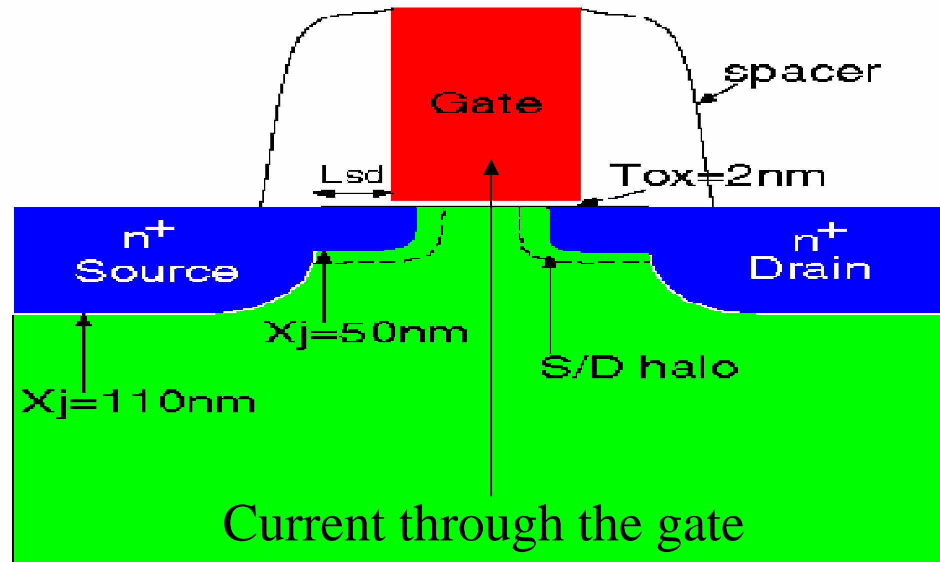
Task 3: On Chip Passive Elements (Inductors)



Task 1: EM Coupling to Semiconductor Devices

- EM coupling may induce large voltages on semiconductor device terminals inside IC's
- Large terminal voltages can damage devices permanently and cause upsets.
- Most modern ICs are composed of MOSFETs.
- Pentium IV contains 40 million nanoscale MOSFETs.
- MOSFETs are exceptionally vulnerable.
- Task 1 focuses on detailed modeling of MOSFETs to understand their internal mechanisms of EM induced failure.

MOSFET Cross-Section and Illustration of Vulnerabilities: Oxide and Avalanche Breakdown

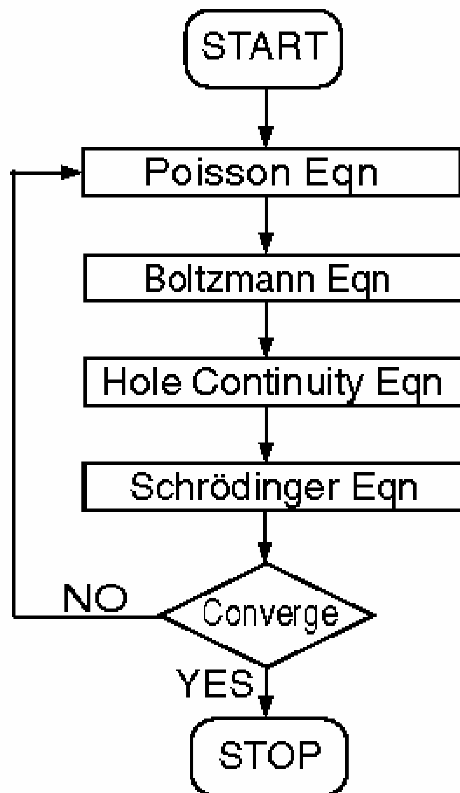


Problems:

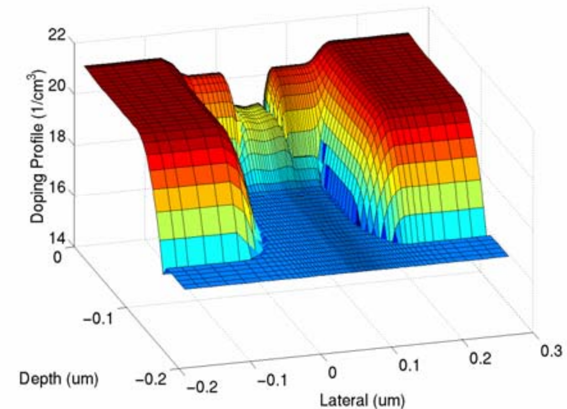
-Scaling to the nanometer gate length requires oxides less than 20Angstroms.
-Such thin oxides give rise to such large gate current that devices will not function.
-Large internal fields cause impact ionization, avalanching and damaging filaments
-Problems especially important for EM coupling, which induces large voltages to Gate and Drain Electrodes!

Developed Quantum Device Simulator to Investigate Internal MOSFET Subject to Large Coupled EM Terminal Voltages:

Solve QM Device Equations Numerically. Inputs are device structure, doping profile & basic physics.



Device Doping Profile



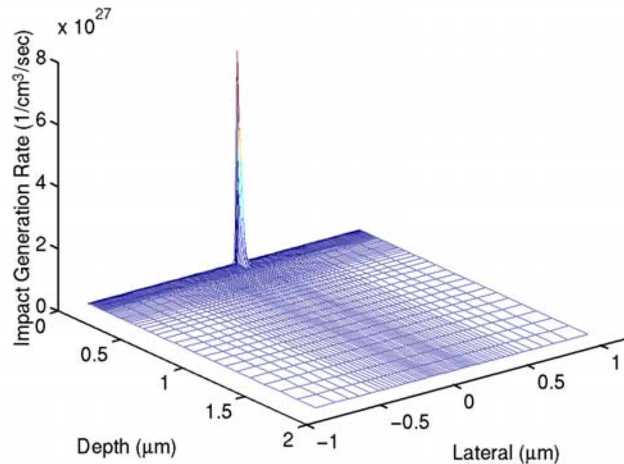
Electron Transport Physics Include:

-Acoustic & Optical Phonons
-Band Structure
-Ionized Impurities
-Impact Ionization & Breakdown
-Gate Current and Oxide Breakdown

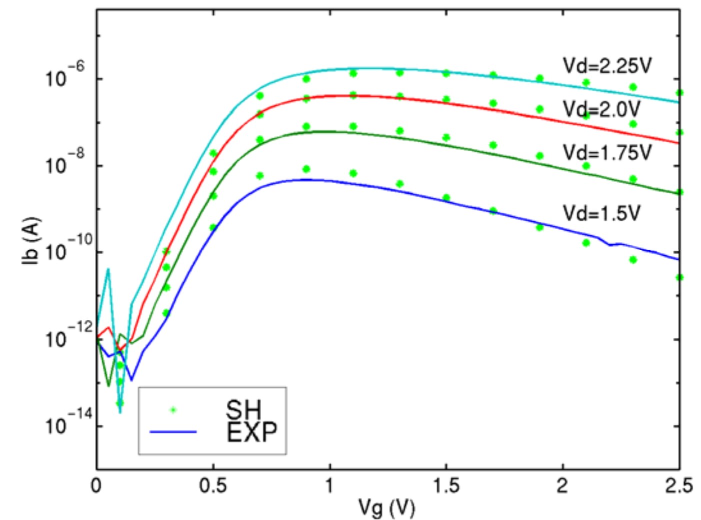
Device Modeling Probes Inside Device Where Experiments Can Not Reach

Pinpoints Internal Fields, Currents and Problem Spots:

Internal MOSFET Avalanche Rate



Resulting Parasitic Substrate Current



Using the new simulator to model EM induced avalanche breakdown

-Result indicate 2V on drain of 0.1μm causes excessive electron-hole pair generation peak in channel.

-Simulations agree with experiment on resulting substrate current

-Excessive substrate current causes permanent filament damage

Gate Current: Mathematical Model

The final gate leakage current will be the summation of the tunneling and thermionic current

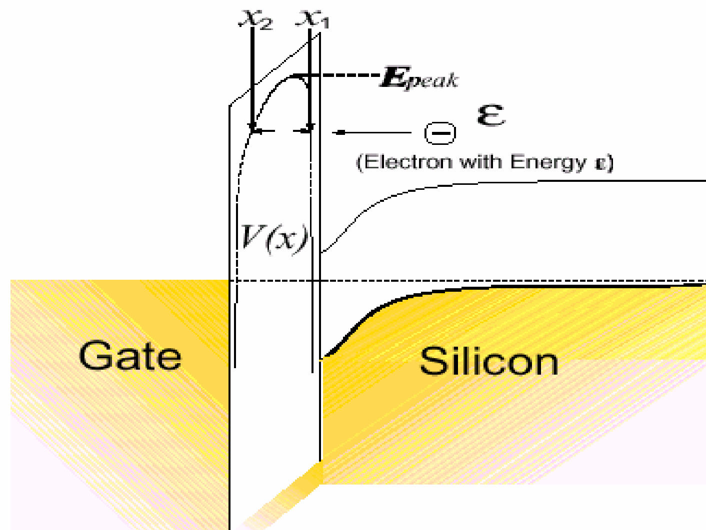
$$J_{gate}(x) = J_{tu}(x) + J_{th}(x)$$

Where tunneling current

$$J_{tu}(x) = \int_0^{E_{peak}} f(\xi, x) g(\xi) v_\perp(\xi) T_{tun}(\xi, x) d\xi$$

And thermionic current

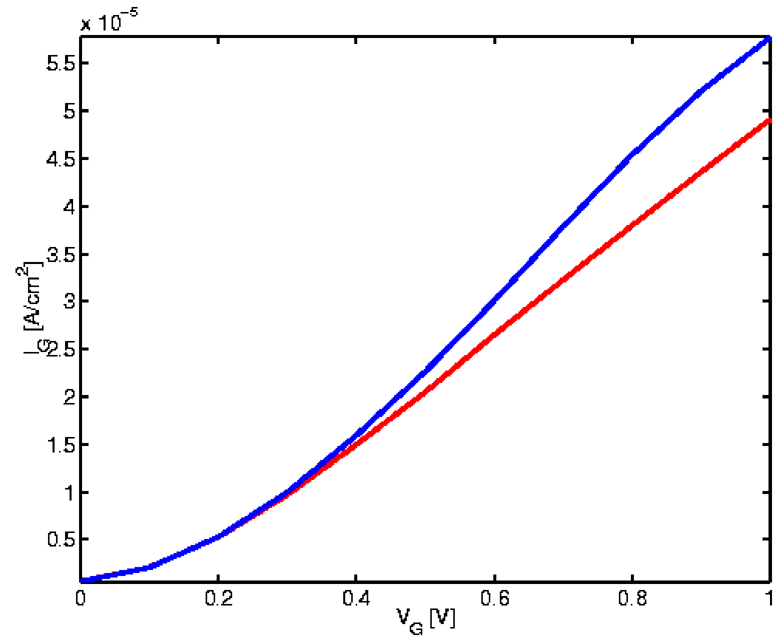
$$J_{ther}(x) = \int_{E_{peak}}^{\infty} f(\xi, x) g(\xi) v_\perp(\xi) T_{ther}(\xi, x) d\xi$$

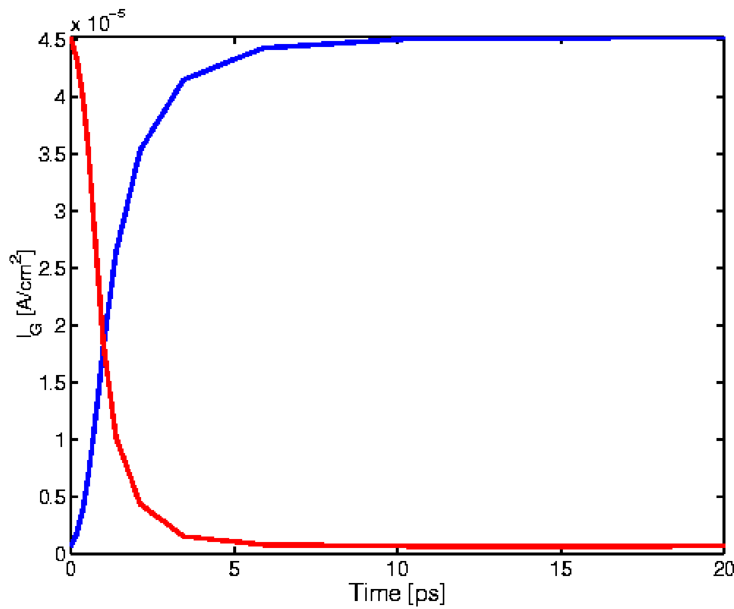


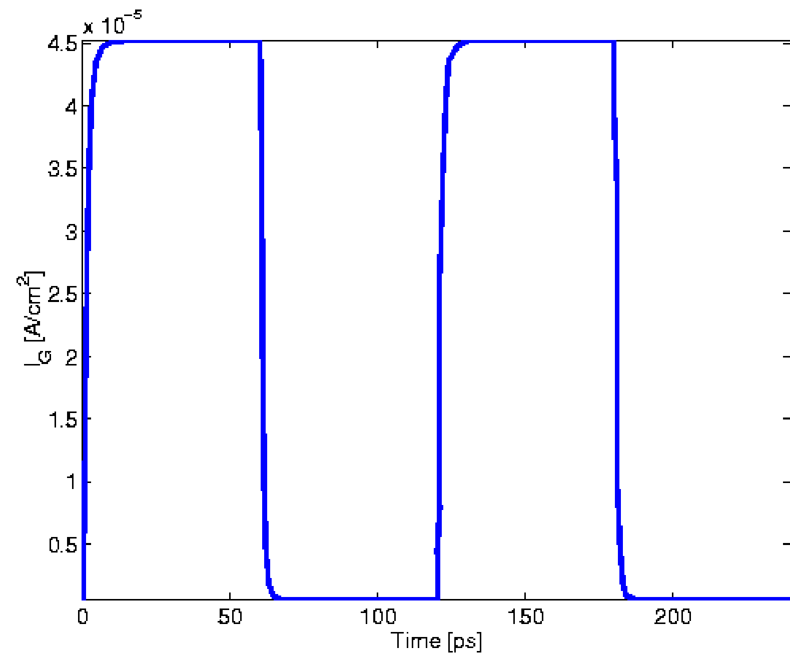
J_{gate} = *Gate Current Density*
f = *Distribution Function*
g = *Density of States*
T_{tu} = *Tunneling Probability*
T_{ther} = *Thermionic Probability*

Gate Tunneling Current
Ig vs. Time
DC and Transient

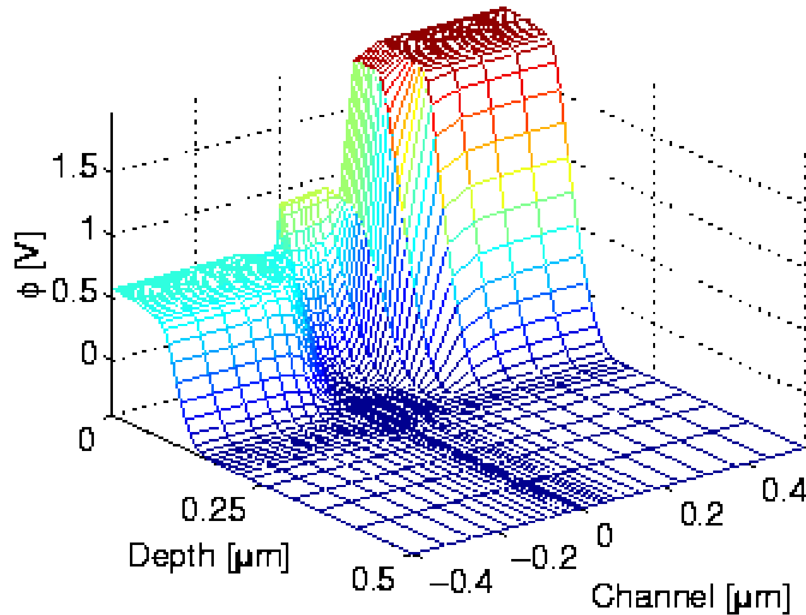
Transient does not increase gate current density, and thus probably does not increase probability of breakdown.

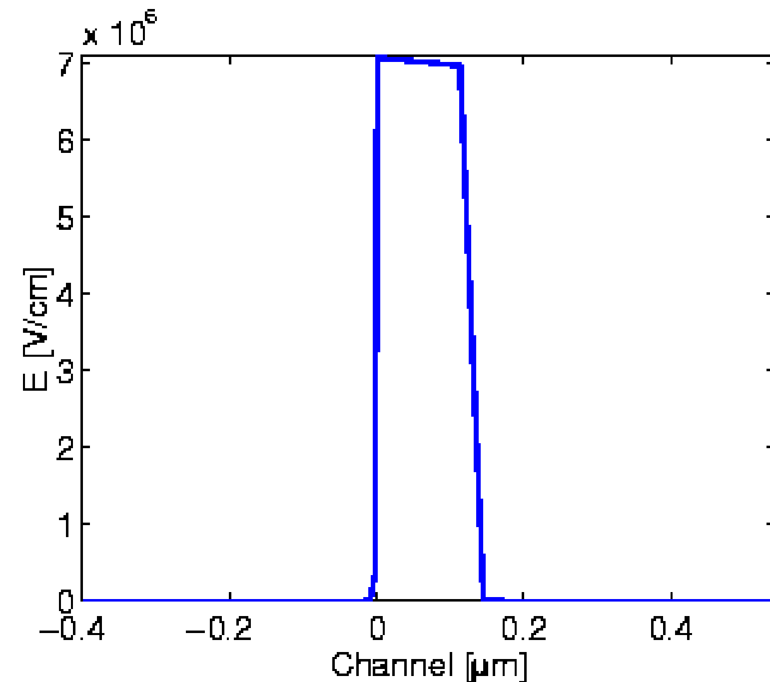






Resulting Electrostatic Potential inside 0.14μm MOSFET: Bias Conditions for Oxide Breakdown





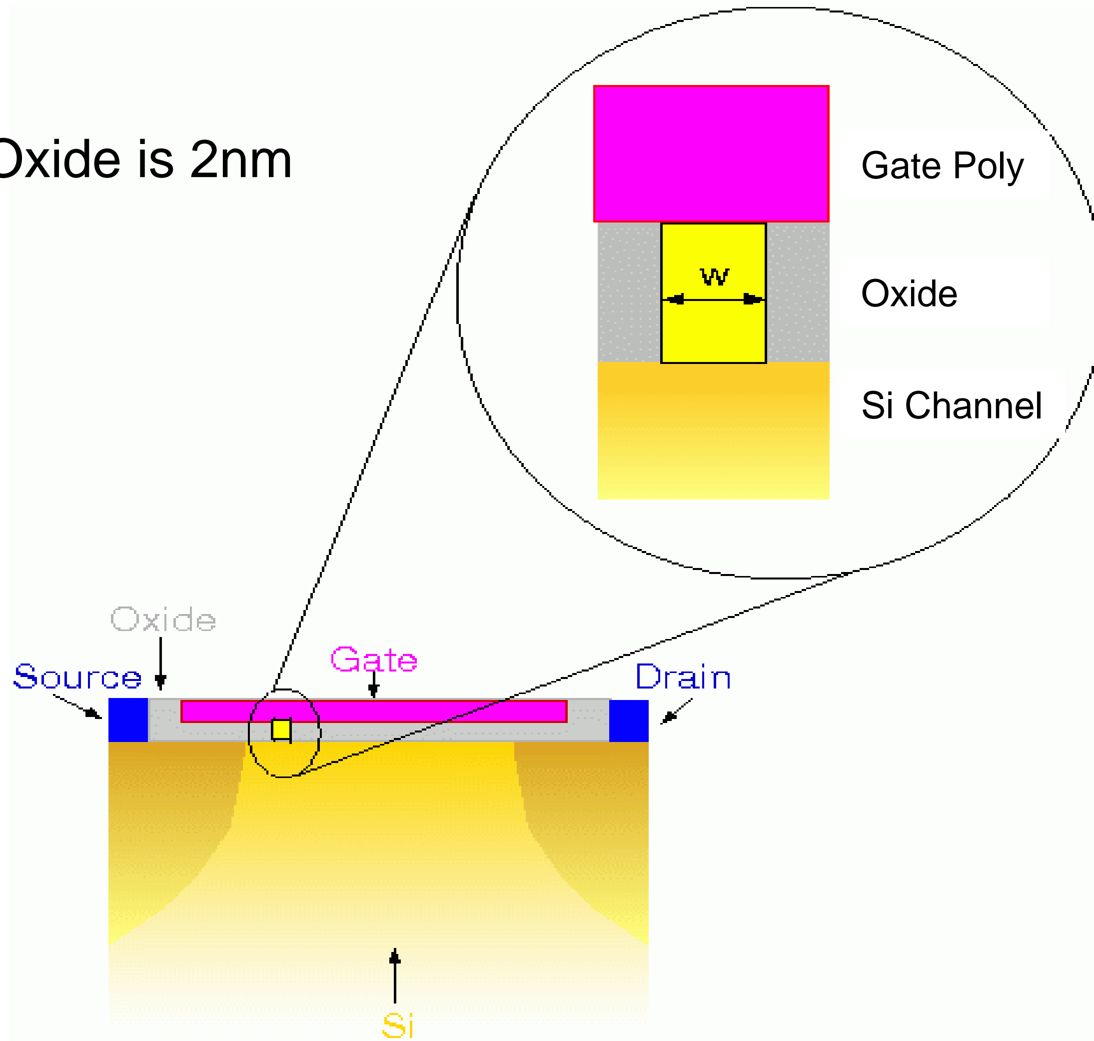
V_G=2.8V V_D=1.4V V_S=V_B=0V

If $|E_y|$ > 7MV/cm => Oxide Breakdown

Device Simulations predicts induced gate voltage of 2X supply causes MOSFET oxide damage

MOSFET Gate Dielectric Breakdown:
Formation of channels in oxide between gate and channel

Gate Oxide is 2nm thick



Modeling Effects of Channel Formations: Current deviates & flows to gate.

$$\nabla^2 \phi = -\frac{q}{\varepsilon}(p - n + D)$$

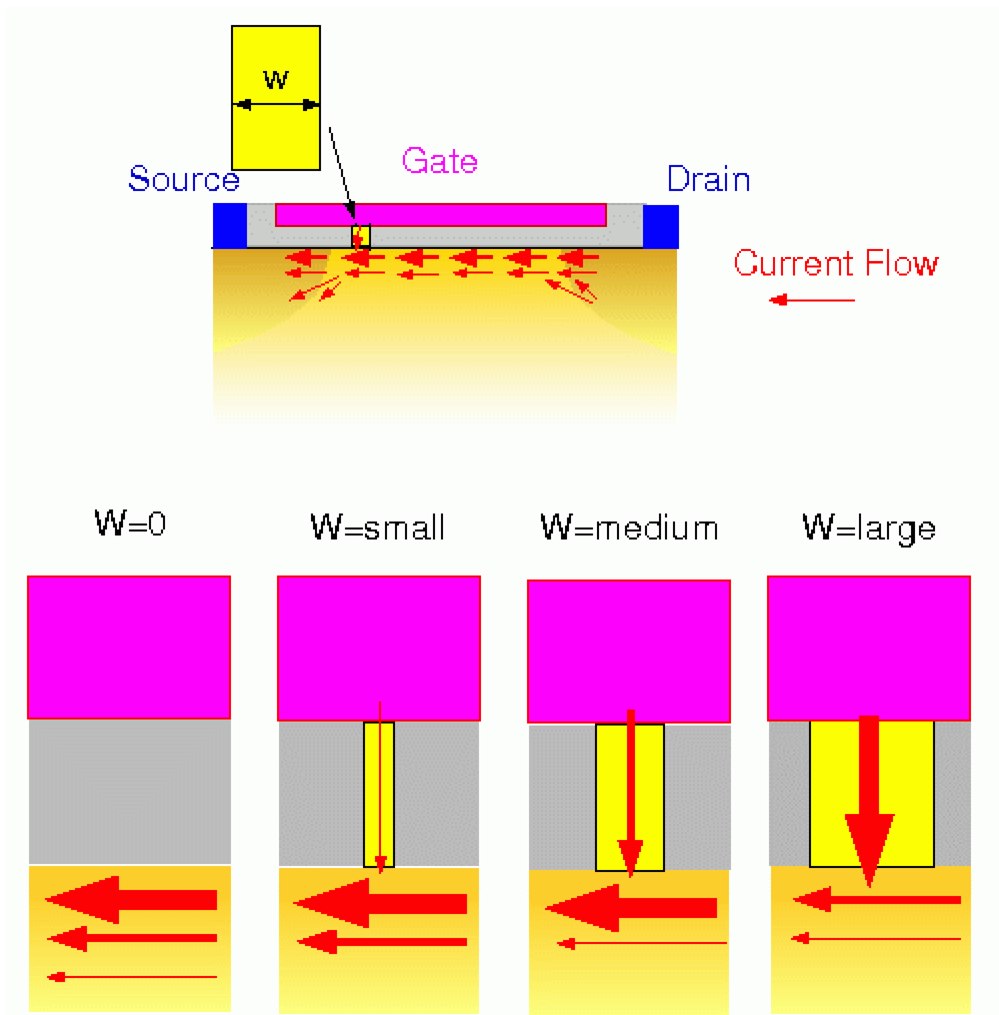
$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . J_n - R_n + G_n$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . J_p - R_p + G_p$$

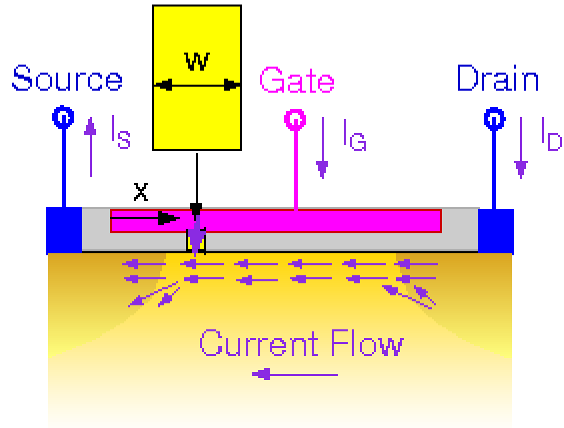
Poisson Eqn.

Electron Current Continuity Eqn.

Hole Current Continuity Eqn.



Effect of Different Breakdown Channel Locations on MOSET

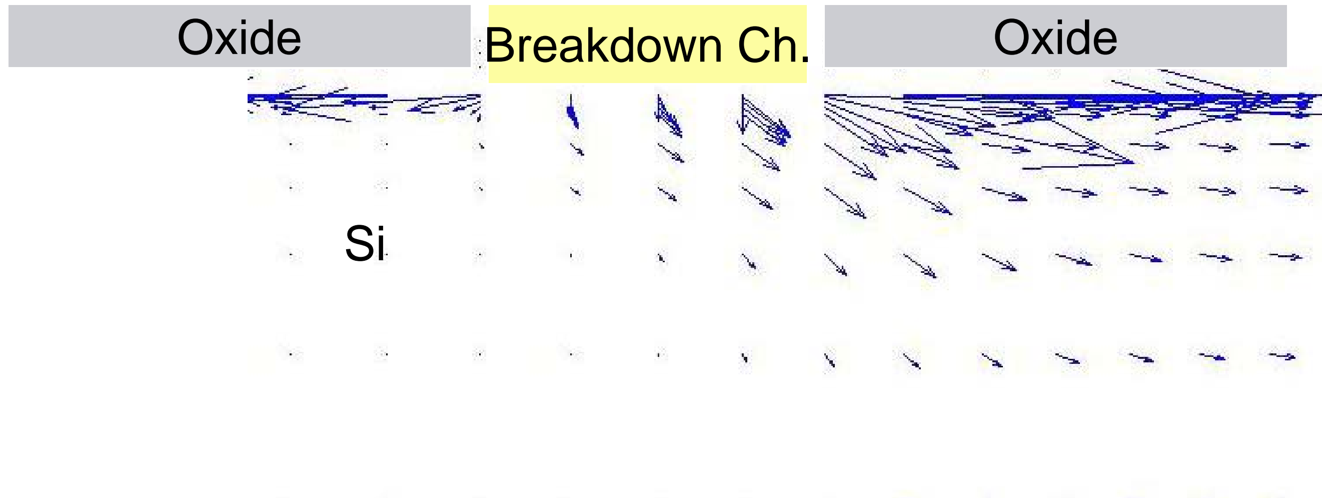


w=0.01μm Channel Length=0.13 μm

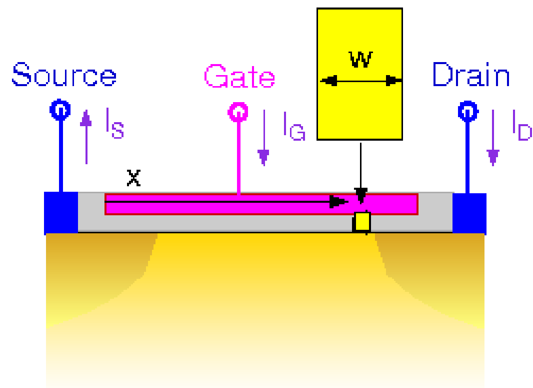
V_{GS}=2.0V V_{DS}=0

X (μm)	I_G (A/μm)	I_S (A/μm)
0.02	5.18E-3	4.01E-3
0.05	2.79E-3	1.46E-3
0.08	2.81E-3	1.32E-3
0.11	1.13E-2	1.14E-3

X=0.11μm



Modeling Different Breakdown Channel Widths:



x=0.11µm Channel Length=0.13 µm
V_{GS}=2.0V V_{DS}=0

w (µm)	I_G (A/µm)	I_D (A/µm)
0.005	5.64E-3	-3.26E-3
0.01	1.13E-2	-7.34E-3
0.015	1.95E-2	-1.35E-2

Task 2. EM Effects on Gates

Differential equation based modeling of EM effects on inverter circuits

- Stage 1: Develop simulation tool.
- Stage 2: Use tool to analyze distributed effects of EM GHz range coupling on fundamental computer chip circuit elements.

Developed Distributed Circuit Simulator Applied to Inverters

DD Equations

$$\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}}(p - n + D)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . \overrightarrow{J_n} - R_n + G_n$$

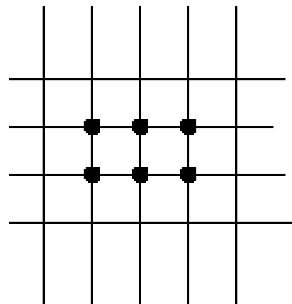
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . \overrightarrow{J_p} - R_p + G_p$$

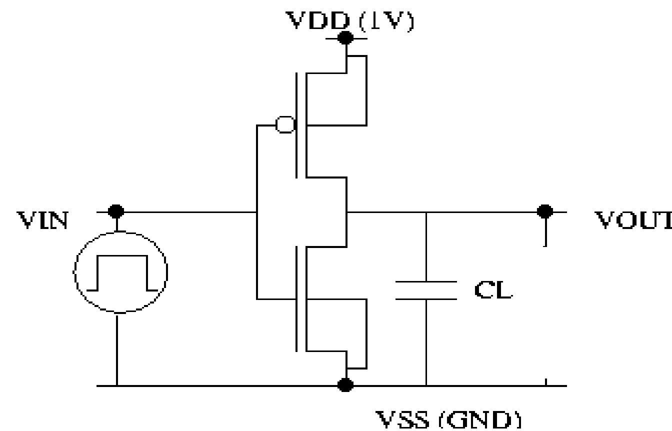
Supplementary DD Equations

$$\overrightarrow{J_n} = -q\mu_n n\overrightarrow{\nabla\Phi} + q\mu_n V_T \overrightarrow{\nabla n}$$

$$\overrightarrow{J_p} = -q\mu_p p\overrightarrow{\nabla\Phi} - q\mu_p V_T \overrightarrow{\nabla p}$$

Coupled Discretized DD Equations are solved at each mesh point





CMOS Inverter (CMI)

Lumped KCL equation check at the output node and using the KCL equation, the output guess is updated for the next iteration, V_O^{i+1}:

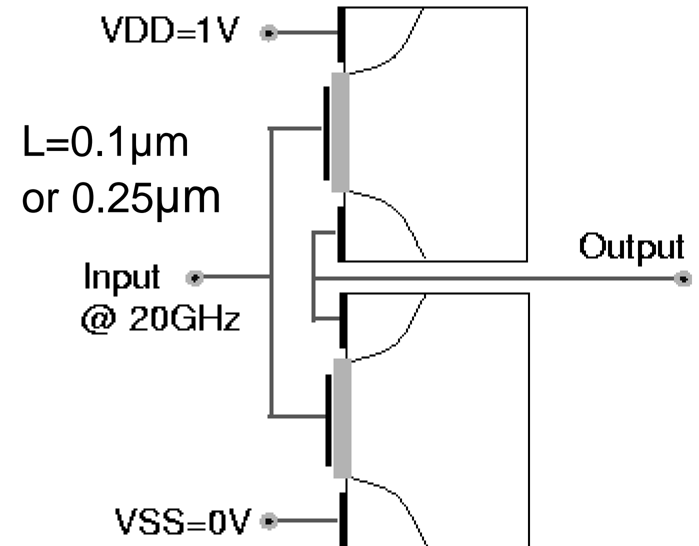
$$I_{DN} - I_{DP} + I_{R_L} + I_{C_L} = 0$$

$$A_N + B_N V_o^{i+1} + A_P + B_P V_o^{i+1} + \frac{V_o^{i+1} - V_{SS}}{R_L} + C_L \frac{V_o^{i+1} - V_o^i}{\Delta t} = 0$$

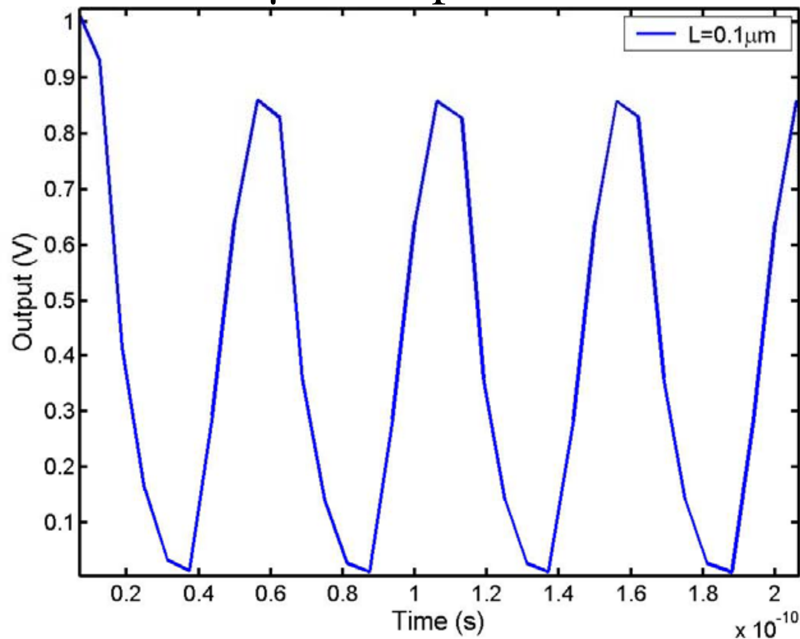
$$V_o^{i+1} = \frac{V_{SS} + V_o^i \frac{R_L C_L}{\Delta t} - (A_N + A_P) R_L}{1 + \frac{R_L C_L}{\Delta t} + (B_N + B_P) R_L}$$

Modeling 20GHz, 1V Coupled to 0.1μm & 0.25μm Inverters

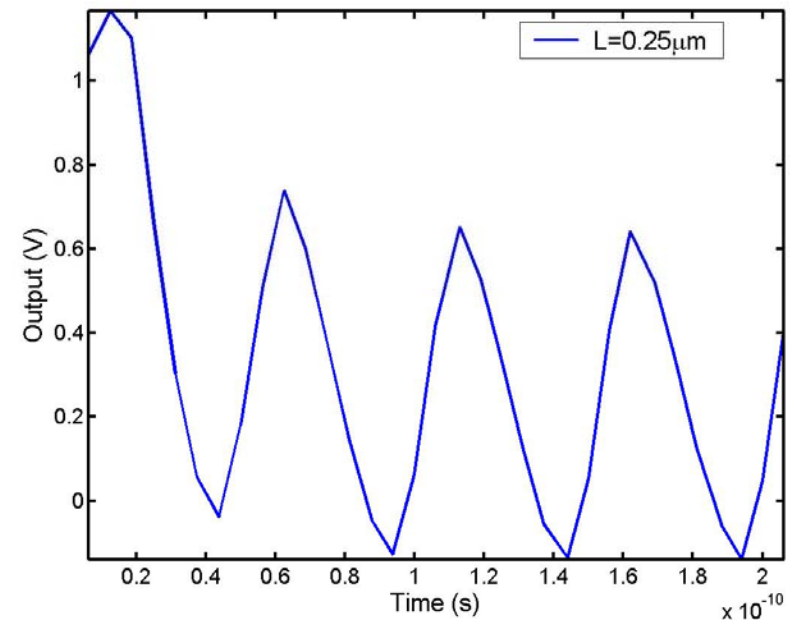
- Output follows input but with reduced amplitude in 0.25
- Bit errors can still occur in larger device but may be less likely



0.1μm Output



0.25μm Output



Summary of Device Modeling of EM Effects

- We have developed a device simulator to model EM coupling effects inside transistors.
- Simulations allow us to probe inside transistors where experimental probes can not reach, pinpointing regions of failure. (Circuit simulators like SPICE can not show this since they which only perform lumped analyses.)
- Technique developed to simulate oxide breakdown.
- Location of avalanching shown to be near source-channel junction.
- Transient inverter simulations show smaller devices more susceptible to bit errors.
- High frequency transients appear to be less likely to induce damage than low frequency transients.
- It therefore follows that demodulation effects of nonlinear device structures can give rise to breakdowns. (Rogers)
- Major benefit of simulator is that it can predict breakdown of devices not yet built. (It provides a virtual device without the investment.)
- We can use virtual (simulated) device to extract SPICE models and simulate large circuits before actually building any of them.

Task 3. Interconnects and Passive Elements

Developed Finite Difference Time Domain Alternating Direction Implicit Method (FDTD-ADI) for Solving Maxwell's Equations on Chip.

Motivations & Challenges

- Interconnects: Skin depth effect in the metal layer. Thin insulator layer. Substrate current.
- EM wave scattering and penetration: Model the EM field distribution in the close proximity and within the natural and synthetic conductive material
- Broadband signal propagation in-door environment.
- How to couple large EM wavelength (mm to cm) scale with fine material structure (of um scale) in the same simulation?
- Conventional FDTD method limited by Courant's Condition: $\Delta t < \dfrac{1}{c\sqrt{\dfrac{1}{\Delta x^2} + \dfrac{1}{\Delta y^2} + \dfrac{1}{\Delta z^2}}}$

ADI Schemes

$$\frac{\partial \varepsilon \overrightarrow{E}}{\partial t} = \nabla \times \frac{\overrightarrow{B}}{\mu} - \sigma \overrightarrow{E}$$

$$\frac{\varepsilon E^{n+1}_{x,(i+1/2,j,k)} - \varepsilon E^{n}_{x,(i+1/2,j,k)}}{\Delta t} =$$

$$\frac{1}{\mu}\frac{B^{n+1}_{z,(i+1/2,j+1/2,k)} - B^{n+1}_{z,(i+1/2,j-1/2,k)}}{\Delta y}$$

$$-\frac{1}{\mu}\frac{B^{n}_{y,(i+1/2,j,k+1/2)} - B^{n}_{y,(i+1/2,j,k-1/2)}}{\Delta z}$$

$$-\sigma E^{n+1}_{x,(i+1/2,j,k)} \quad \textbf{... (1)}$$

$$\frac{\partial \overrightarrow{B}}{\partial t} = -\nabla \times \overrightarrow{E}$$

$$\frac{B^{n+1}_{z,(i+1/2,j-1/2,k)} - B^{n}_{z,(i+1/2,j-1/2,k)}}{\Delta t}$$

$$= \frac{E^{n+1}_{x,(i+1/2,j,k)} - E^{n+1}_{x,(i+1/2,j-1,k)}}{\Delta y} -$$

$$\frac{E^{n}_{y,(i+1,j-1/2,k)} - E^{n}_{y,(i,j-1/2,k)}}{\Delta x} \quad \textbf{... (2)}$$

Example for one component

Namiki, 1999; Zheng et al., 1999

ADI Continued

- Substitute (2) to (1) and form

$$a \times E^{n+1}_{x,(i+1/2,j-1,k)} + b \times E^{n+1}_{x,(i+1/2,j,k)}$$
$$+ c \times E^{n+1}_{x,(i+1/2,j+1,k)} = d$$

(a tri-diagonal matrix).

- Alternate the implicitness for the other Ey, Ez; Bx, By components.

Form 3 Tri-Diagonal systems for three Electric field components.

- Solve for next time step E^{n+1} with tri-diagonal matrix solver. Use (2) and E^{n+1} to update B^{n+1}.

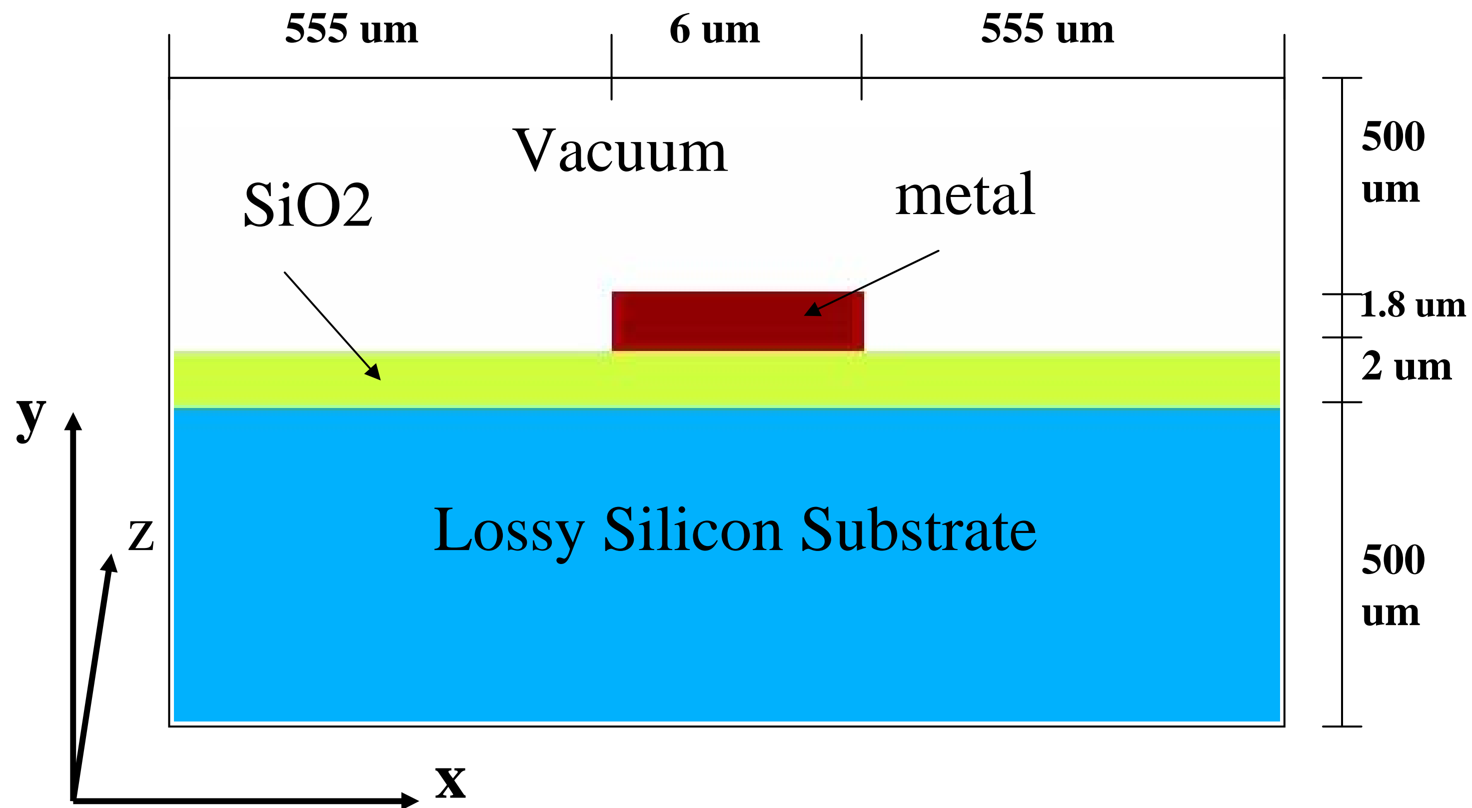
Step 2:

- Treat the other half (H_y) of equ. (1) as implicit and perform similar calculation as in step 1.

Fully coupled to Mur's first order absorption boundary condition.

Time step is chosen to resolve key temporal behavior.

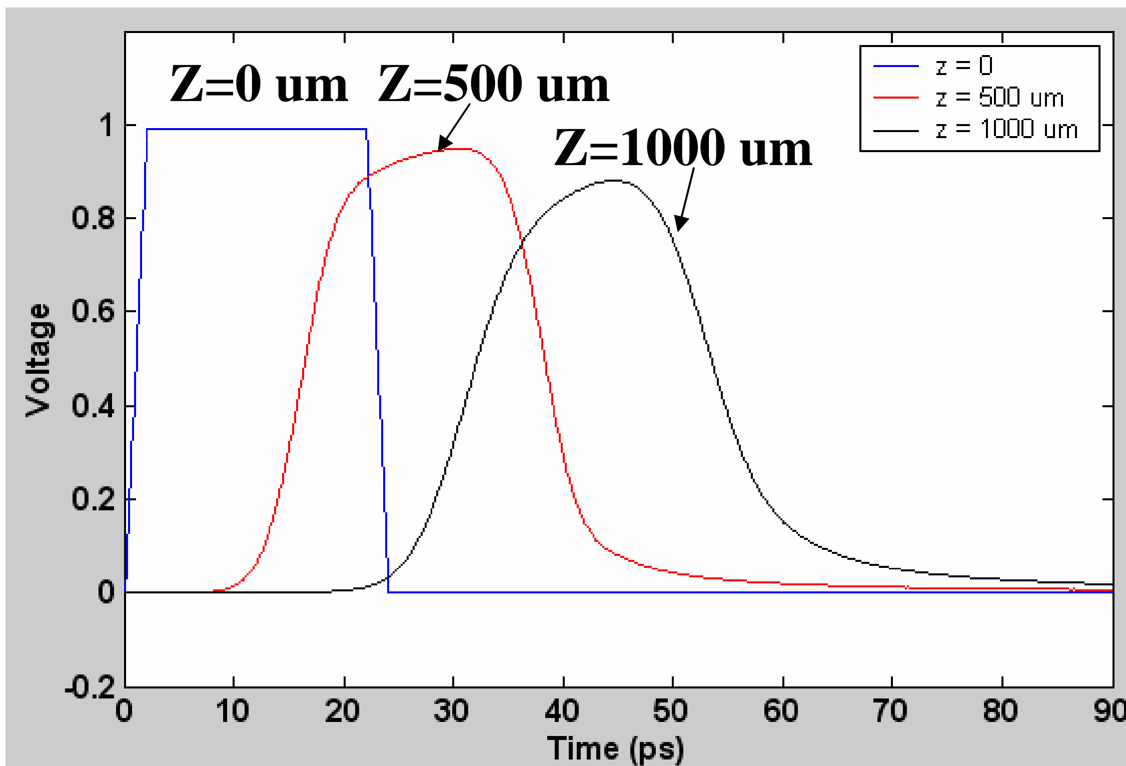
Simulating Signal Propagation along Metal-Insulator-Silicon (MIS) Interconnect



Simulation Performance

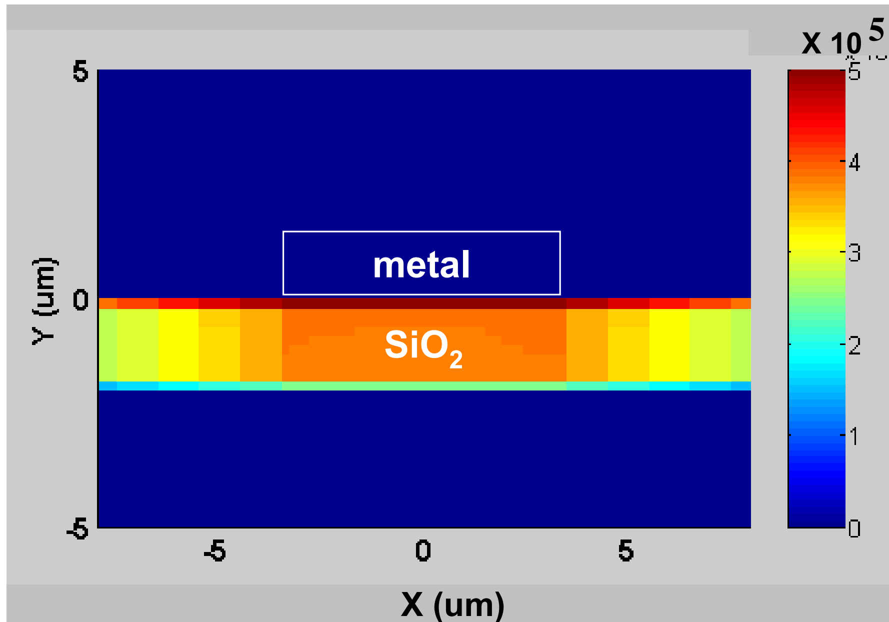
- Non-uniform grid in the cross section; smallest grid size in the cross section is 0.1 um. Uniform grid = 25 um in the propagation direction.
- Simulation $\Delta t = 2 \times 10^{-13}$ sec. Courant's limit is
  $\Delta t < 0.33 \times 10^{-15}$sec
- Simulation time is 3-4 hour on a PC for 1000 step simulation.
- Outer boundary condition: Mur's first order

Voltage observed at different Z locations along the MISS Strip



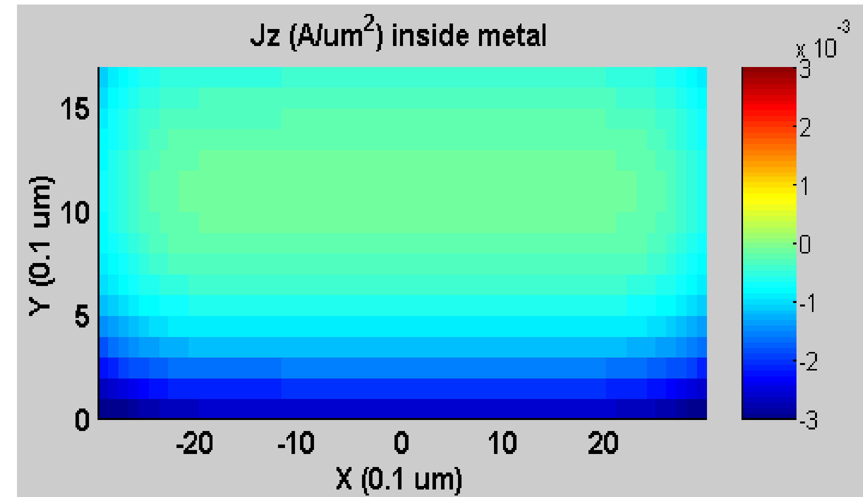
- A fast 1V, 20psec digital pulse of rise-time= 2ps is excited
- Substrate doping $n = 10^{17}$ /cm^3
- Metal conductivity $= 5.8\text{x } 10^7$ S/m.
- Shows digital signal losses and dispersion.

Cross Section of Ey field



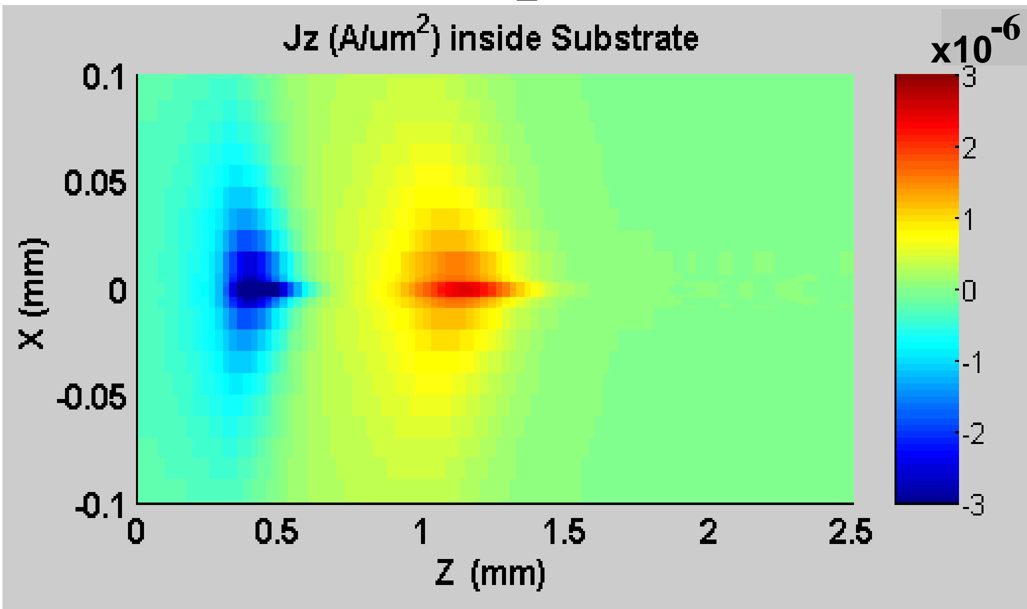
• Electric field concentrates inside the SiO_2 layer.

Cross Section of Current Jz inside Metal

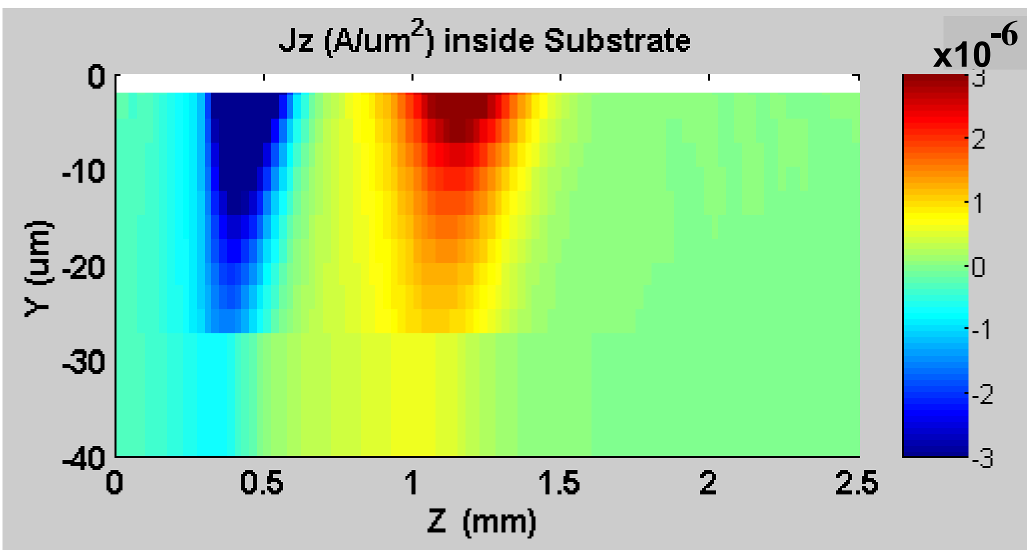


• X, Y units are 0.1 um.
• Skin depth effect.
• metal edge effect.

Snap-shot of Substrate Current



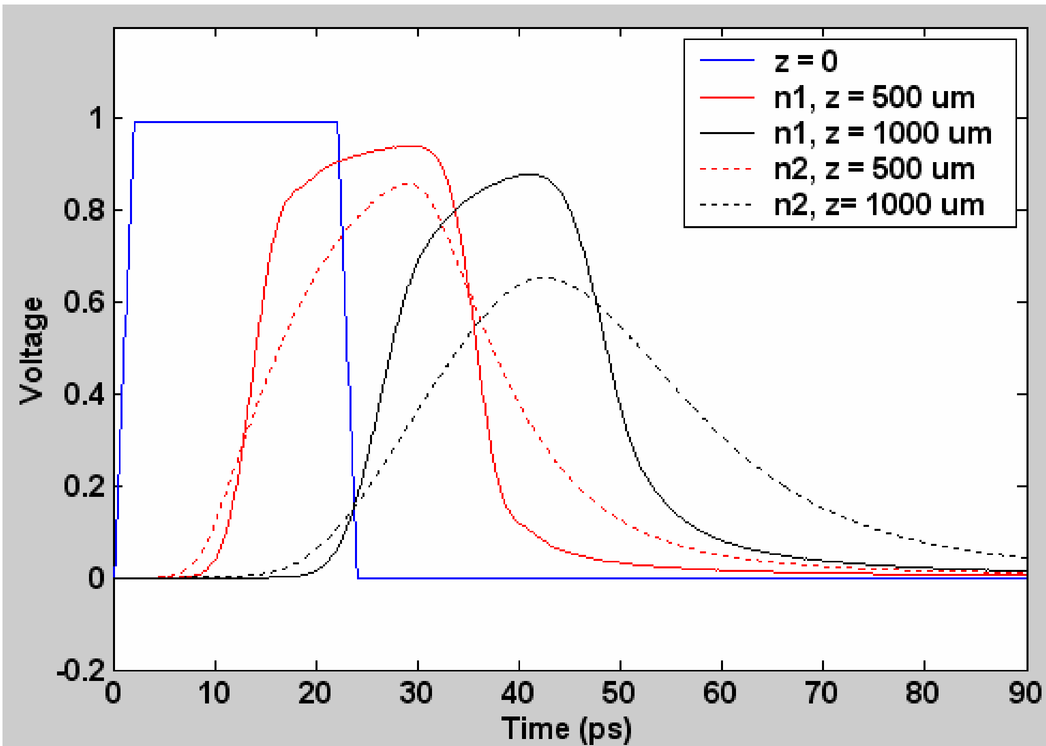
Top view



Side View

- Red and blue shade correspond to rising and falling of the signal.
- Top view shows potential interference and coupling in lateral direction (tenth mm scale).
- Side view Shows current penetration to the substrate.

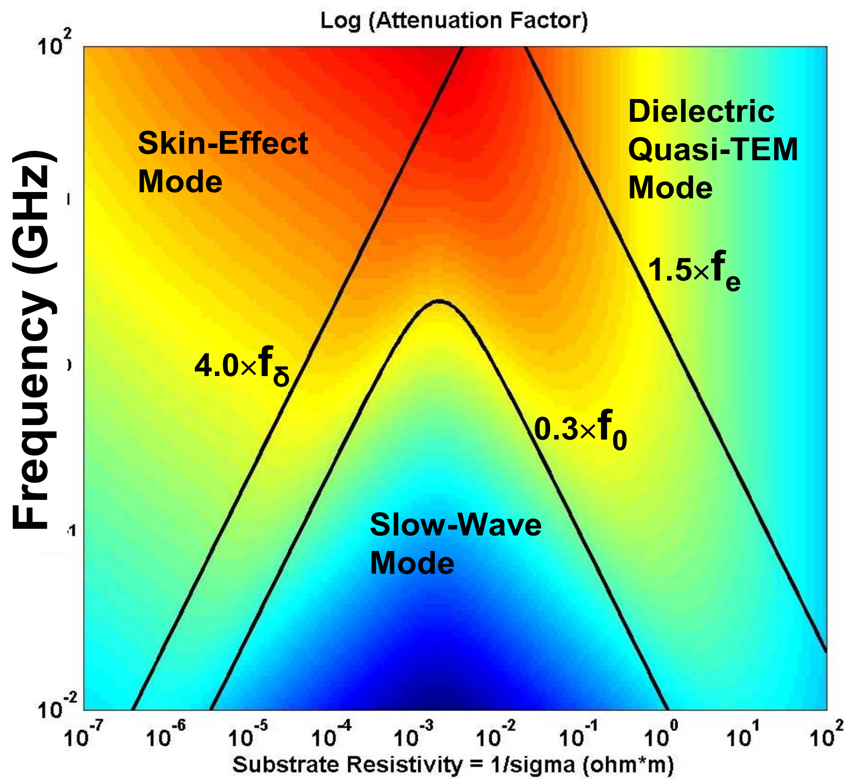
Signal Propagation with Different Substrate Doping



- n1 = 10^{18} /cm^3 (solid)
- n2 = 10^{16} /cm^3 (dashed)
- At the skin-effect mode, higher substrate doping conforms signal better.

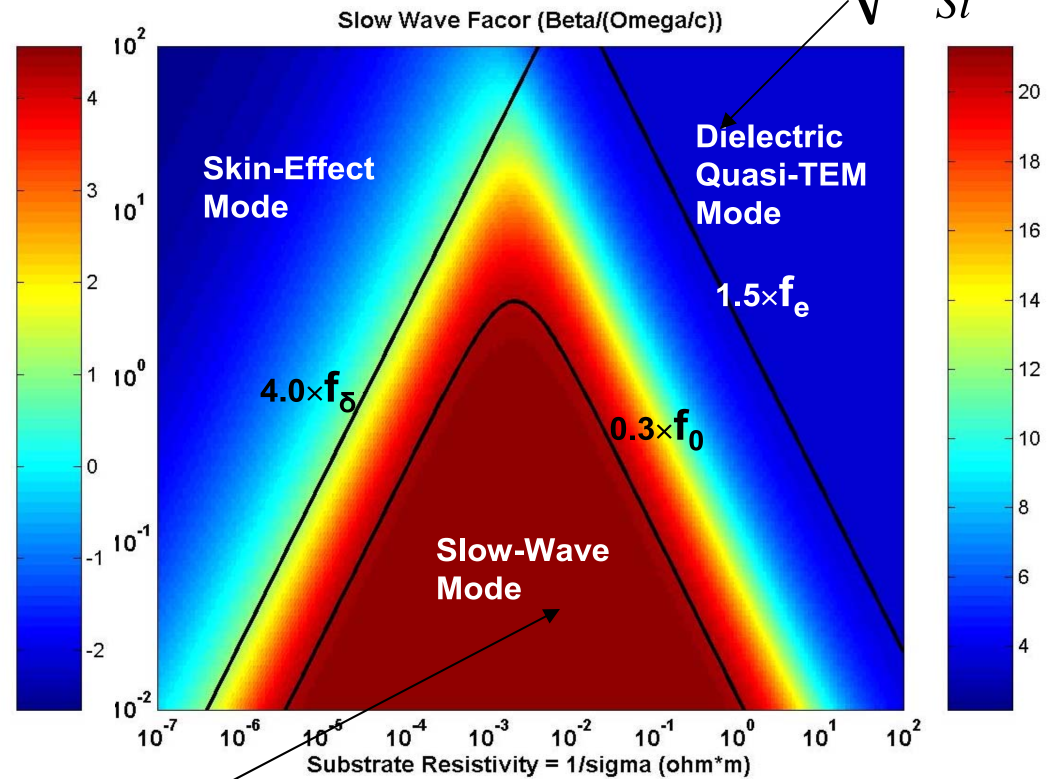
Three Fundamental Propagation Modes for MIS Structure

Log (Attenuation Factor)



Substrate Resistivity

Slow Wave Factor (c/V_{phz}) $\sqrt{\varepsilon_{Si}}$



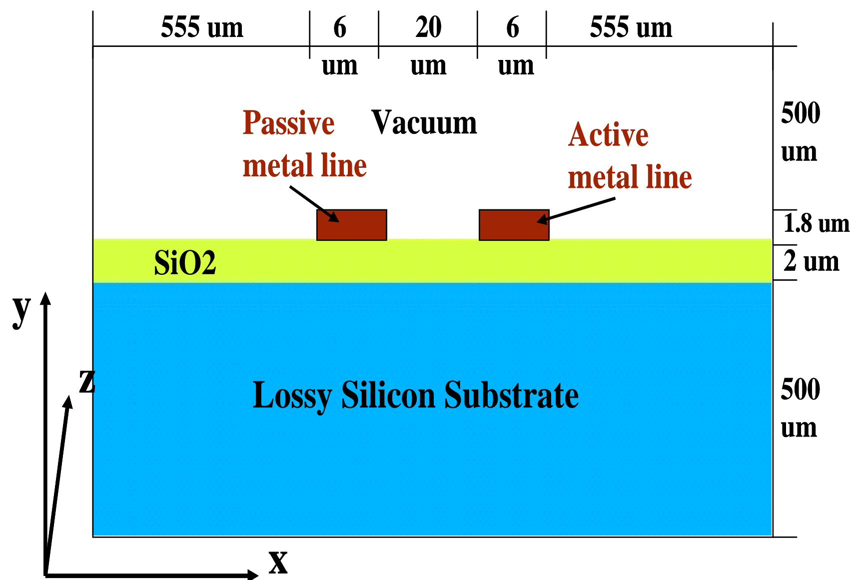
$\sqrt{\varepsilon_{SiO_2}(b/b_1)}$

Substrate Resistivity

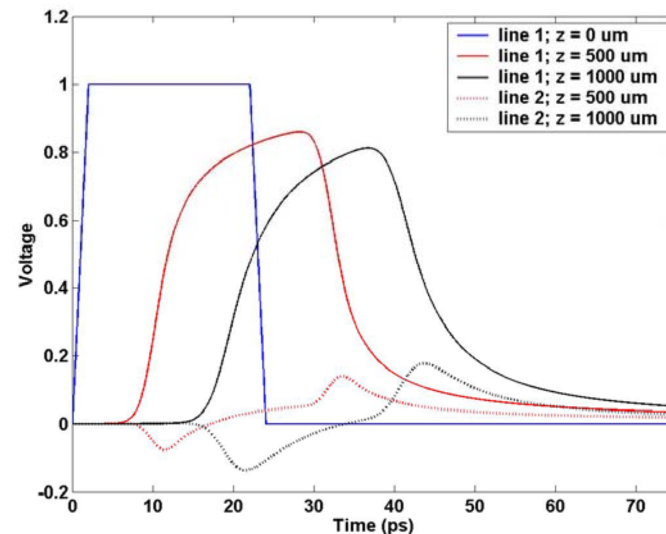
$$f_\delta = \frac{1}{2\pi}\frac{2}{\mu_0\sigma_2 b_2^2} \quad f_e = \frac{1}{2\pi}\frac{\sigma_2}{\varepsilon_2\varepsilon_0} \quad f_s = \frac{1}{2\pi}\frac{\sigma_2}{\varepsilon_1\varepsilon_0}\frac{b_1}{b_2} \quad f_0 = \left[f_s^{-1} + \frac{2}{3}f_\delta^{-1}\right]^{-1}$$

Simulating EM Coupling between Interconnect Lines in Metal-Insulator-Silicon-Substrate (MISS) Structure

Adjacent Interconnects X-section



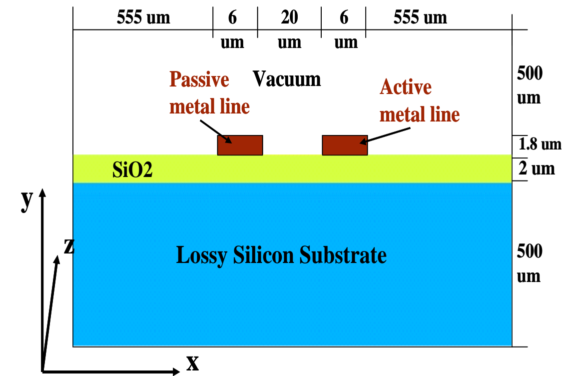
Voltage Pulse Coupling Results



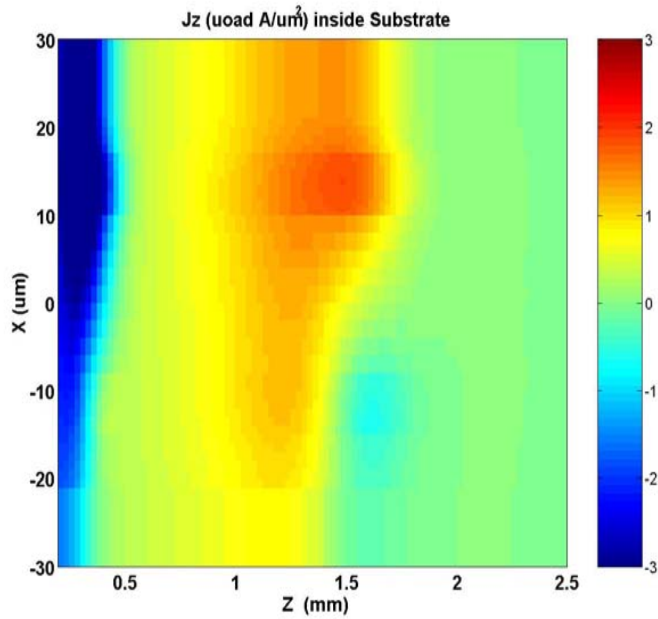
Results: New simulator allows for resolving large variations in grid points

Induced voltage 20% of applied signal even at 20μm apart.

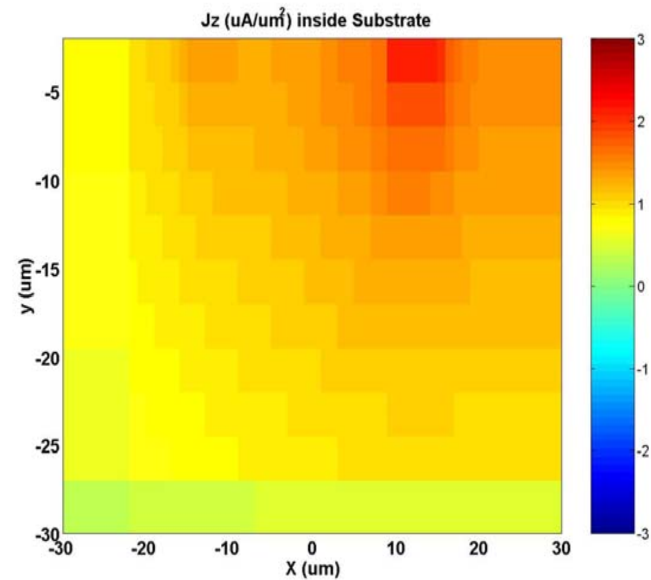
Simulations show extensive coupling through substrate currents.



Substrate Current: Horizontal x-section



Substrate Current: Vertical x-section



Task 2: Accomplishments

- Developed Maxwell Equation based CAD tool for modeling on-chip interconnects and passive structures.
  - New tool overcomes Courant limit and is thus well suited for analyzing chips where resolving mm and μm size structure simultaneously.
  - Applied the new tool to modeling propagation of pulses along IC interconnect transmission lines.
  - Simulations show details of fields and current densities inside semiconductor substrate and metal interconnects
  - Simulations indicate significant losses and dispersion which depend on the doping density of the semiconductor substrate and geometry
  - Simulations indicate extensive coupling between interconnect lines. 20% percent coupling is seen on lines as much as 20μm apart.
- New tool used to extract 3 fundamental propagation modes for transmission lines on semiconductor chips
  - Slow Wave Mode
  - Skin Effect Mode
  - Dielectric Quasi TEM Mode

Task 3: EM-Sensitive Passive Components on Semiconductor Chips: Modeling, Testing and Design

- Modern RF circuits often feature on-chip inductors required by circuit design
  - Operating frequencies are high enough to make this feasible
- Increasing circuit complexity also creates other inductive components
  - Long transmission (bus) lines; signal/clock distribution networks…

Motivation

- Investigating parasitic effects
  - Vulnerability to external EM coupling
  - Potential to create on-chip interference
    - Radiation
    - Substrate current
- System-on-a-chip RF circuits require on-chip inductors with high L, small area and high Q
  - Automated design and speedy evaluation of geometrical tradeoffs.
- On-Chip Inductors are fundamental elements for RF IC's.
- Different geometries will resonate with different external RF

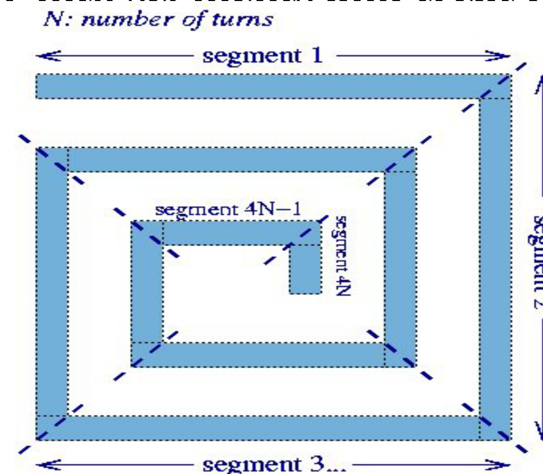
Issues for On-Chip Passive Components

- Semiconductor substrates are conductive→ unable to treat system as metal/dielectric/ground plane
  - New processes feature higher doping, higher conductivity
- Device circuits underneath metal structures display variable doping
  - Non-uniform substrate: n+ and p+ active regions, n-wells, p-wells, lightly doped chip substrate…

Inductor Modeling---Theory

Modeling Approach: **Divide a spiral inductor into segments and treat each current segment separately.**

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} L_{11} & L_{m,12} & \cdots & L_{m,1N} \\ L_{m,21} & L_{22} & \cdots & L_{m,1N} \\ \vdots & \vdots & \cdots & \vdots \\ L_{m,N1} & L_{m,N2} & \cdots & L_{NN} \end{bmatrix} \bullet s \begin{bmatrix} I \\ I \\ \vdots \\ I \end{bmatrix}$$



L_{kk}=self-inductance (external+internal) of segment k

Sources: Frequency-dependent current distribution within the segment and the magnetic flux linkage to the loop formed by the segment and its return current.

L_{kl}=mutual inductance between segments k and l

Sources: Magnetic flux linkage of the current in the first segment to the loop formed by the second segment and its return current.

***Lossy substrate effect**:* The return current has an effective distance into the substrate; this is frequency-dependent and can be modeled as a *complex* distance to account for the losses.

Other frequency dependency: Skin effect in the metal; current crowding in the metal

Mutual Inductance

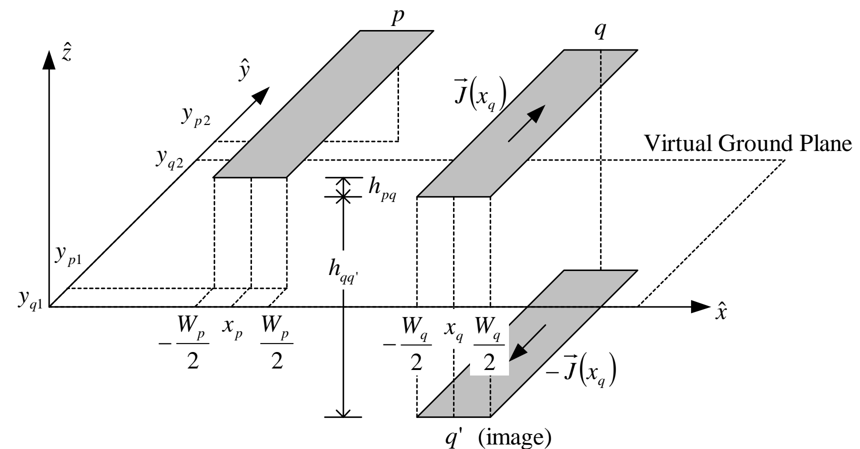
Mutual inductance: The magnetic flux created by the current on one loop linking to the area of other loop

$$L_{ij} = \frac{\Psi_{ij}}{I_j}$$

Calculate Ψ from the magnetic vector potential and *I* from the current distribution; the mutual inductance between two current segments is then

$$L_{m,ij} = \frac{\frac{\mu}{4\pi}\frac{1}{a_i}\int_{a_i}\int_{b_i}^{c_i}\int_{a_j}\int_{b_j}^{c_j}\frac{J_j d\vec{l}_i \bullet d\vec{l}_j}{R_{ij}}da_i da_j}{\int_{a_j} J_j da_j}$$

Frequency dependency: The signal current of a current segment and its image current both induce voltages on the "target" current segment; the distribution of the image current varies with frequency on a semiconductor substrate.

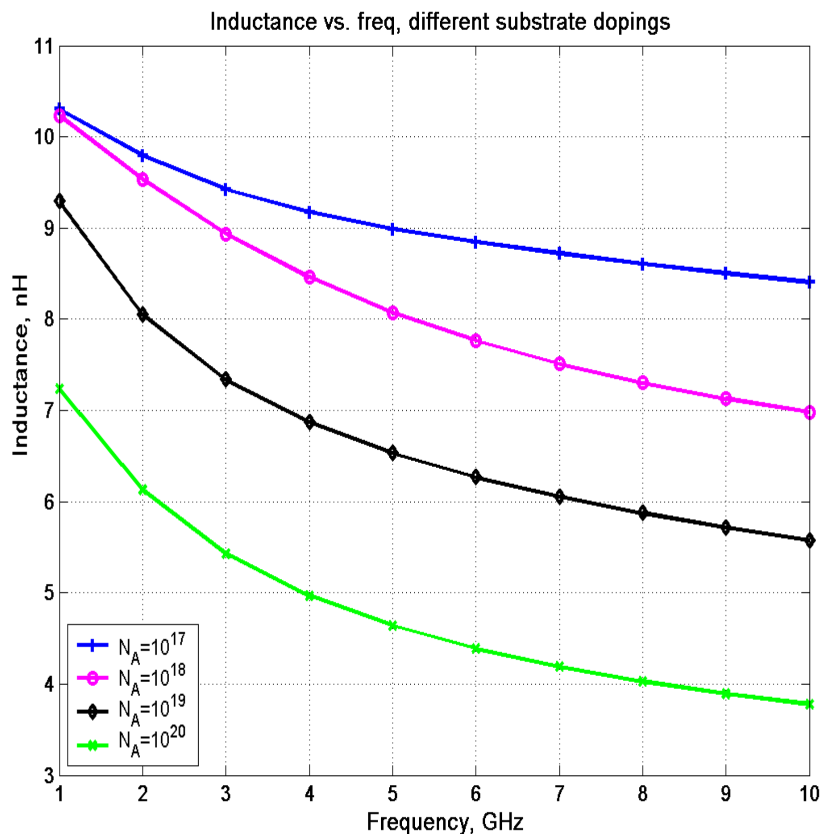


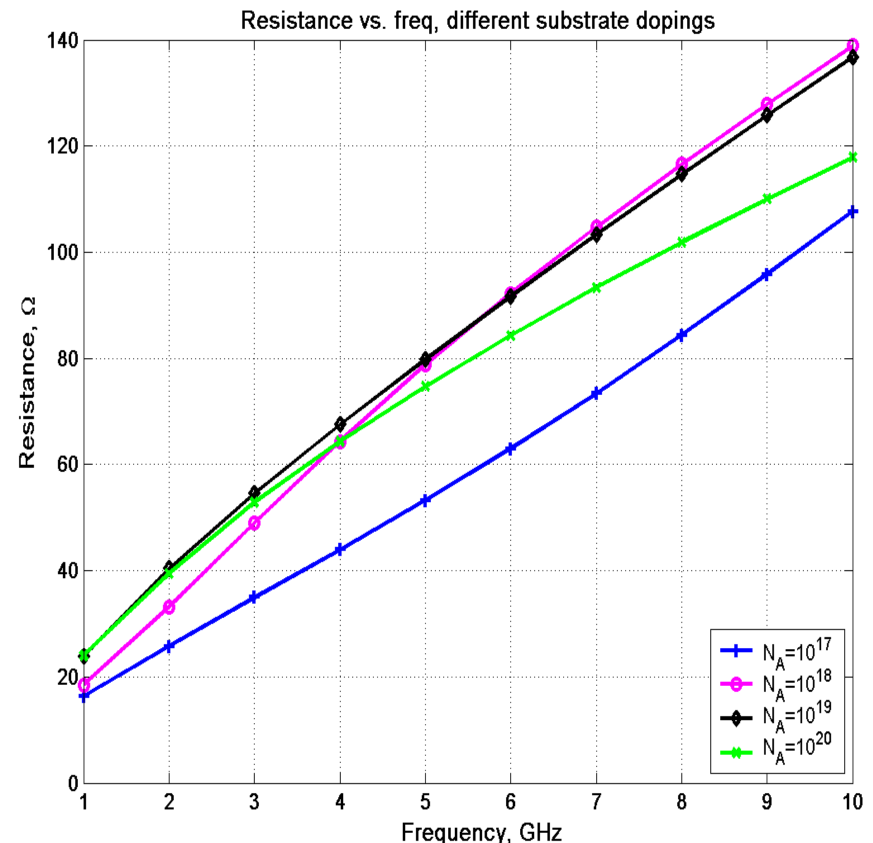
On-Chip Inductor Analysis Issues

- ***Variations in layout:***
  - **Metal layer**
  - **Length**
  - **Number of turns**
  - **Metal trace width**
  - **Metal trace spacing**
  - **Substrate doping**
  - **Shape**
  - **…**

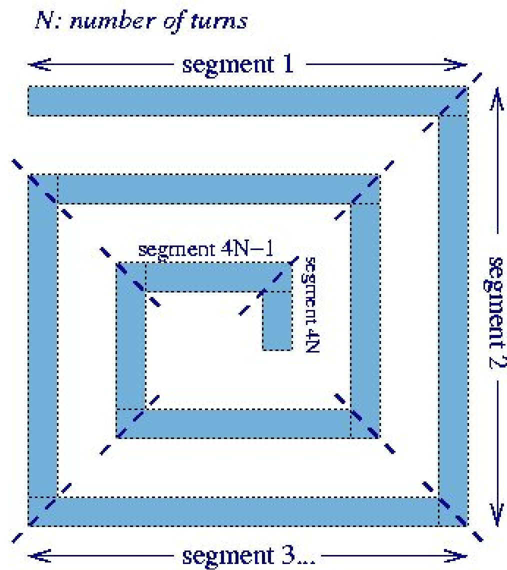
Some Modeling Results

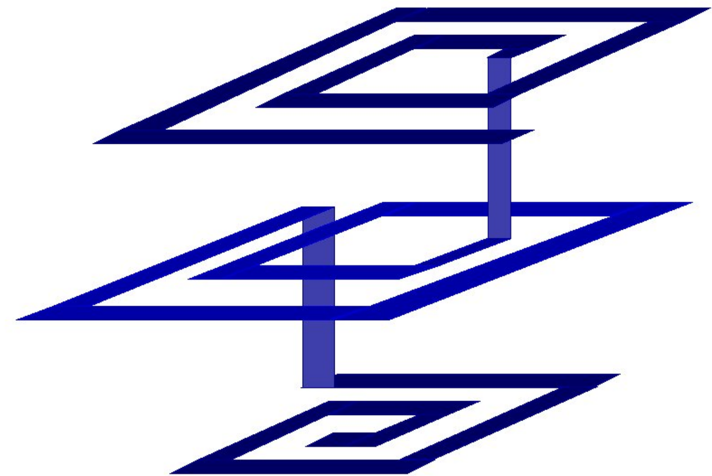
Overall, higher doping reduces inductance (closer return current, smaller loops) and makes it more freq-dependent (low enough doping pushes all current to bottom). Relationship between resistance and doping is not straightforward, since conductivity of substrate affects return current distribution, composition, and its frequency dependence all at the same time and these effects interact.





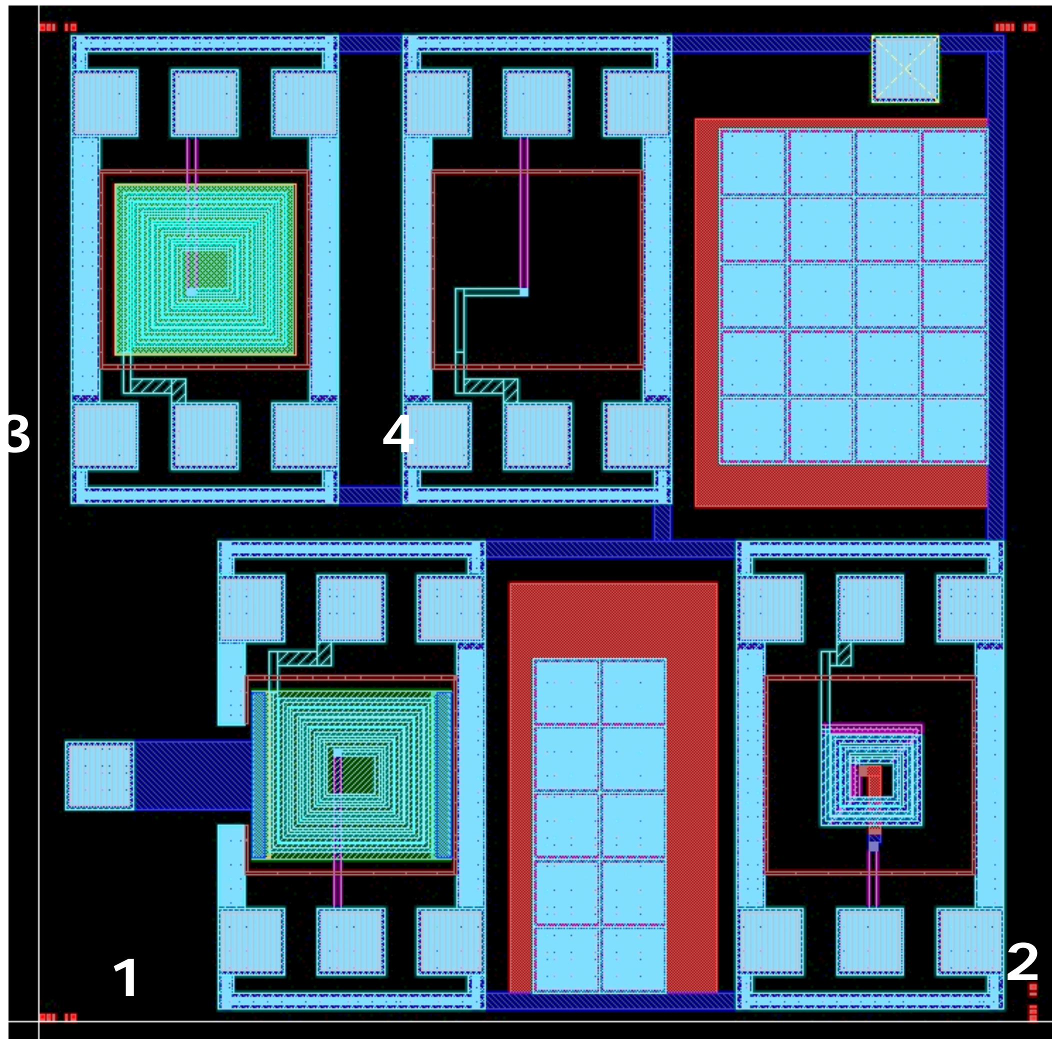
Planar Inductor vs. Multilayer Inductor





Same net length → same net resistance, but higher inductance.
(three - level multilayer)

3D vs Planar Inductors--- Test Chips



1.5mm

Designed for RF-probe station measurements

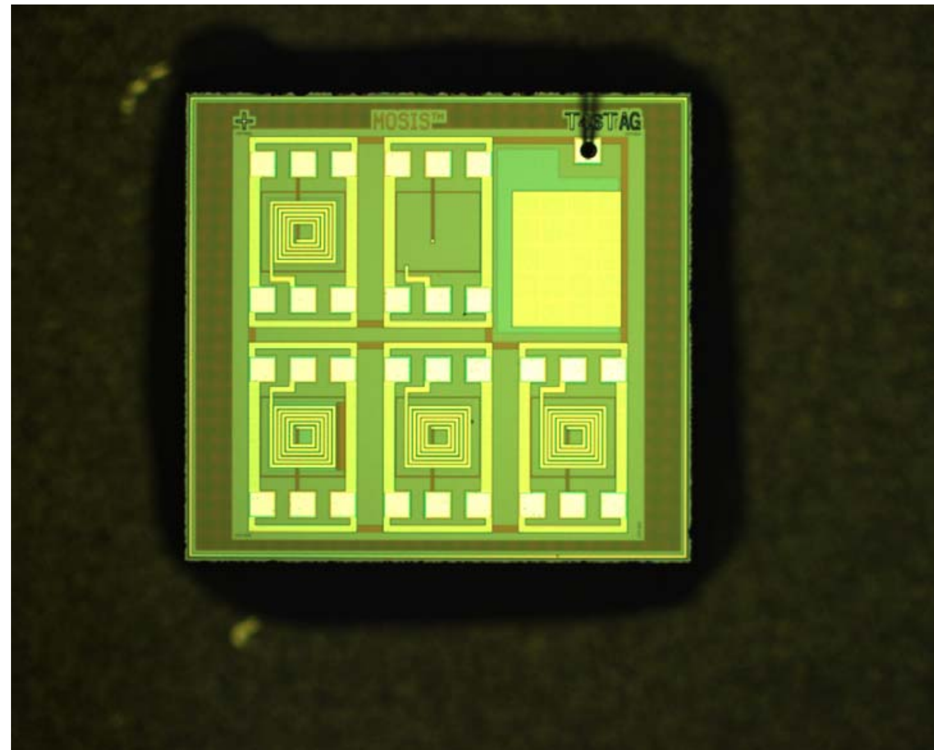
Manufactured through MOSIS

AMIS 0.5 µm; 3 Metal layers

Structures on chip 1:

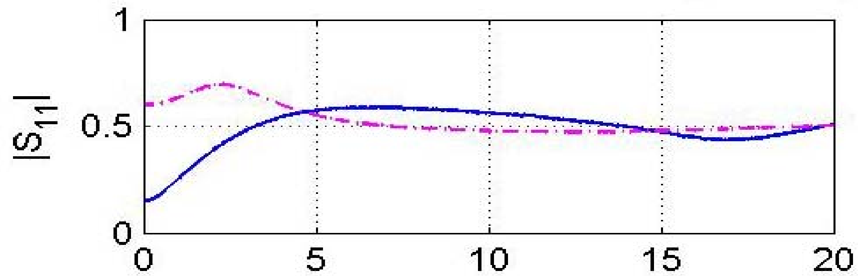
1. **Planar inductor on pin-diode**
2. **Stacked inductor on p-substrate**
3. **Planar inductor on p-plus**
4. **De-embedding structure: Thru**

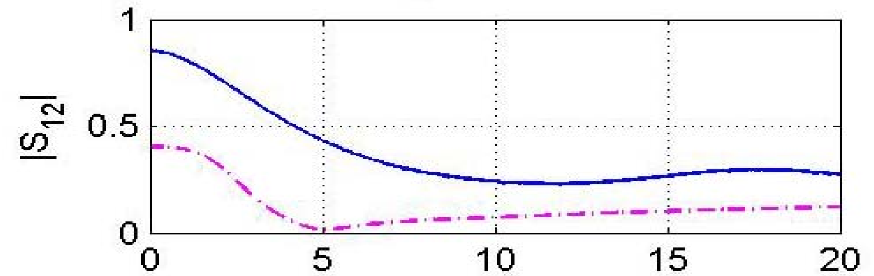
Actual Fabricated On-Chip Inductors

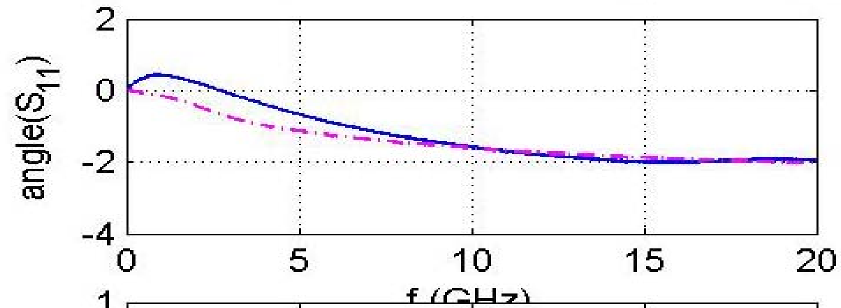


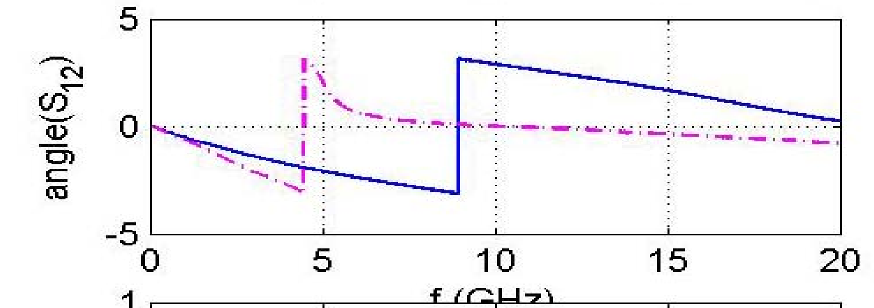
Test Chip: Investigating Micro Geometry
Planar vs Stacked Inductors

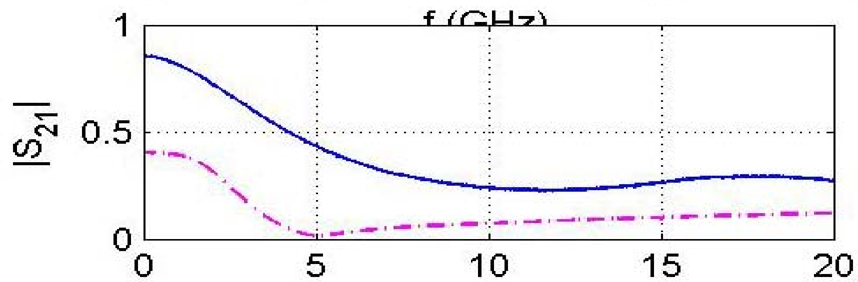
Devices: , planar:b, stacked:m-., pre-deembedding

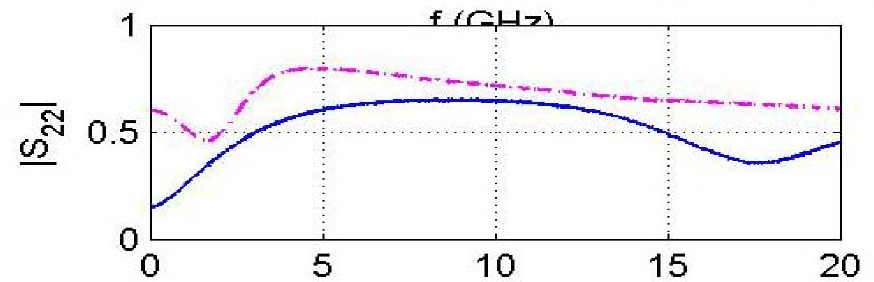


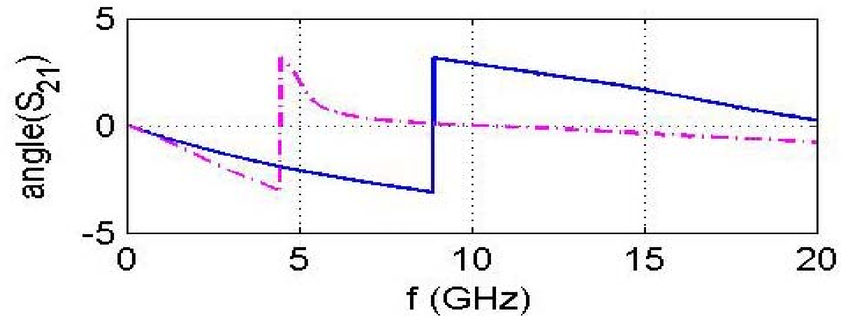


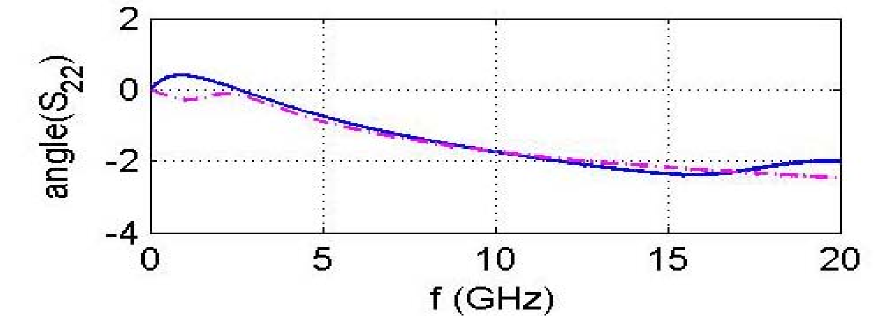




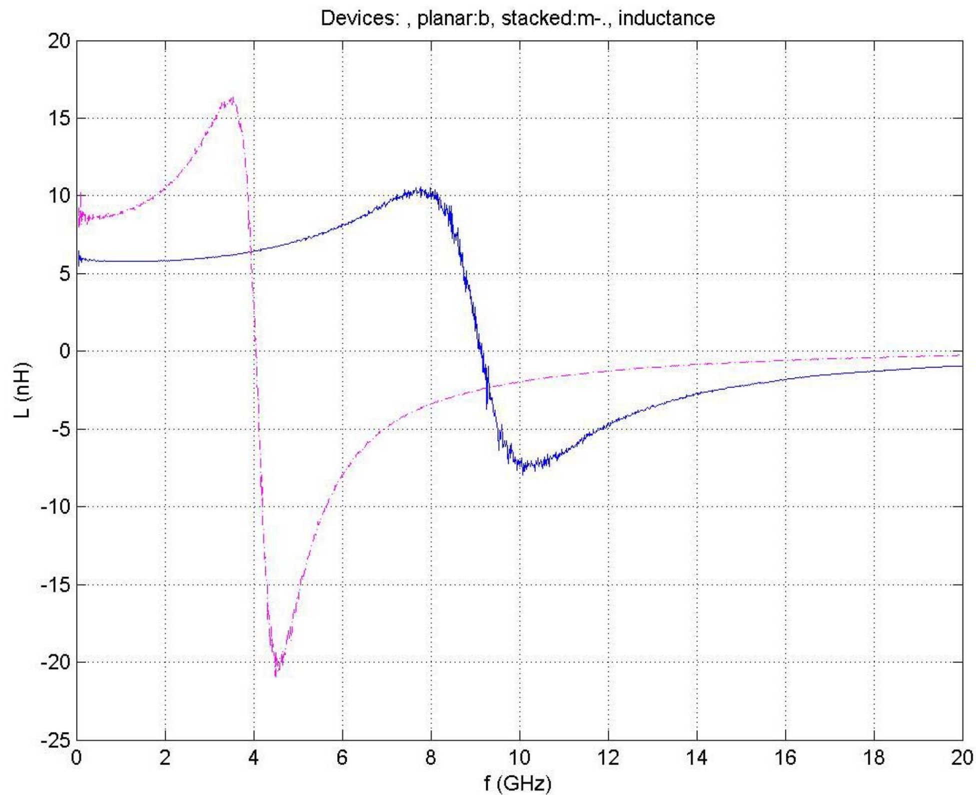








Test Chip: Investigating Micro Geometry Planar vs Stacked Inductors



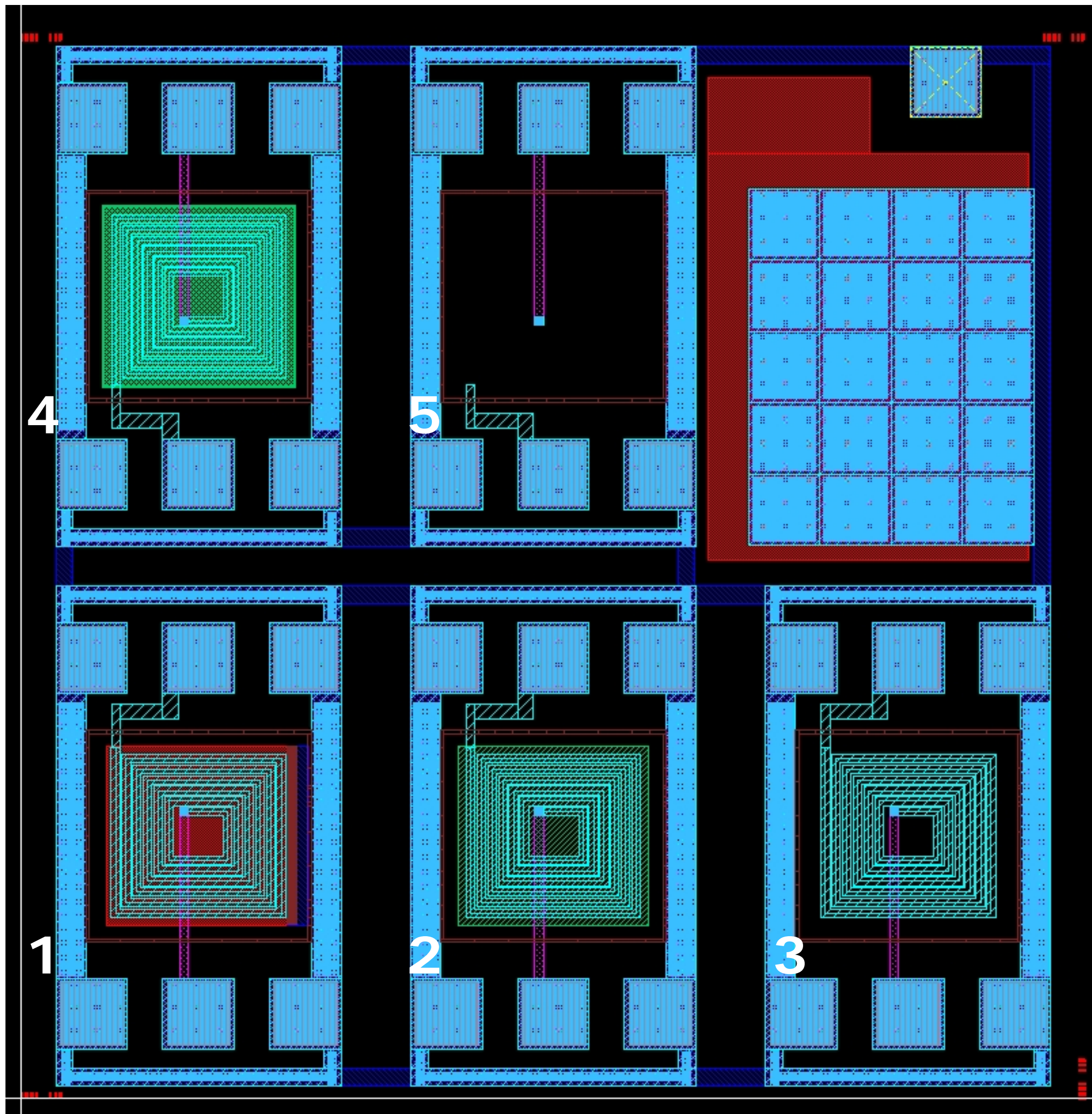
Values for Micro-Inductors Extracted.

Resonances observed depend on geometry.

Intrinsic capacitance and substrate losses determine behavior variations.

Inductors are typical for those found on IC's and show resonance at 4 to 10 GHz.

Test Chip: Investigating Micro Inductors
Effect of Silicon Substrate Doping



Designed for RF-probe station measurements

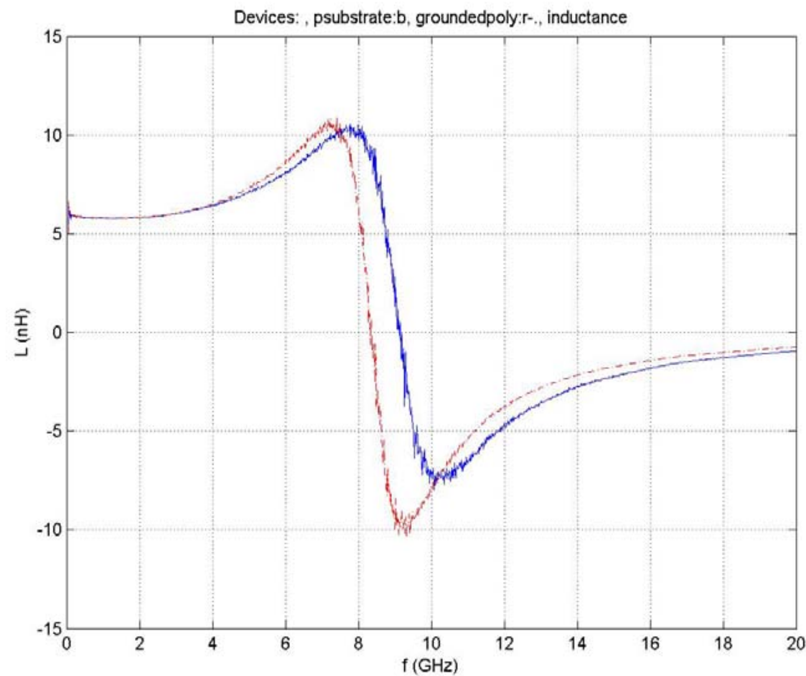
Manufactured through MOSIS

AMIS 0.5 µm; 3 Metal layers

Structures on chip 1:

1. Planar inductor on grounded poly
2. Planar inductor on n-well
3. Planar inductor on p-substrate
4. Planar inductor on n-plus
5. De-embedding structure: Open

Test Chip: Investigating Micro Inductors
Effect of Silicon Substrate Doping



Measurements show resonance for much higher doped substrate occurs at lower frequency.

Indicates higher intrinsic capacitance for more highly doped system.

Future Work

- Continue modeling of oxide breakdown in nanoscale MOSFETs.
- Extend MOSFET oxide breakdown modeling to transient case.
- Continue modeling of on-chip interconnects using ADI code.
- Investigate effect of doping and geometry on how bus lines couple to external EM.
- Continue experiments and modeling on on-chip passive elements.
- Extend theory for calculating inductance to include intrinsic capacitance effects as well.

Publications

- C.K. Huang and N. Goldsman, Non-equilibrium modeling of tunneling gate currents in nanoscale MOSFETs, *Solid State Electronics*, vol. 47: pp. 713-720, 2003.
- A. Akturk, N. Goldsman and G. Metze, ``Faster CMOS Inverter Switching Obtained withChannel Engineered Asymmetrical Halo Implanted MOSFETs, *Solid State Electronics,* vol. 47, pp.~185--192, 2003.
- X. Shao, N. Goldsman, O. M. Ramahi, P. N. Guzdar, A New Method for Simulation of On-Chip Interconnects and Substrate Currents with 3D Alternating-Direction-Implicit (ADI) Maxwell Equation Solver. *International Conference on Simulation of Semiconductor Processes and Devices,* pp. 315-318, 2003.
- X. Shao, N. Goldsman, and O. M Ramahi, The Alternating-Direction Implicit Finite-Difference Time-Domain (ADI-FDTD) Method and its Application to Simulation of Scattering from Highly Conductive Material, *IEEE International Antennas and Propagation Symposium and USNC/CNC/URSI North American Radio Science Meeting: URSI, Digest*, p. 358, 2003.
- Y. Bai, Z. Dilli, N. Goldsman and G. Metze, Frequency-Dependent Modeling of On-Chip Inductors on Lossy Substrate, *International Semiconductor Device Research Symposium,* pp. 292-293, 2003.
- 6. X. Shao, N. Goldsman, O. M. Ramahi,and P. N. Guzdar, Modeling RF Effects in Integrated Circuits with a New 3D Alternating-Direction-Implicit Maxwell Equation Solver, *International Semiconductor Device Research Symposium,* pp. 532-533, 2003.