Studies of Upset and Nonlinear Effects in Circuits and Systems

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Goals of Microwave Effects Task

- Not another “cookbook” approach
- Investigate basic high-frequency electronics
- Measure the (out-of-band) frequency response of fundamental devices excited by microwave pulses
- Map transfer characteristics of circuits
- Develop simple but comprehensive models for simulations
- Understand how RF response scales with device size, speed, logic levels and operating voltages.
Outline

• Overview of nonlinear circuit elements and their microwave characteristics

• Examples of experimental results:
  – Parasitic resonances in integrated circuits
  – Simple rectification by electrostatic discharge (ESD) protection
  – Bias shift, RF gain, and instability in devices
  – Effects from RF sources with wideband modulation
  – Chaotic circuit response

• Results from high-frequency SPICE Models

• RF Effects in systems
IC development and technological trends

Circuits under test at UMD

Number in Service

Examples of input circuitry in advanced logic

Virtually all chips have electrostatic discharge protection integrated into their physical layout.
Typical layout of a CMOS gate with electrostatic discharge (ESD) protection

Capacitive loading is predominately from ESD
Schematic of a CMOS data line

Typical LC values in advanced CMOS have GHz resonant frequencies
Analysis of simplified CMOS input (series RLD circuit) with equivalent diode model

\[ A_V = \frac{V_d}{V_{in}} = \frac{1 + sC_jR_S}{1 + s^2L_P C_j + sC_jR_S} \]

\[ A_V(\omega_R) = 1 - j\sqrt{L_P / C_j(V_D) / R_S} \]

\[ Q = \sqrt{L_P / C_j(V_D) / R_S} \]

Typical values:
- \( C_{j0} \approx 3 \text{ pF} \)
- \( L_P \approx 10 \text{ nH} \)
- \( R_V \approx 1 \text{ M\text{	extgreek{\textalpha}}\text{\textgreek{\textalpha}}} \)
- \( R_S \approx 10 \text{ \textgreek{\textalpha}} \)

Give:
- \( 0.5 < f_R < 3 \text{ GHz} \)
- \( 2 < Q < 6 \)
- \( 1.5 < |A_V| < 6 \)
Calculated capacitance, impedance and voltage gain for simplified CMOS model

\[ C_{j0} = 3.6 \text{ pF}, \quad L_p = 16\text{nH}, \quad R_s = 15 \Omega \]
Measured input impedance (small signal) vs. frequency and bias voltage in typical micron-scale CMOS

- $C_j$, $f_r$, and $Q$ depend on bias voltage
- Logic voltages at input shift the microwave response
- How about rectified voltages?
Rectification of RF in Circuits w/ ESD Diodes and Parasitic Elements

Input I-V characteristic of CMOS w/ ESD diodes

$V_{\text{logic}}$ steers RF current which determines circuit impedance and response
Realistic “digital” waveforms have high probability of being near the threshold voltage where RF susceptibility is high.

Also, the high-frequency response ($f_r$, and $Q$) in devices is a moving target.
The diode detects the AM (pulse) frequencies on the RF carrier and generates harmonics of the excitation signal.

Detected voltage (small-signal) at baseband: \( v_{\text{det}} \propto v_{RF}^2 G' \)

RF-to-Baseband voltage transfer related to diode parameters.

The signal the CMOS sees occupies two distinct frequency bands.
Effects due to Rectification of RF pulse by ESD diodes

Prompt Bit Error

Oscillations

Undefined Voltages & Latent Latch

More Oscillations
Example of CMOS family (LVX) that is latched by RF only when input is biased high
Contours of measured large-signal response in advanced CMOS

HCT

ALVC
RF pulse biasing both CMOS transistors into conduction where they amplify high-frequencies.
Nonlinear response in circuits generates harmonics of the RF and modulation signals which can excite high and low-frequency oscillations in the circuit.
CMOS RF→RF transfer characteristics

Measurements

Simulation Results

Video Clip

Video Clip
How to hit a moving target

Hughes 8537H TWTA
Variable Atten.
Delay Line

Attenuator
Bias Tee
DUT= ALVC

Spectrum Analyzer
RF Detector
Scope

<table>
<thead>
<tr>
<th>Time [us]</th>
<th>RF Amplitude</th>
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<tbody>
<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>0.05</td>
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<td>2</td>
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<tr>
<td>3</td>
<td>0.2</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
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</table>

<table>
<thead>
<tr>
<th>Frequency [GHz]</th>
<th>Spectral Power [dBm]</th>
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</thead>
<tbody>
<tr>
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<td>-75</td>
</tr>
<tr>
<td>1</td>
<td>-65</td>
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<tr>
<td>2</td>
<td>-55</td>
</tr>
<tr>
<td>3</td>
<td>-45</td>
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<tr>
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<tr>
<td>5</td>
<td>-25</td>
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<tr>
<td>6</td>
<td>-15</td>
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</table>

<table>
<thead>
<tr>
<th>Frequency [GHz]</th>
<th>A(t-tau/4)</th>
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<td>3</td>
<td>-0.1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
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</table>
Response of Advanced Low-Voltage CMOS to wideband RF source (RF amplitude = 450 mV)
Chaos in the Driven RLD Circuit

Voltage across Resistor $R \sim I$

Maximum Voltage across Resistor $R$

Driving Amplitude $V_0$ (V)

Bifurcation diagram

$R = 25 \ \Omega$
$L = 50 \ \mu H$
$D = \text{NTE610}$
$f = 2.5 \ \text{MHz}$

$V_0 \sin(\omega t)$
$f = 2.5 \ \text{MHz}$
## Search for Period Doubling and Chaos in Driven RLD Circuit

<table>
<thead>
<tr>
<th>Diode</th>
<th>$\tau_{RR}$ (ns)</th>
<th>$C_j$ (pF)</th>
<th>Results with $f_0 \sim 1/\tau_{RR}$</th>
<th>Results with $f_0 \sim 10/\tau_{RR}$</th>
<th>Results with $f_0 \sim 100/\tau_{RR}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1N5400</td>
<td>7000</td>
<td>81</td>
<td><strong>Period-doubling and chaos for</strong> $f/f_0 \sim 0.11 – 1.64$</td>
<td><strong>Period-doubling and chaos for</strong> $f/f_0 \sim 0.16 – 1.76$</td>
<td><strong>No chaos, nor period-doubling</strong></td>
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<td>1N4007</td>
<td>700</td>
<td>19</td>
<td><strong>Period-doubling and chaos for</strong> $f/f_0 \sim 0.13 – 2$</td>
<td><strong>Period-doubling and chaos for</strong> $f/f_0 \sim 0.23 – 1.3$</td>
<td><strong>No period doubling or chaos</strong></td>
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<tr>
<td>1N5475B</td>
<td>160</td>
<td>82</td>
<td><strong>Period-doubling and chaos for</strong> $f/f_0 \sim 0.66 – 2.2$</td>
<td><strong>No chaos, nor period-doubling</strong></td>
<td><strong>No chaos, nor period-doubling</strong></td>
</tr>
<tr>
<td>NTE610</td>
<td>45</td>
<td>16</td>
<td><strong>Period-doubling and chaos for</strong> $f/f_0 \sim 0.14 – 3.84$</td>
<td><strong>Period-doubling only for</strong> $f/f_0 \sim 1.17 – 3.25$</td>
<td><strong>No chaos, nor period-doubling</strong></td>
</tr>
</tbody>
</table>

\[ f_0 = \frac{1}{2\pi \sqrt{LC_j}} \]
Chaos in the Driven Diode Distributed Circuit

A simple model of p/n junctions in computers

Delay differential equations for the diode voltage

1) \[ 2V_{inc}(t) = V(t) + Z_0[gV + \frac{d}{dt}Q(V(t))] \]

2) \[ V_{ref} = V(t) - V_{inc}(t) \]

3) \[ V_{inc}(t) = V_{ref}(t-2T) + V_g(t-T) \]

\[
\frac{d}{dt}V(t) = \frac{-(1 + Z_0g)}{Z_0C(V(t))}V(t) + \frac{\rho_g(1-Z_0g)}{Z_0C(V(t))}V(t-2T) + \frac{-\rho_gC(V(t))}{C(V(t-2T))} \frac{d}{dt}V(t-2T) + \frac{V_g\tau_g}{Z_0C(V(t))}\cos(\omega(t-T))
\]
Chaos in the Driven Diode Distributed Circuit

Simulation results

\[ V_g = 0.5 \text{ V} \quad \text{Period 1} \]

\[ V_g = 2.25 \text{ V} \quad \text{Period 2} \]

\[ V_g = 3.5 \text{ V} \quad \text{Period 4} \]

\[ V_g = 5.25 \text{ V} \quad \text{Chaos} \]

\[ f = 700 \text{ MHz} \]
\[ T = 87.5 \text{ ps} \]
\[ R_g = 1 \Omega \]
\[ Z_0 = 70 \Omega \]
\[ \text{PLC, } C_r = C_f/1000 \]
Chaos in the Driven Diode Distributed Circuit

Simulation results

- Period 1
- Period 2
- Period 4
- Chaos

- $f = 700 \text{ MHz}$
- $T = 87.5 \text{ ps}$
- $R_g = 1 \Omega$
- $Z_0 = 70 \Omega$
- PLC, $C_r = C_f/1000$
RF effects modeling using SPICE

Includes:
- Package and bonding parasitics
- High frequency characteristics of power line and bypass capacitor
- ESD diodes: reverse recovery, $C_j(V)$, $R_s$ and charge conservation
Comparison of measured and simulated response in CMOS w/ ESD

Models can even predict relaxation oscillations:

[Video Clip]
RF Effects in communications and data systems

• Generalize approach for a wide variety of devices using scaling laws

• Study RF interactions between interconnected devices on transmission lines

• Develop systems-level response models

• Validate simulations with measurements
RF effects decease when devices are heavily loaded by low-impedance interconnects and line drivers.
Systems Example: Programmable LAN Switch

I/O
Logic
System Controller
CPU
Memory
Summary of Most Significant Results

- Identified the culprits: Nonlinear devices (e.g. ESD diodes) have been shown to be the likeliest cause of upset in circuits, µwave diode model works.
- Know their MO: i.e. how to measure & model the fundamental HF elements and construct equivalent circuits.
- Variety of effects (rectification, oscillation, RF gain and instability) in circuits have been characterized.
- Studied some important scaling laws: device size, speed, operating and logic voltages, package parasitics.
- Can predict RF effects: High-frequency SPICE models are fast, easy & work.
- Outline a systems-level approach: looks promising, significant progress made.

Note: Basis for intelligent design of HPM sources (frequency, bandwidth, modulation, pulse width, etc.)
Future Work

- Study emerging technologies (BiCMOS, LinBiCMOS, Low Voltage Differential, deep submicron).
- Further investigate nonlinear effects and excitation: RF pulses with complex (esp. chirp), chaotic and ultra-wideband modulation.
- Continue development of systems models which include:
  - Voltage-frequency response statistics,
  - RF gain, coupling and cascaded response in interconnected devices
  - Effects from time delay and reflections in transmission line-coupled devices.
- Couple transfer characteristics devices and circuits to cables and enclosures.
Collaborations

- Titan-Jaycor
- Institute for Defense Analysis
- NRL
- ARL
- Philips Semiconductor
- Future: Univ. New Mexico, AFRL, DIA