Schottky Diode RF Detectors and RF Pulse Effects on CMOS Logic

Boise State University and University of Maryland

Presented by

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Boise State

Participants:

U. Maryland: Woochul Jeon, John Melngailis
(with help from Andrei Stanishevsky, Nolan Ballew, and John Barry, and Michael Gaitan, NIST)

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Students supported over the last year at Boise State:
Curtis Cahoon, Kelly DeGregrio (both now with Micron), and Ben Rivera (now with Freedom IC)

Outline: ***(Schottky diodes)***

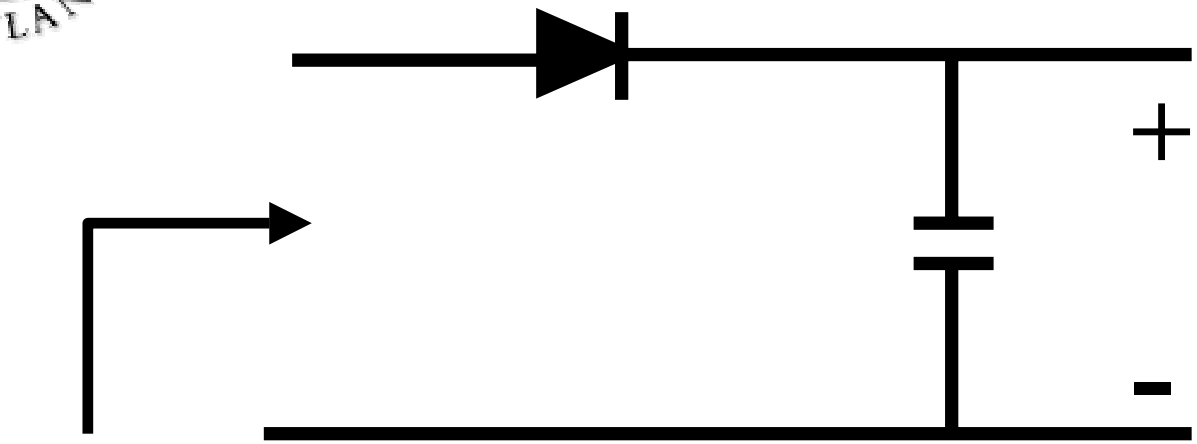
-- diodes fabricated and tested (DC and RF)

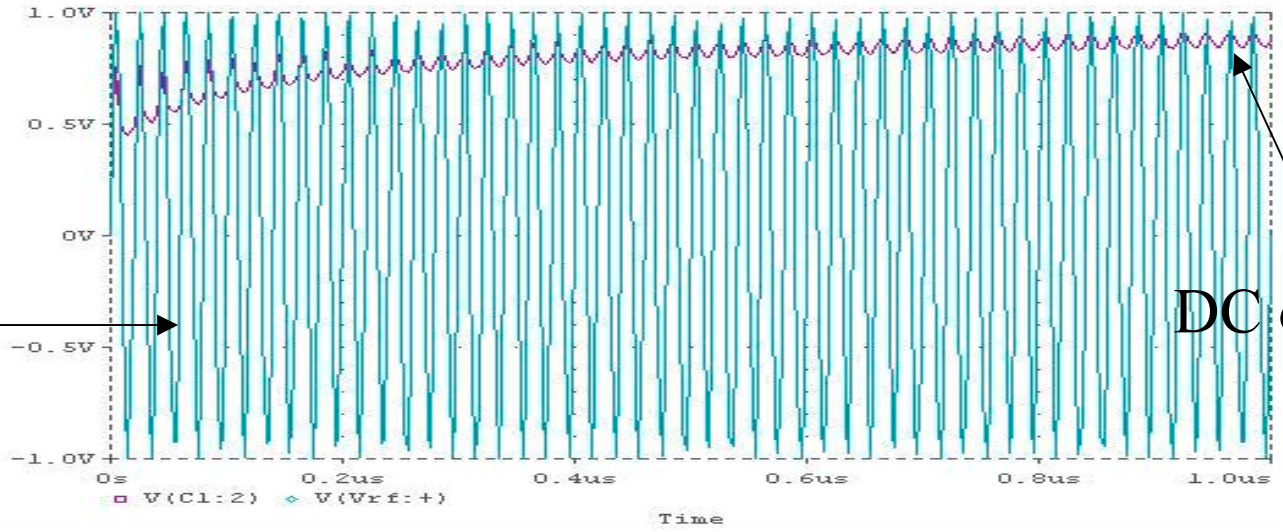
-- diodes for high freq. operation,
preliminary fab and test at DC,
RF structures designed

-- integrated circuits designed with diodes
connected to in-situ amplifiers

Operation of Power detector

(Simulated)





RF input

DC output

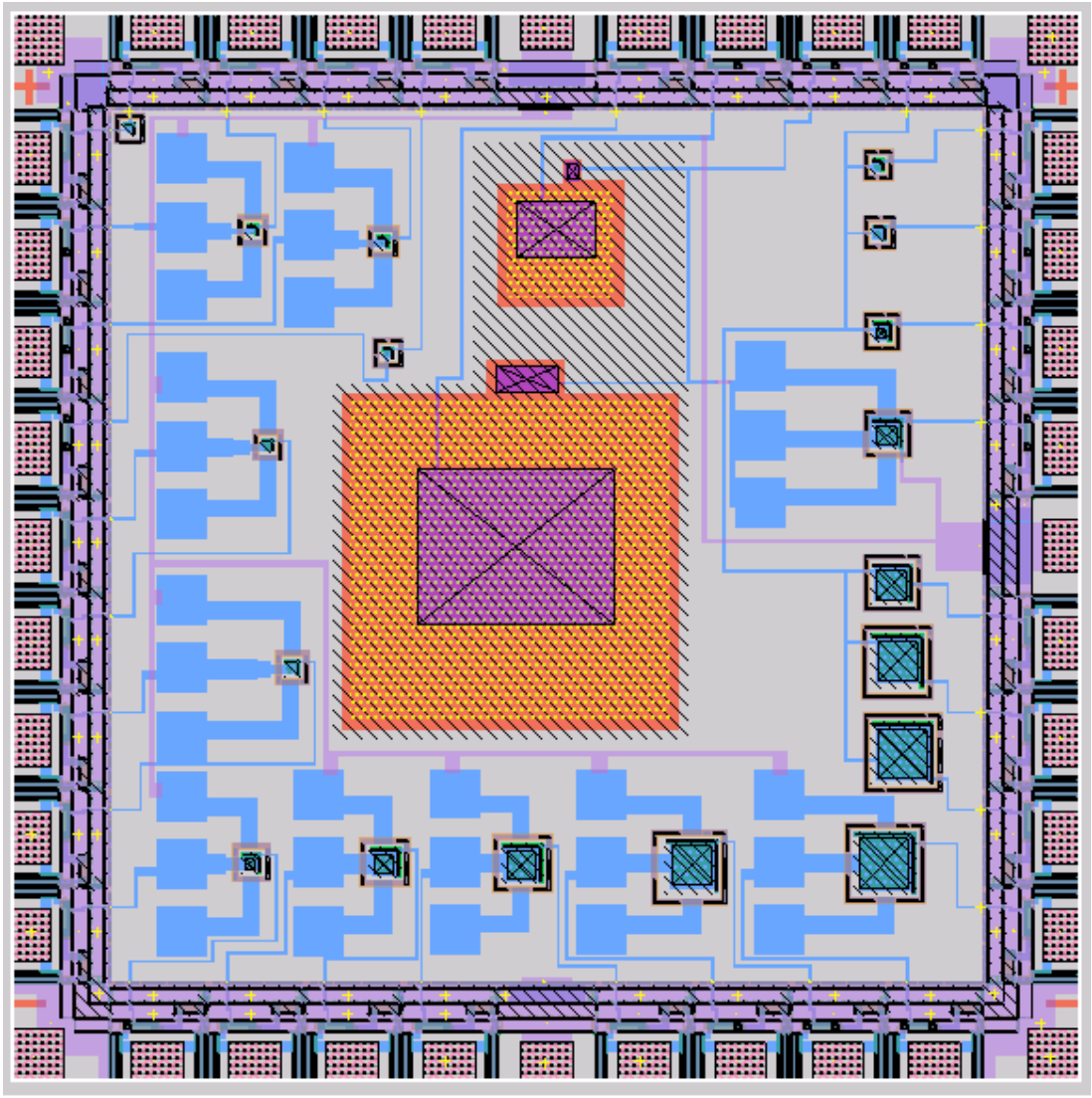
Chip Sumitted to MOSIS

2.2 x 2.2 mm

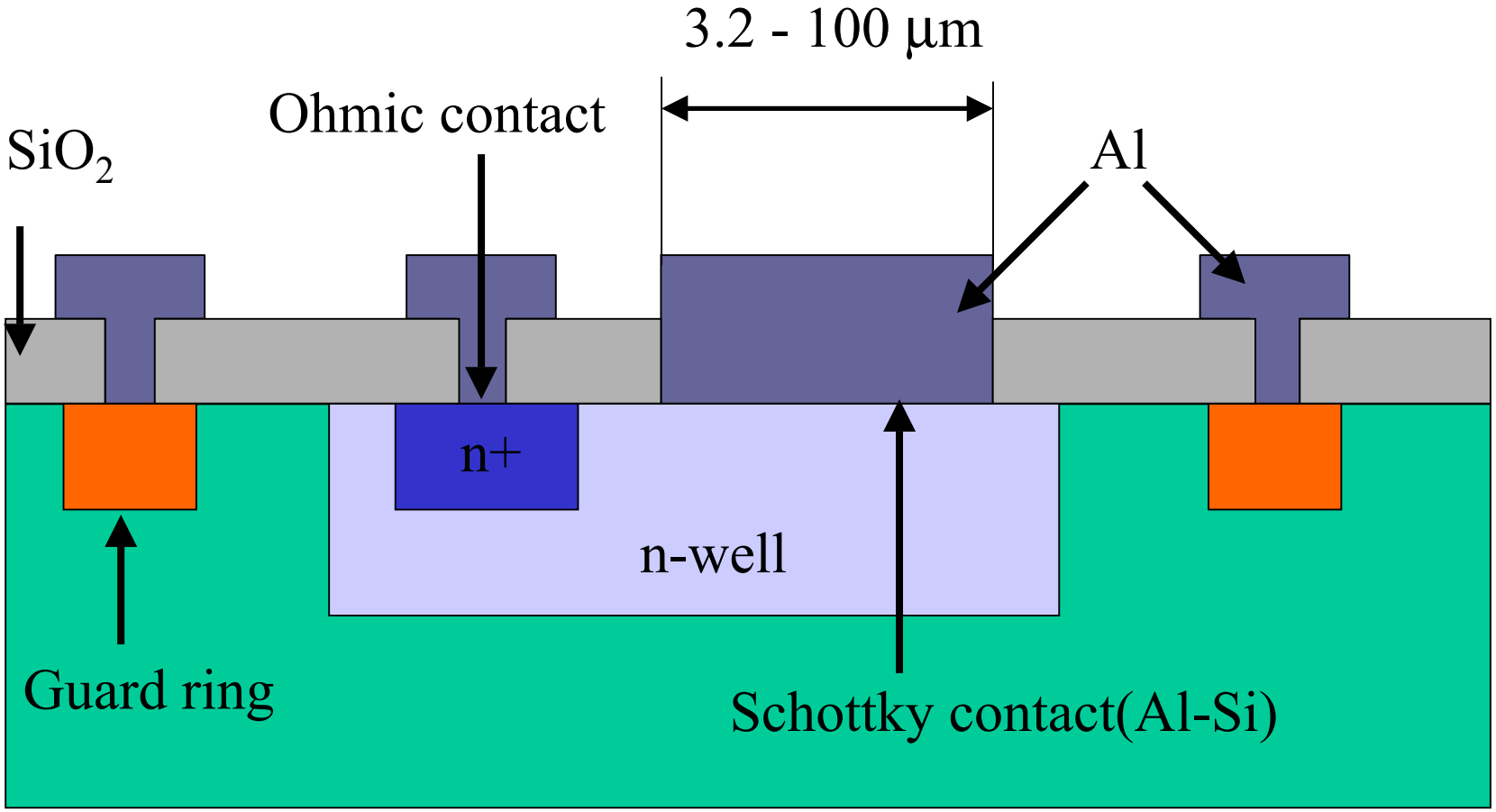
AMI 1.5μ process,

SCNA λ= 0.8

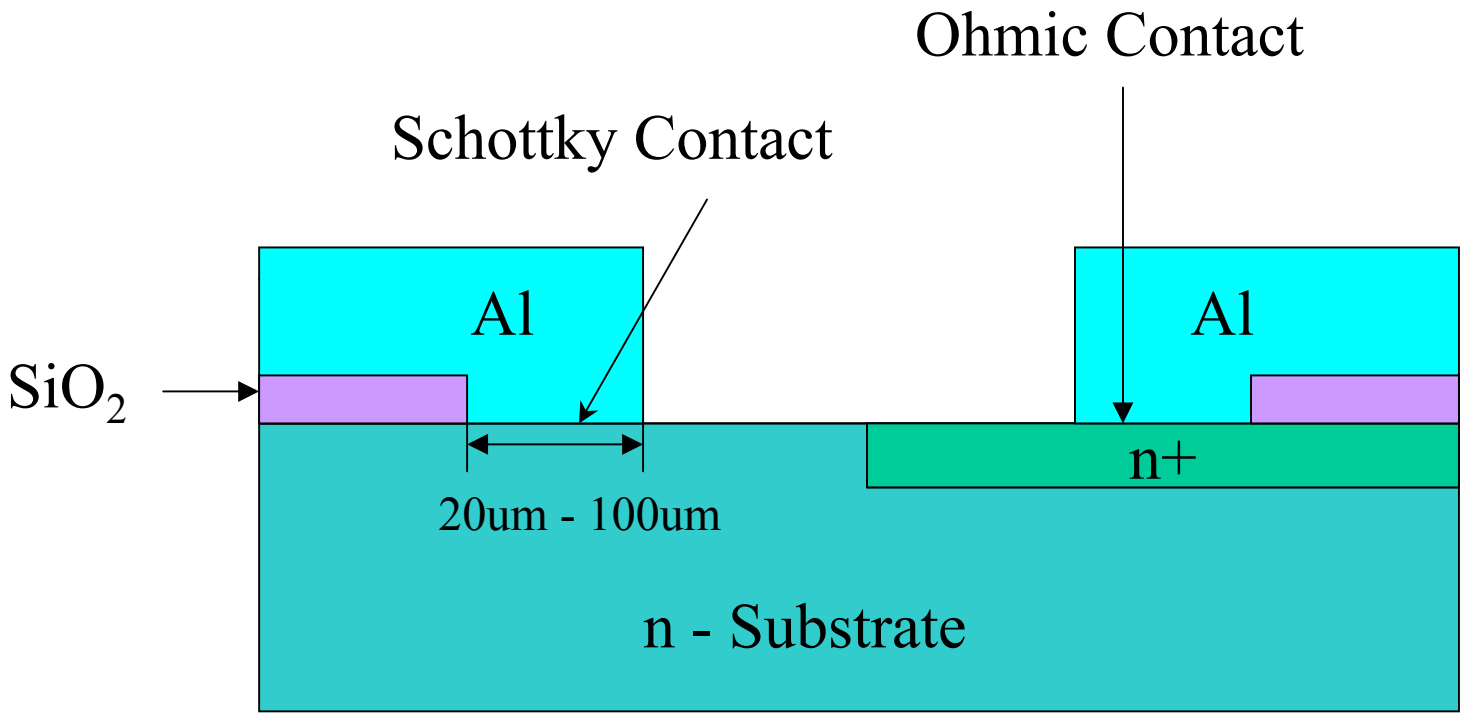
Diodes did not work!



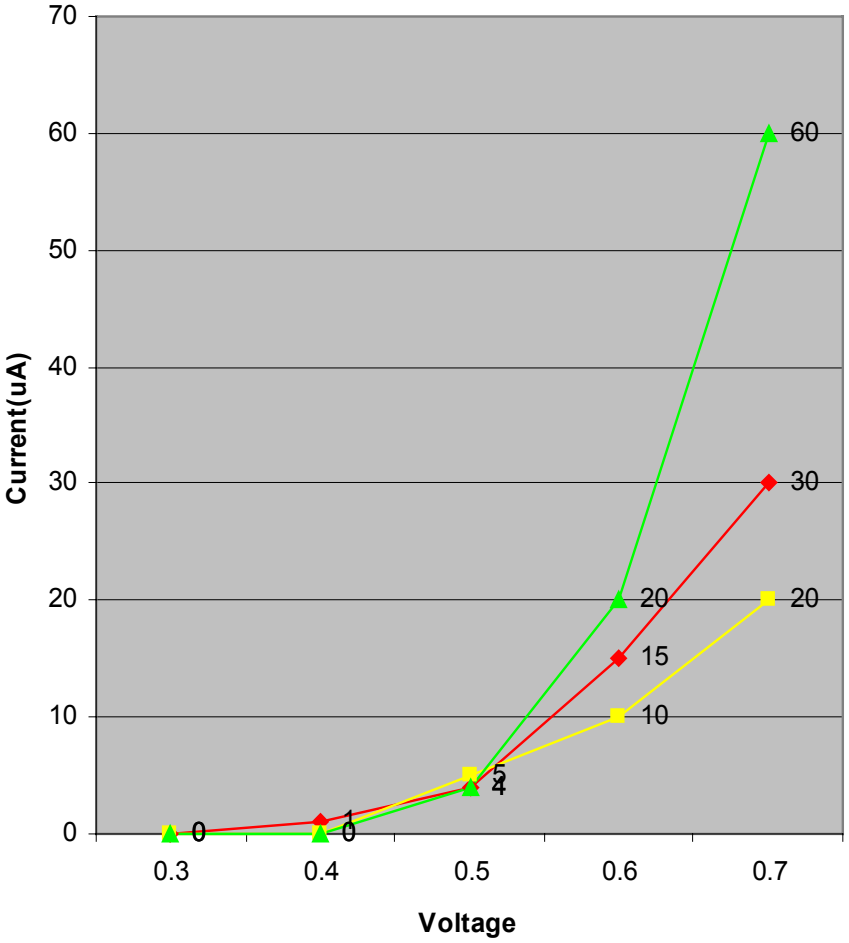
Cross section view

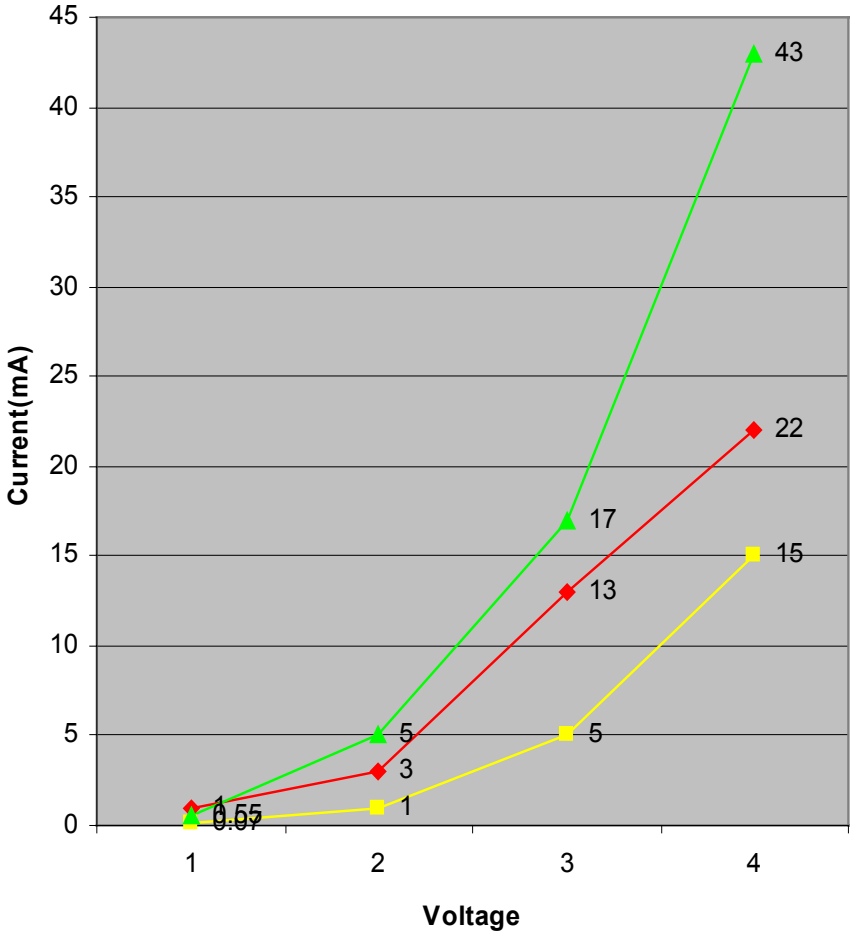


Cross section of Schottky diodes, fabricated with existing, crude mask and wafer



Measured I-V Characteristics 20x20um Schottky diodes.





Capacitance and Series resistance

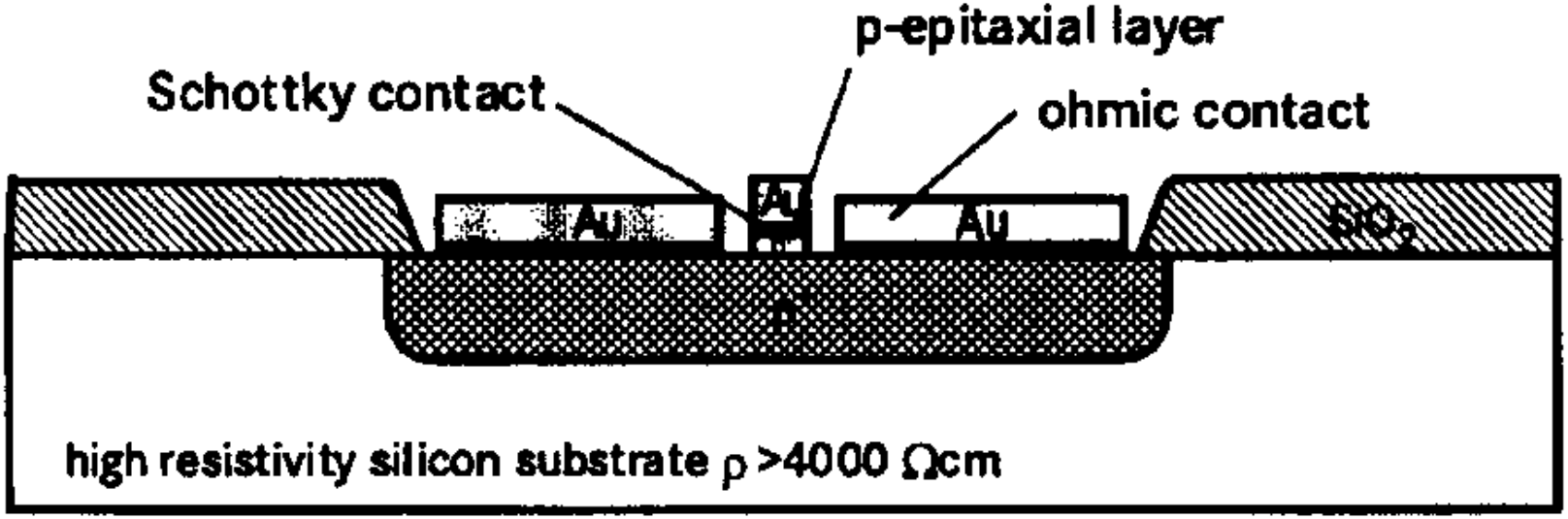
- $f_c = 1/(2\pi RC)$

➔ Make R and C as small as possible to increase cutoff frequency (f_c)

- $$Cj = A\sqrt{\frac{\varepsilon qNs}{2(V+Vd)}}$$ ➔ A: contact area, Ns: doping concentration
  V: applied voltage, Vd: built-in voltage

- Series resistance = $R_j + R_n + R_{n+}$
  - ➔ $R_n >> R_{n+} >> R_j$
  - ➔ Series resistance mainly determined by R_n(n layer resistance).
- Objective ➔ Reduce contact area(A) and resistance of R_n layer

Coplanar Schottky Diode Developed for Rectifying Antennas *Operated to 93GHz*



K.M. Strohm, J. Buecher, & E. Kasper ,

Daimler Benz Research, Ulm

IEEE Trasn. MTT Vol.46, 669, (May, 1998)

Developing High Frequency Schottky Diode Detector

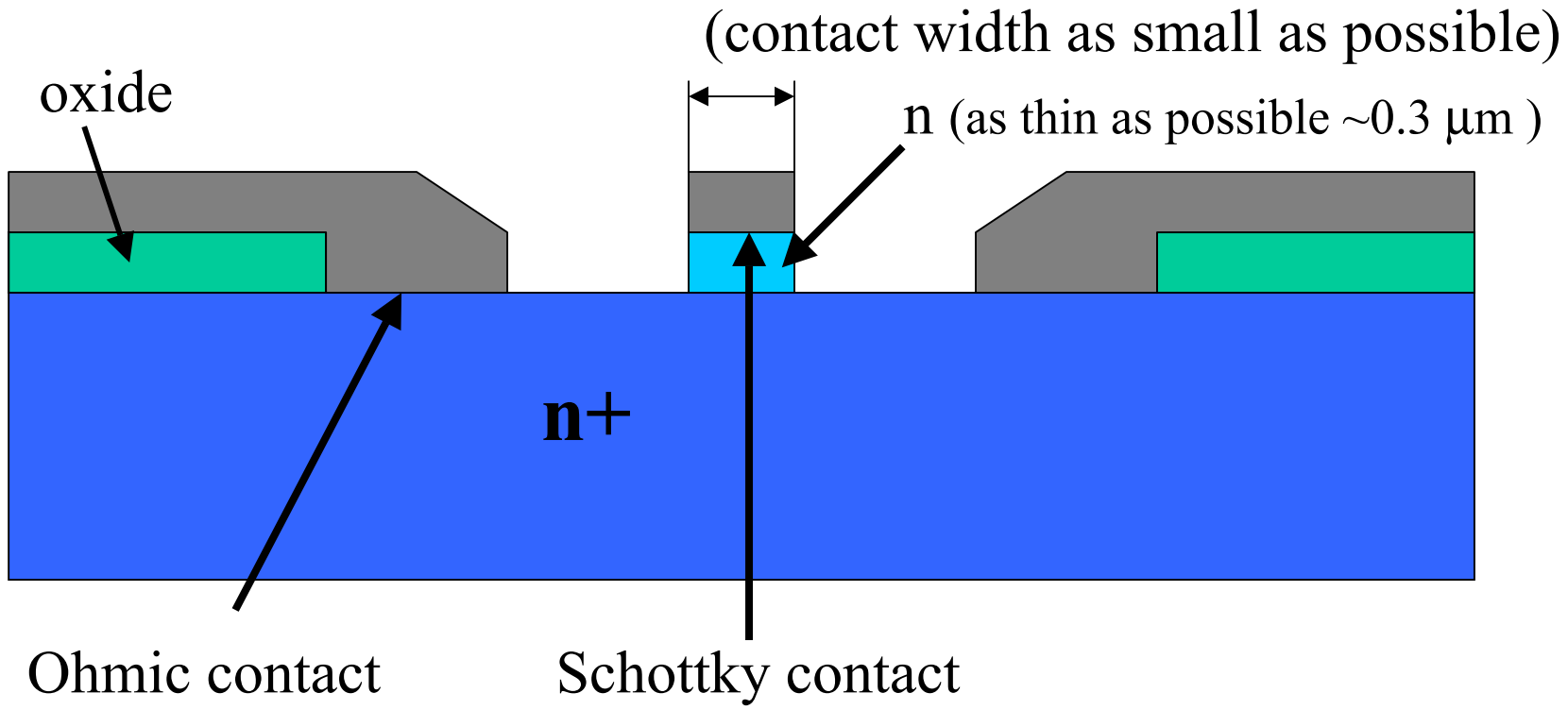
-- 93GHz detector (Daimler Benz) needs MBE growth over n+, not compatible with CMOS

-- use n on n+ wafers to test diode fabrication and RF pickup by various structures,

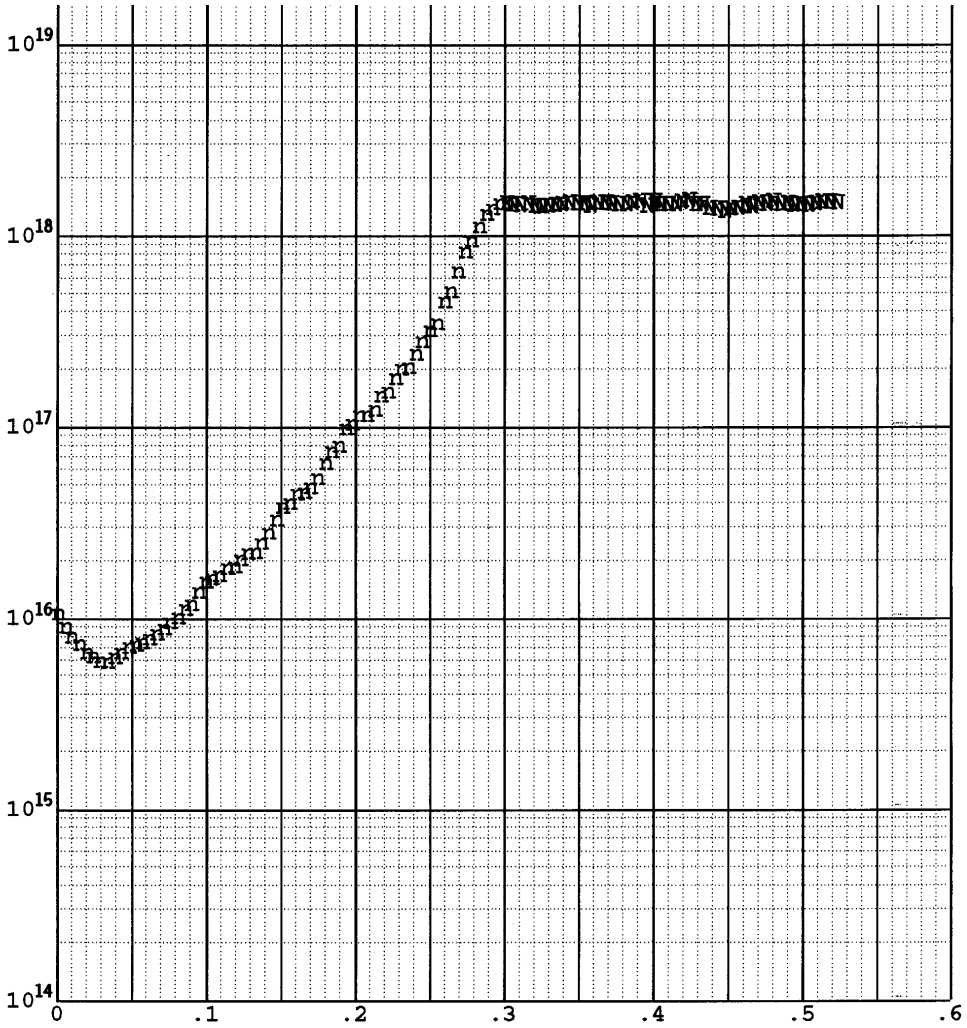
-- develop process for inserting n-on-n+ diodes in CMOS chips

Proposed structure

- Reduce series resistance => use n+ substrate
- Reduce contact capacitance => decrease contact area
- Additional Process: Si-MBE (n layer on n+)

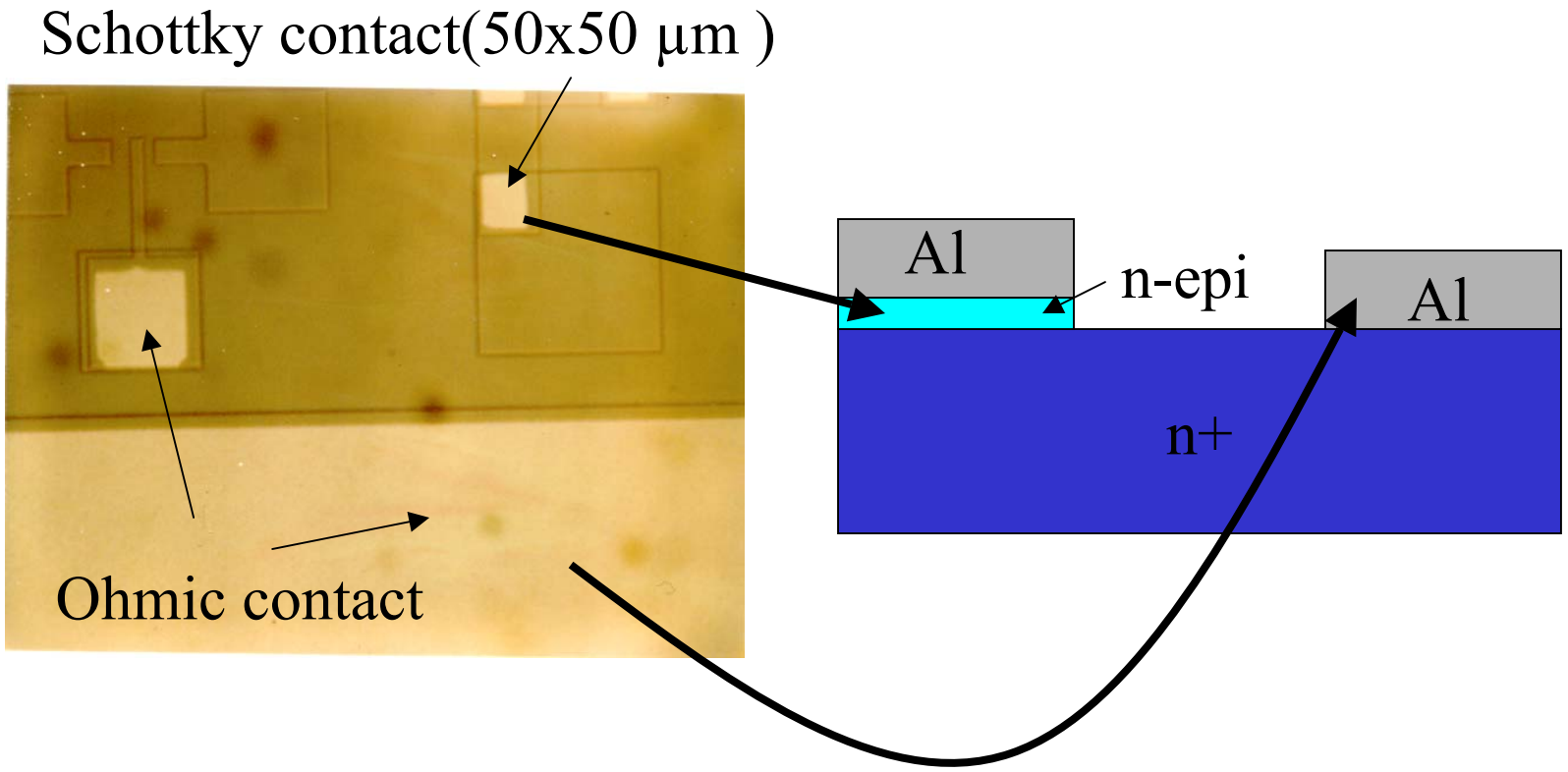


Analysis of n on n^+ Layer on Wafer

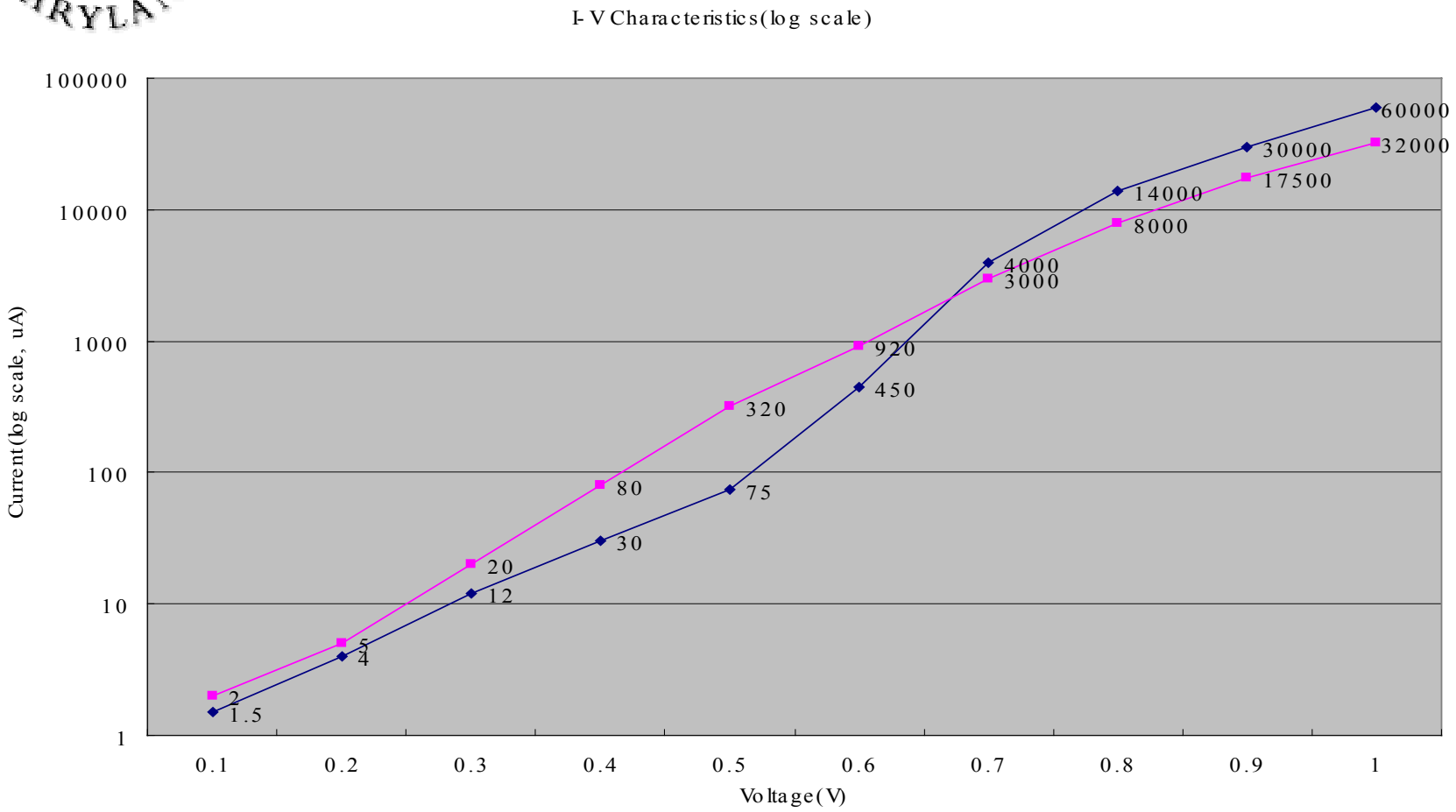


Test ability to make Schottky diode on n+ substrate

- To reduce series resistance n+ substrate with 0.3 μm n-epi layer is used



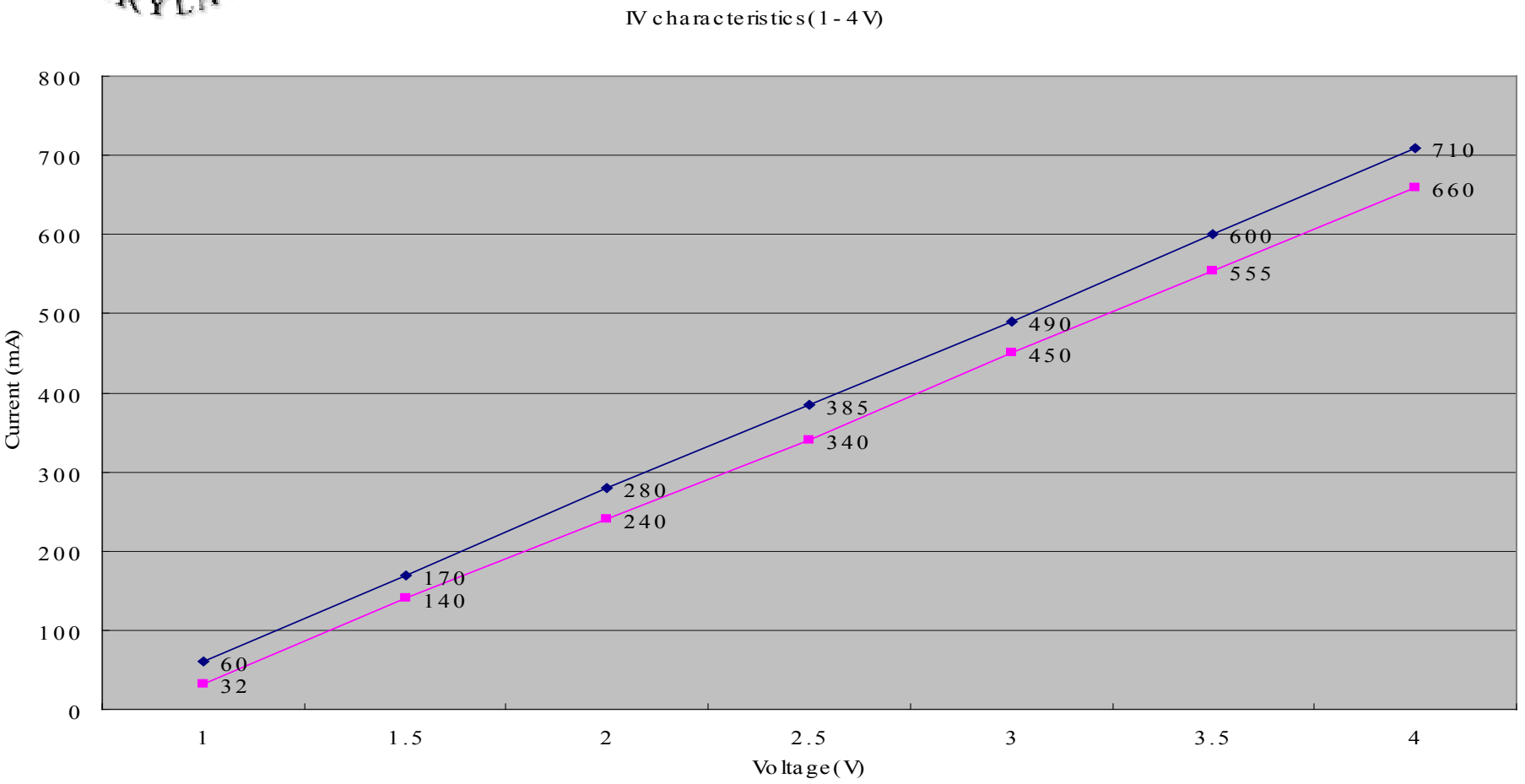
Measured result (0.1-1V)



➔ IV curve (input voltage(0.1-1V), output current(1.5 μA – 60mA)

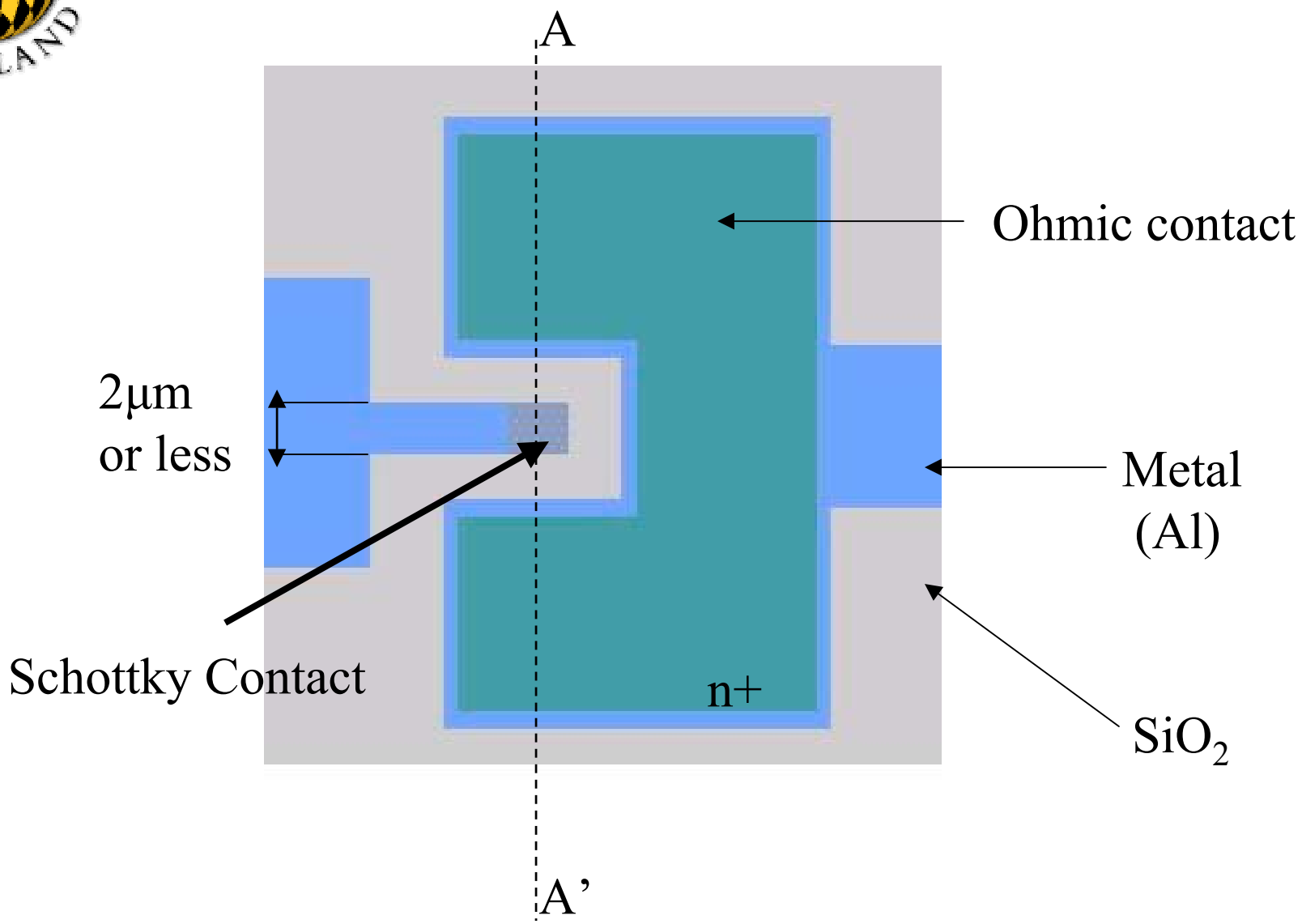
➔ Output current is in log scale (exponential response)

Measured result (1-4V)

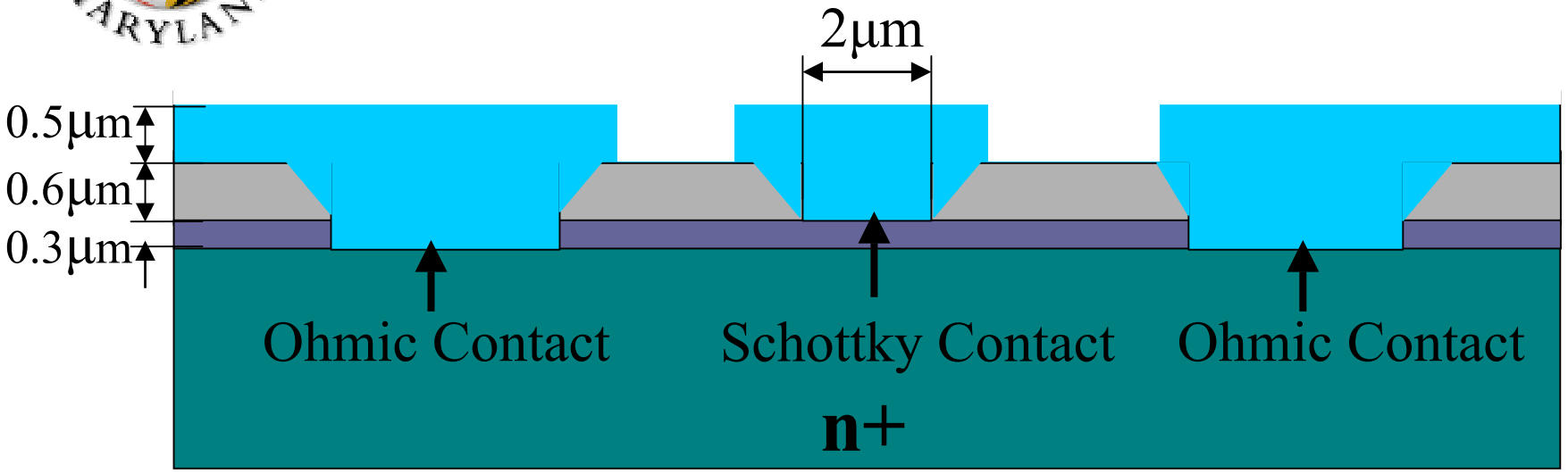


➔ Series resistance = 2V/430mA = 4.7 Ω

Schottky Diode Layout

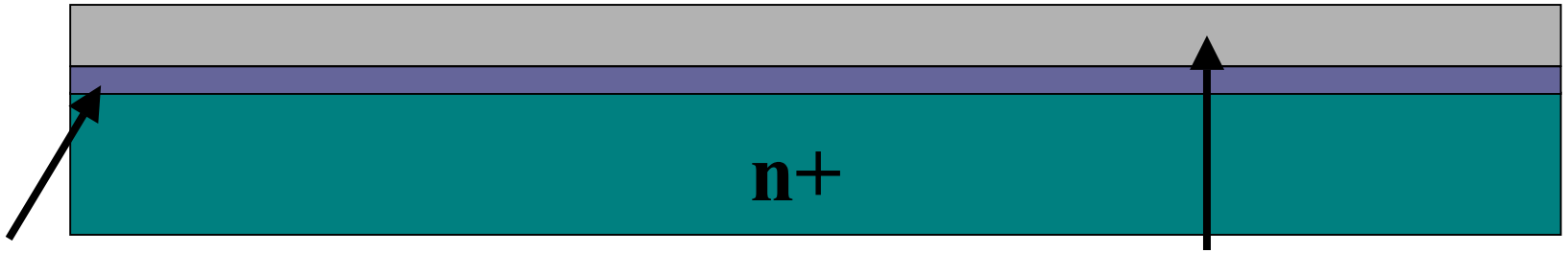


Cross section view of Schottky Diode (A-A')



Starting wafer

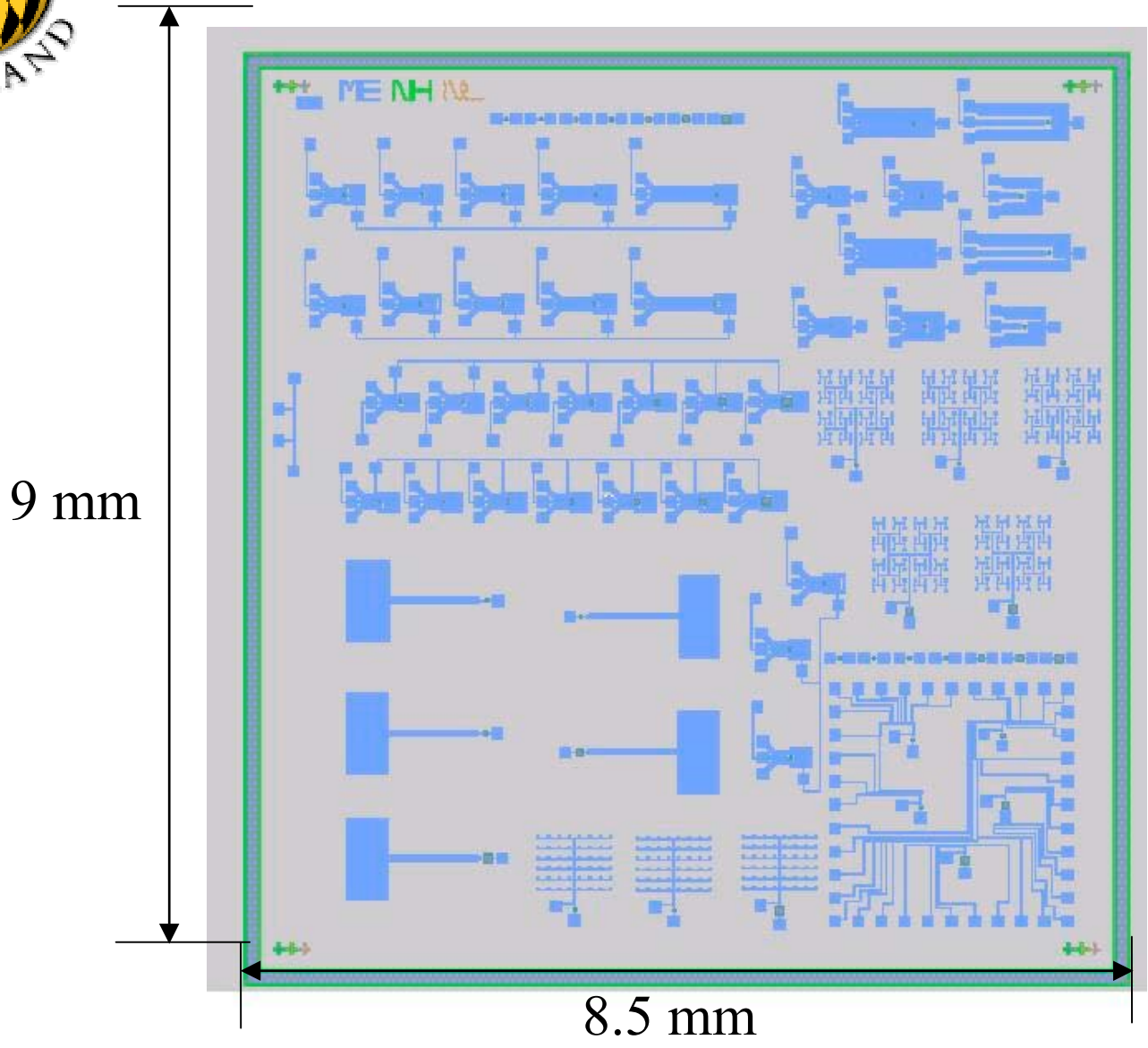
➔ (n+ substrate, 0.3μm lightly doped n layer, 0.6μm Oxide by LPCVD)



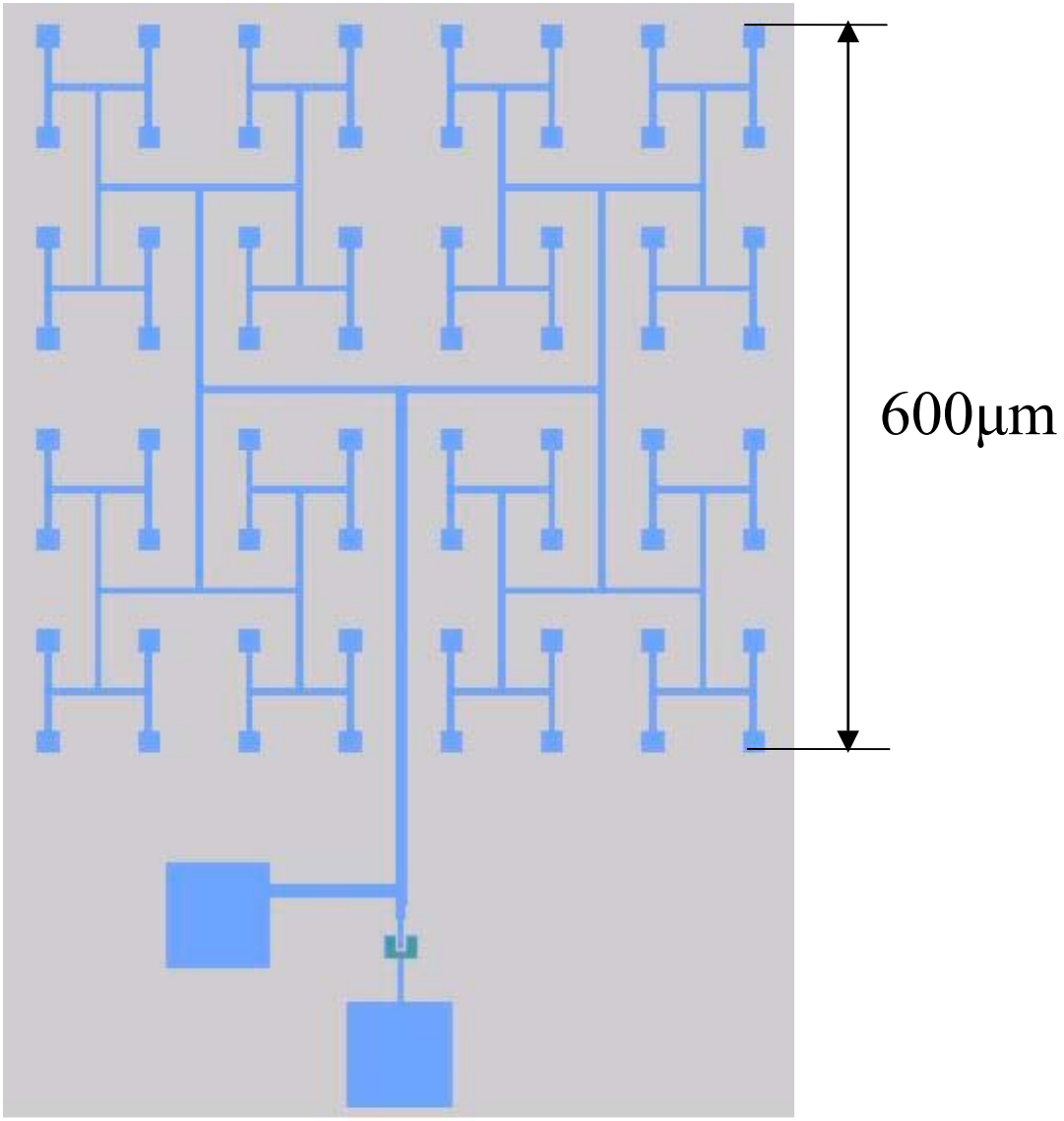
0.3μm n Si epi layer

0.6μm SiO2 layer

Mask Ordered from Berkeley Univ.



Schottky diode with clock tree



What we expect to learn:

-- frequency response of diodes tested by Cascade probes

-- frequency response tested by incident RF

-- RF pickup level of various structures on chip as a function of frequency

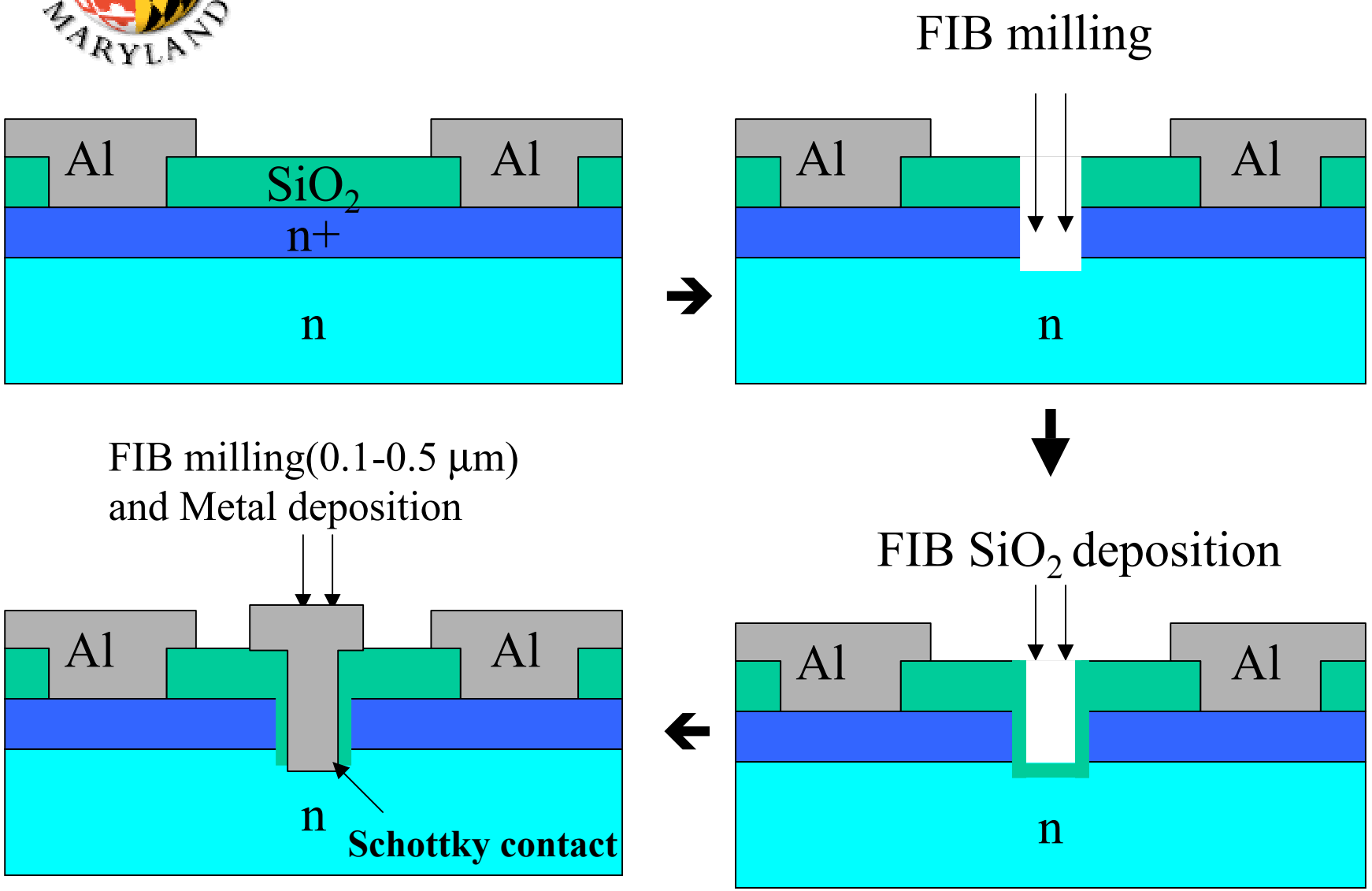
Ideal Diode Detector:

-- compatible with CMOS

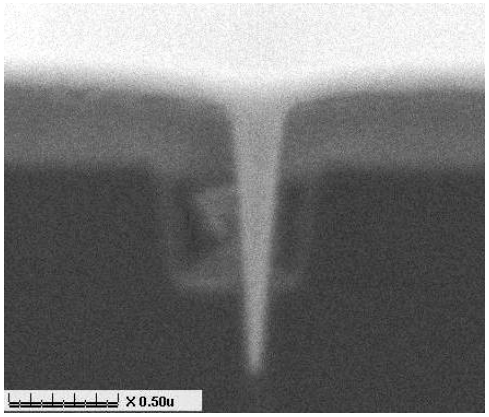
-- high frequency

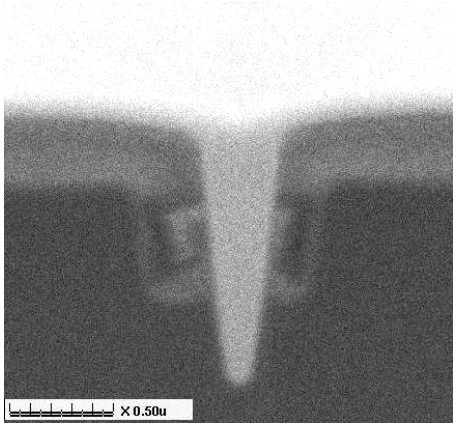
-- easy to fabricate

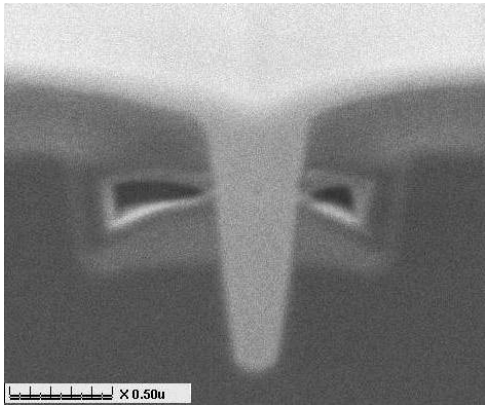
Fabricating Schottky diode by FIB



FIB Tungsten Vias
Through FIB Deposited Oxide Plugs

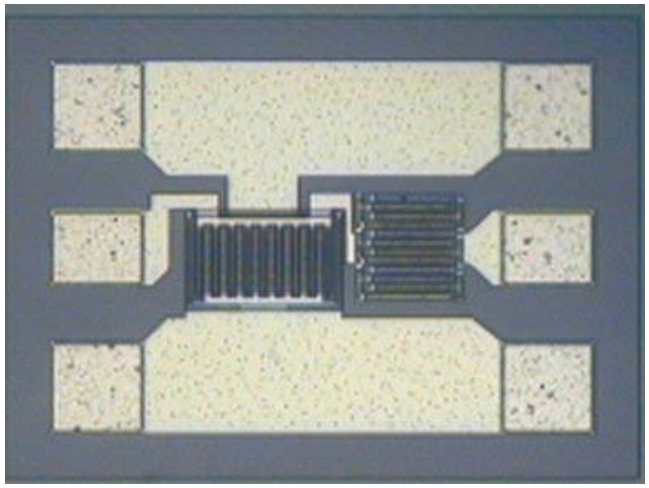


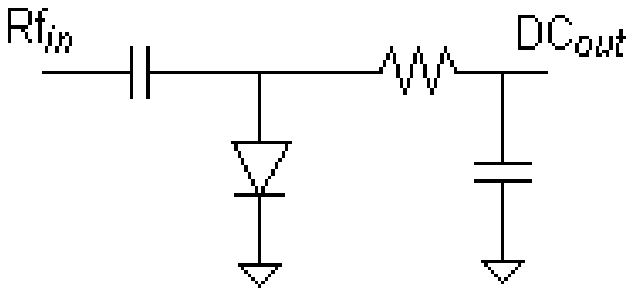




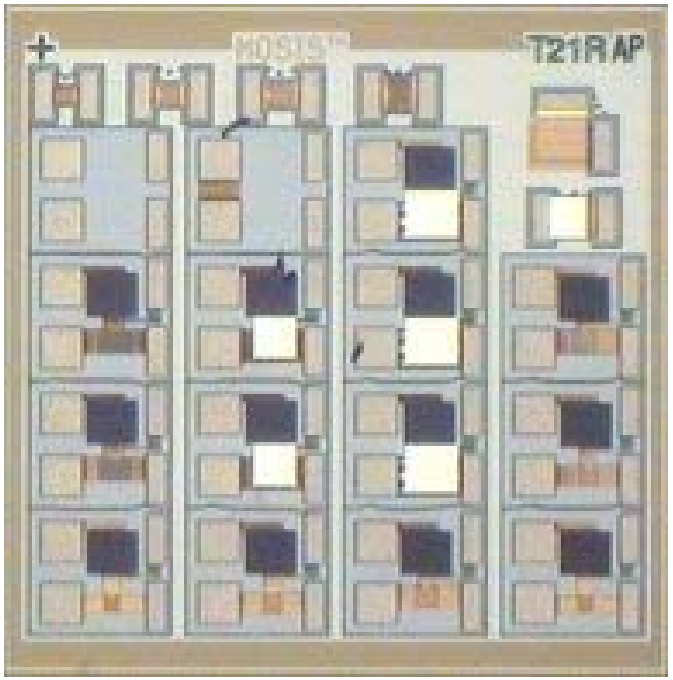
500nm

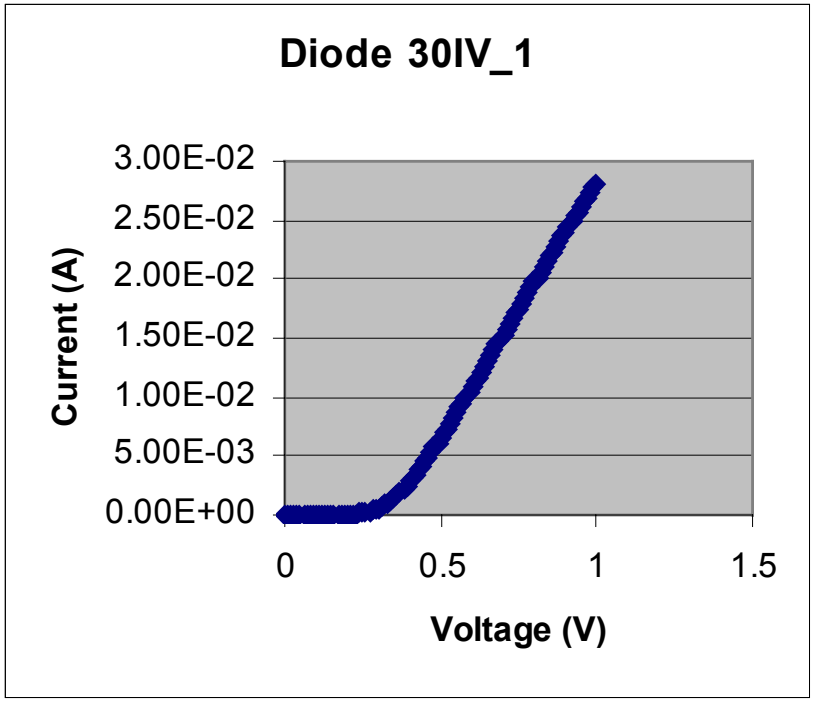
- Design of Schottky diodes, first-chip
- Picture shown for one of the test sites on the chip.



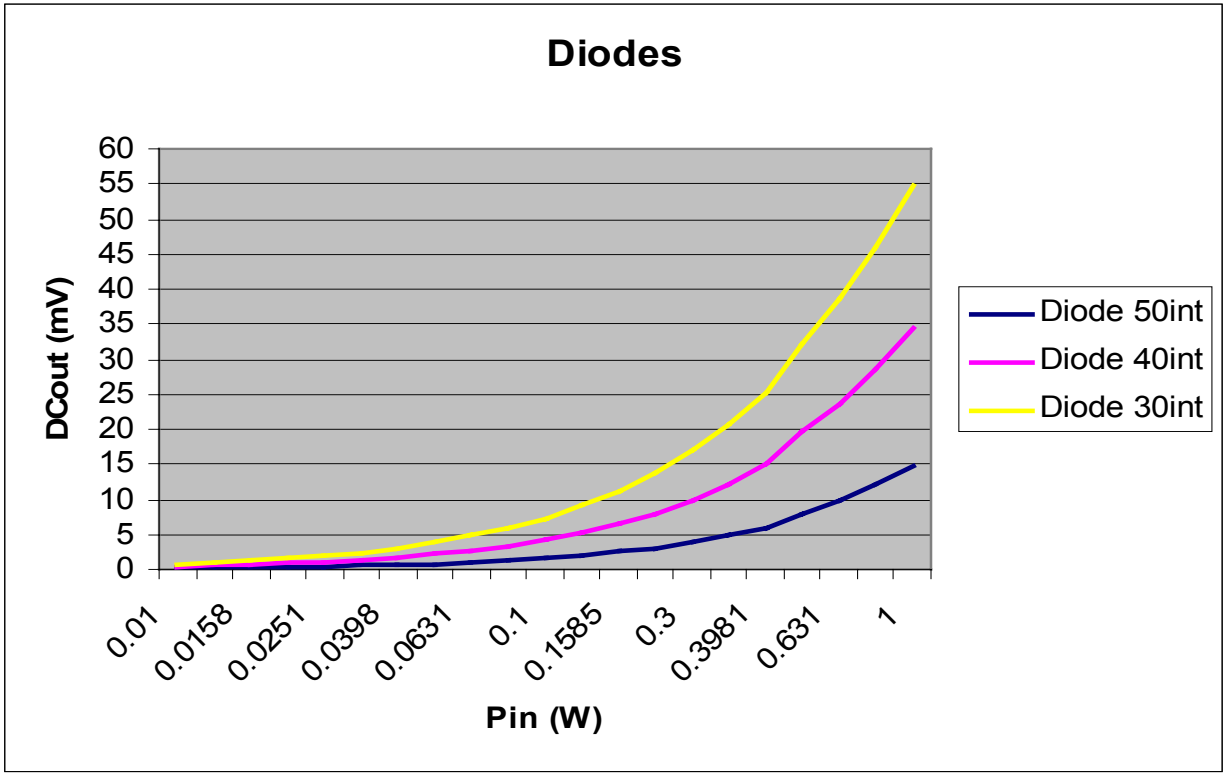


- **Had a spacing problem between the probe pads which affected the microwave measurements. Fixed the problem and re-fabricated.**

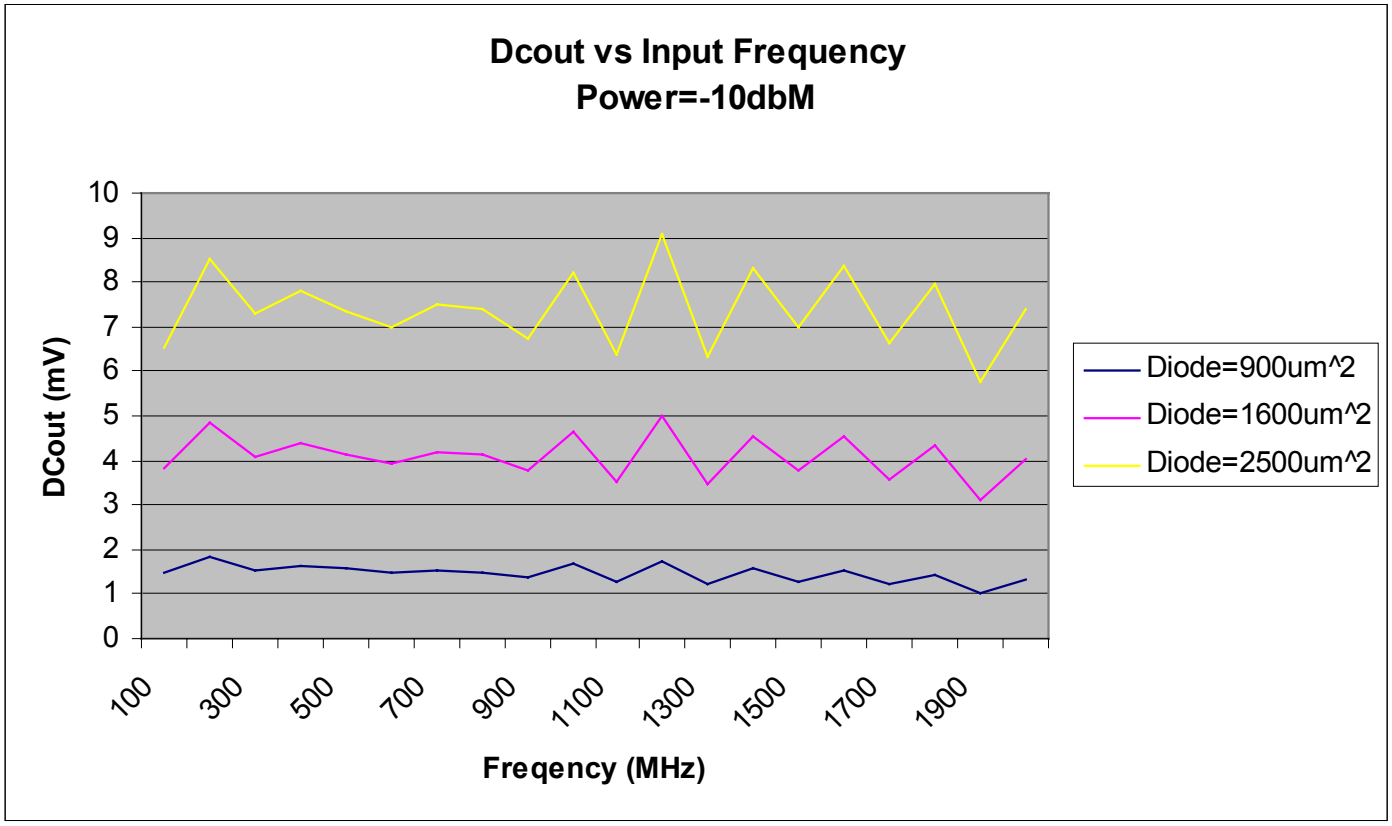




- Several different types of test structures
- Measured the DC voltage out as a function of microwave power applied to the test structure.

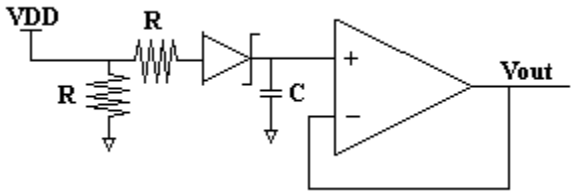


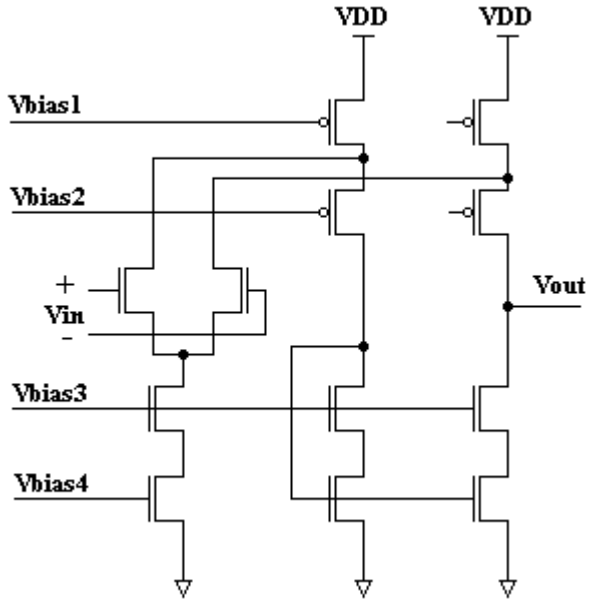
- We also looked at the frequency behavior of the circuit.



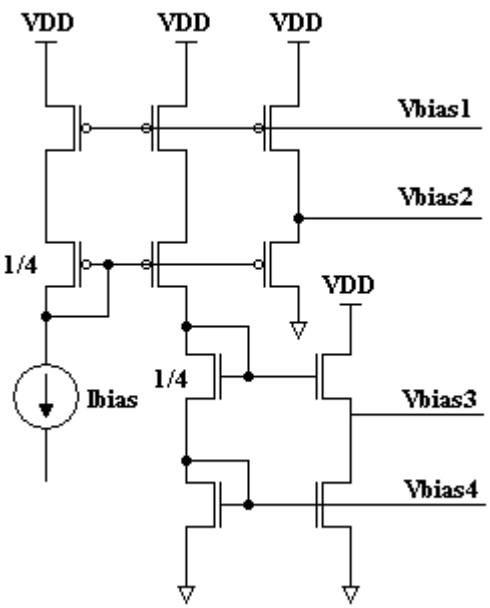
- We are now integrating the detectors with amplifiers for non-invasive on-chip measurements.

Basic concept

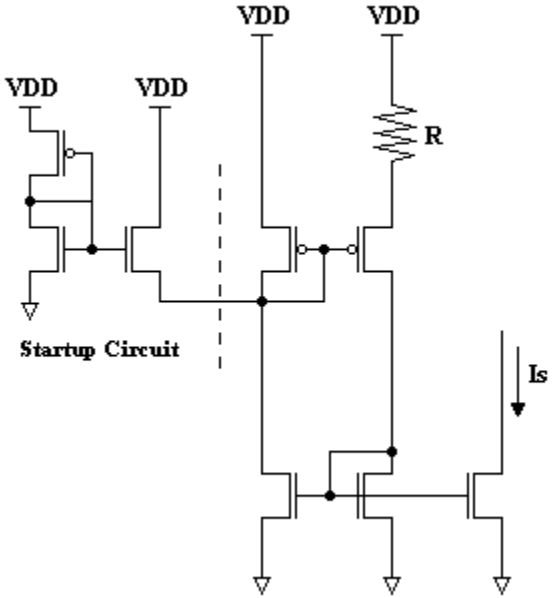




Amplifier schematic

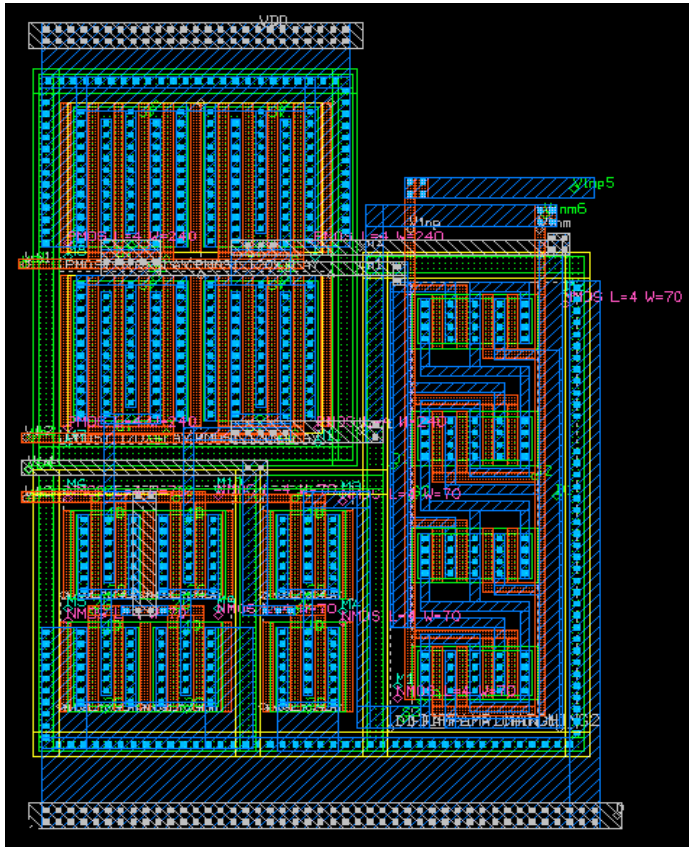


Bias circuit schematic

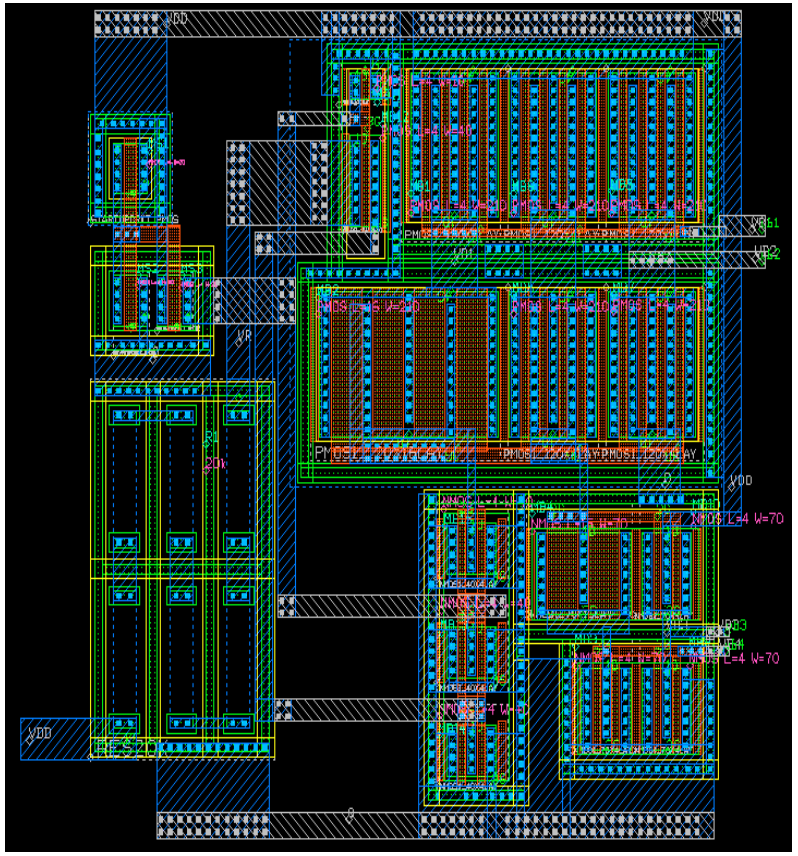


Reference

- Layout views

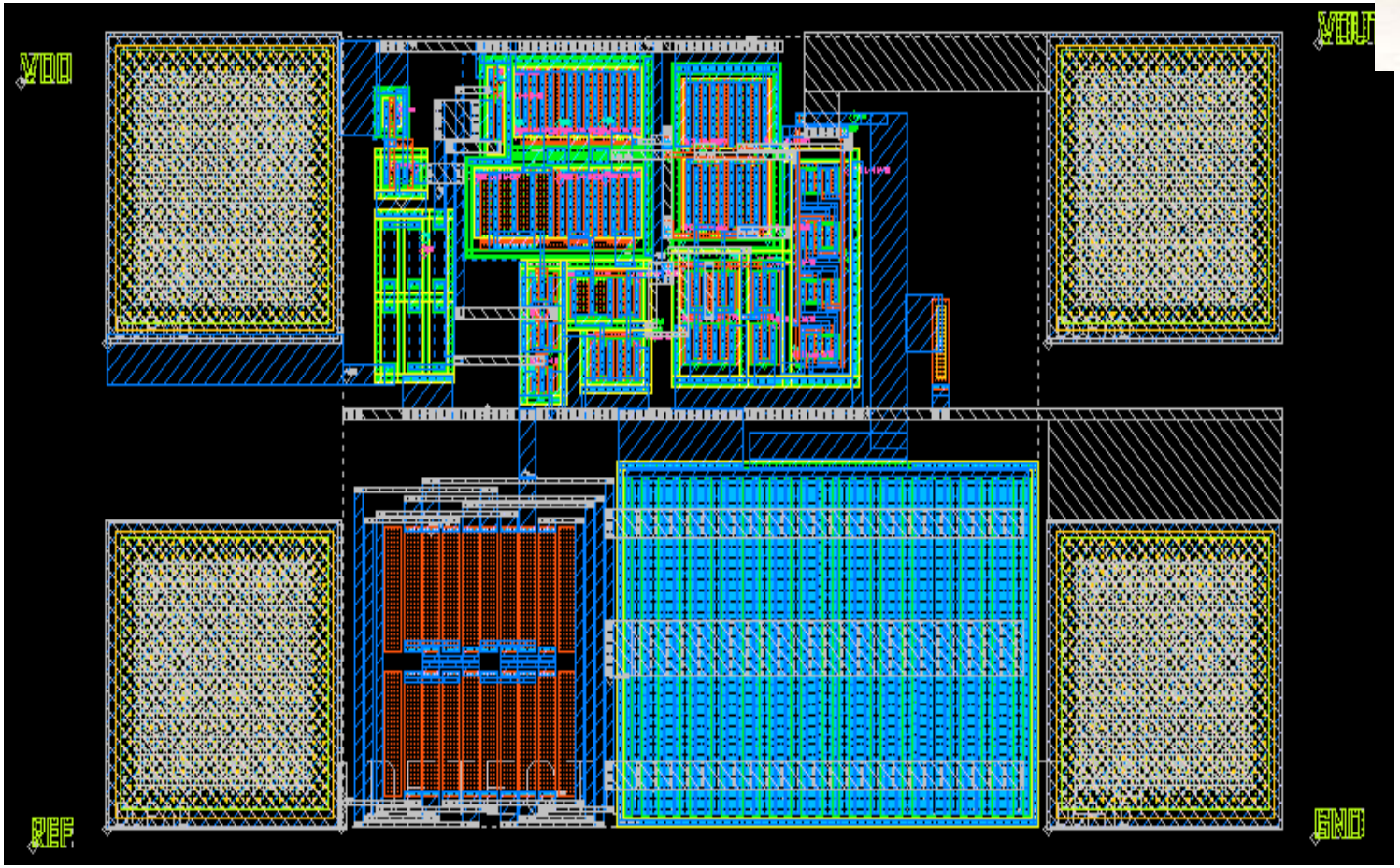


Amplifier layout

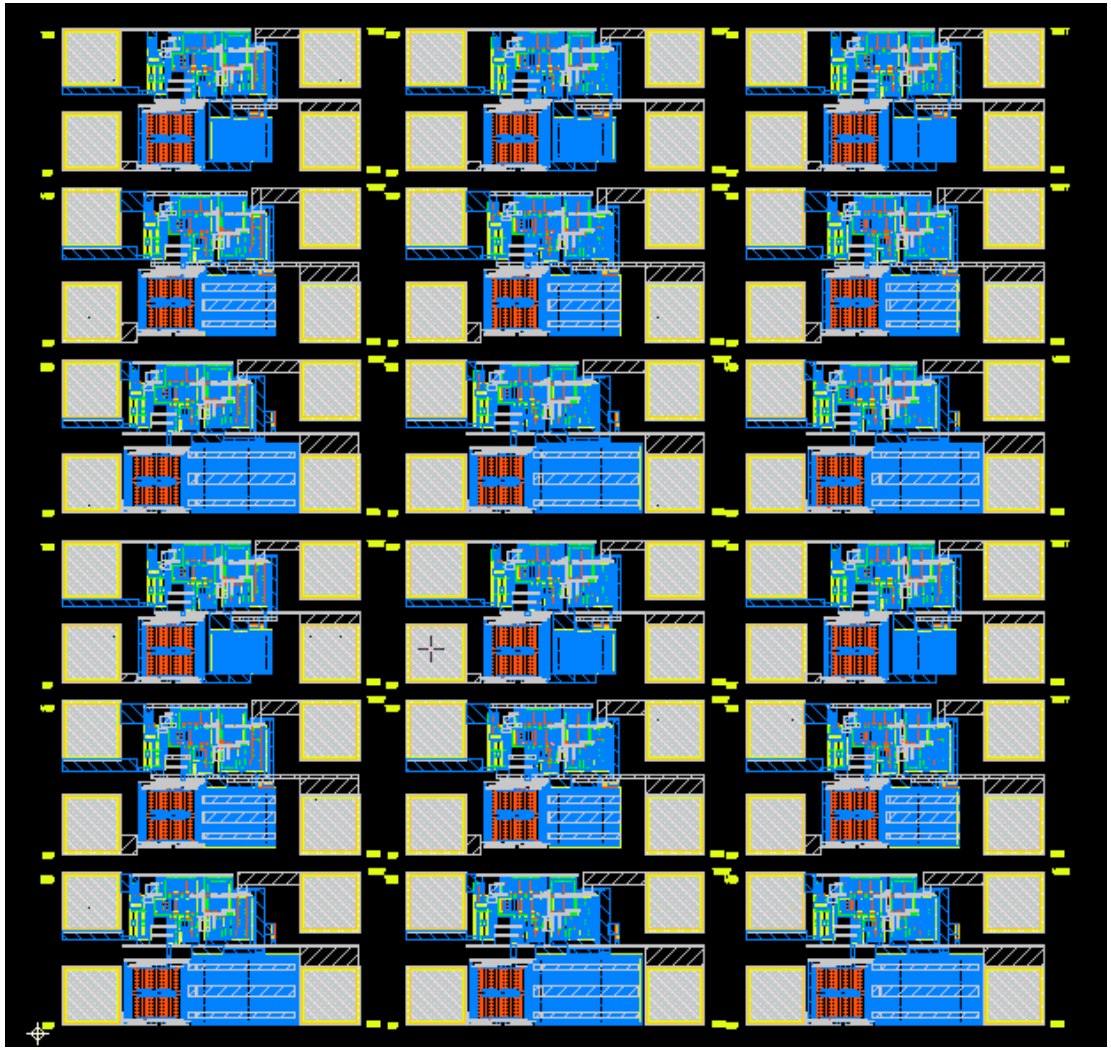


Bias and reference layout

- Complete layout of noise detector circuit



- Complete test chip layout in 0.5 um CMOS



Comments

- The detector test chip will be out of the fab in July.
- Thorough characterization of these detector circuits should result in modules that can be placed into test structures (e.g. clock distribution trees) or any IC for non-invasive measurements.
- This will make way for experiments involving various types of interfering sources during the calendar year 2003.
- The characterizing experiments can be performed using UMCP's test facilities and should result in a clear direction for determining how to make circuits more immune to unwanted RF pulses.

RF Pulses and Basic CMOS logic

- We are also looking at the fundamentals of how RF pulses can disrupt basic CMOS logic (gates, latches, etc.)
- The idea is to inject interfering signals at various points and look at the circuits output (either in the time or frequency domains or using a digital latch to detect a glitch).
- The test chip with the probe point indications is shown on the following pages. This chip is also currently being fabricated.

Basic Logic Test Structures Chip

Pad Descriptions

Pad Number	Pad Type	Input/Output
1.	GND	GND
2.	SIGNAL	VDD INVERTER 2X200
3.	GND	GND
4.	SIGNAL	VDD INVERTER 2X20
5.	GND	GND
6.	SIGNAL	VDD INVERTER 20X20
7.	GND	GND
8.	GND	THRU
9.	GND	THRU
10.	GND	SHORT
11.	INPUT	INVERTER 2X200
12.	OUTPUT	INVERTER 2X200
13.	INPUT	INVERTER 2X20
14.	OUTPUT	INVERTER 2X20
15.	INPUT	INVERTER 20X20
16.	OUTPUT	INVERTER 20X20
17.	SIGNAL	THRU
18.	SIGNAL	THRU
19.	SIGNAL	SHORT
20.	GND	GND
21.	SIGNAL	GND INVERTER 2X200
22.	GND	GND
23.	SIGNAL	GND INVERTER 2X20
24.	GND	GND
25.	SIGNAL	GND INVERTER 20X20
26.	GND	GND
27.	GND	THRU
28.	GND	THRU
29.	GND	SHORT
30.	INPUT	B NAND2X20
31.	GND	GND
32.	SIGNAL	VDD NAND2X20
33.	GND	GND
34.	OUTPUT	NAND2X200
35.	GND	GND
36.	SIGNAL	VDD NAND2X200
37.	GND	GND
38.	INPUT	B NAND2X200
39.	GND	SHORT
40.	INPUT	A NAND2X20
41.	GND	GND
42.	SIGNAL	GND NAND2X20
43.	GND	GND
44.	OUTPUT	NAND2X20
45.	GND	GND
46.	SIGNAL	GND NAND2X200
47.	GND	GND
48.	INPUT	A NAND2X200
49.	SIGNAL	SHORT
50.	INPUT	S SRLATCH2X200
51.	GND	GND
52.	SIGNAL	VDD SRLATCH2X200
53.	GND	GND
54.	OUTPUT	QN SRLATCH2X200
55.	INPUT	S SRLATCH20X20
56.	GND	GND
57.	SIGNAL	VDD SRLATCH20X20

Pad Descriptions, cont'd

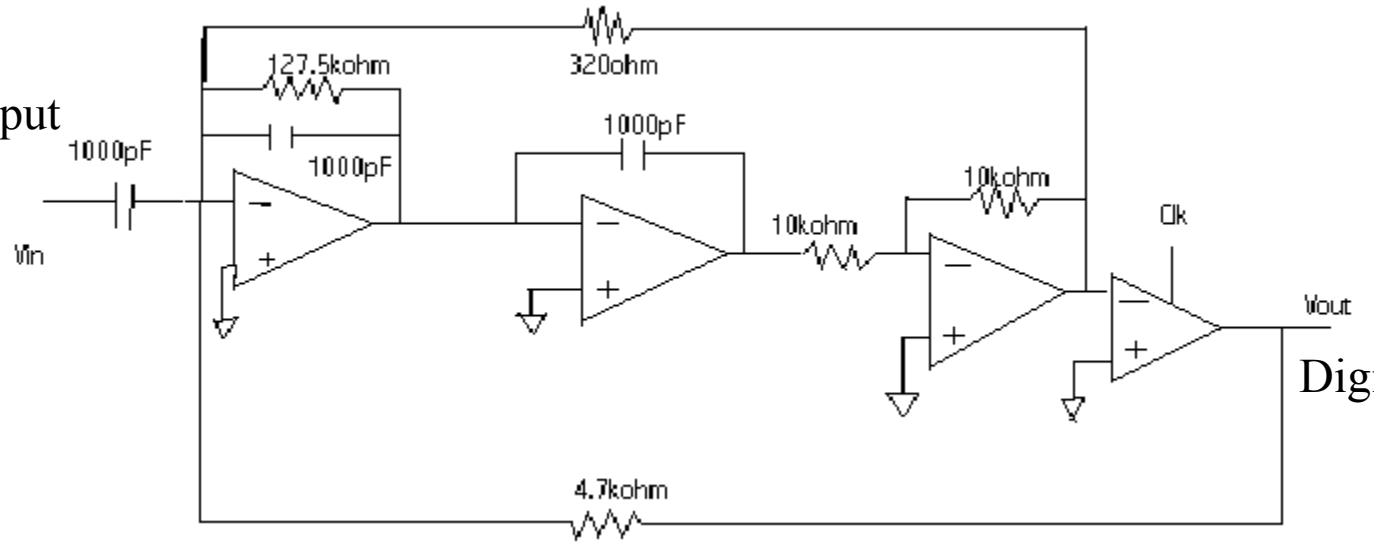
58. GND	GND
59. GND	SHORT
60. INPUT	R SRLATCH2X200
61. GND	GND
62. SIGNAL	GND SRLATCH2X200
63. GND	GND
64. OUTPUT	Q SRLATCH2X200
65. INPUT	R SRLATCH20X20
66. GND	GND
67. SIGNAL	GND SRLATCH20X20
68. GND	GND
69. OUTPUT	QN SRLATCH20X20
70. INPUT	CLK0 DFLIPFLOP2X20
71. GND	GND
72. SIGNAL	VDD DFLIPFLOP2X20
73. GND	GND
74. INPUT	CLK DFLIPFLOP2X20
75. INPUT	S SRLATCH2X20
76. GND	GND
77. SIGNAL	VDD SRLATCH2X20
78. GND	GND
79. OUTPUT	Q SRLATCH20X20
80. INPUT	VIN DFLIPFLOP2X20
81. GND	GND
82. SIGNAL	GND DFLIPFLOP2X20
83. GND	GND
84. OUTPUT	VOUT DFLIPFLOP2X20
85. INPUT	R SRLATCH2X20
86. GND	GND
87. SIGNAL	GND SRLATCH2X20
88. GND	GND
89. OUTPUT	QN SRLATCH2X20
90. OUTPUT	Q SRLATCH2X20

Noise-Shaping A/D Conversion for Measurements

- Built and tested a bandpass noise shaping modulator.
- Can be used for coherent sampling.
- Digital filtering can be used to restrict the frequency range of the noise.
- Experimental results are compared to simulation results.

Schematic of the Modulator

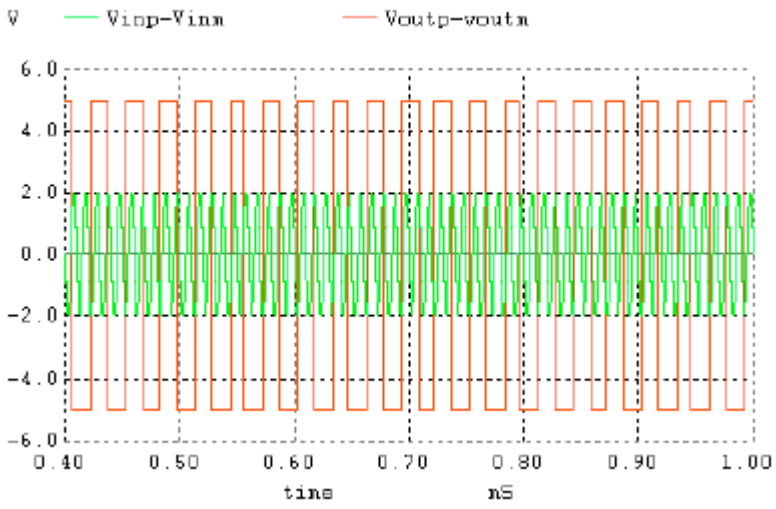
Analog input



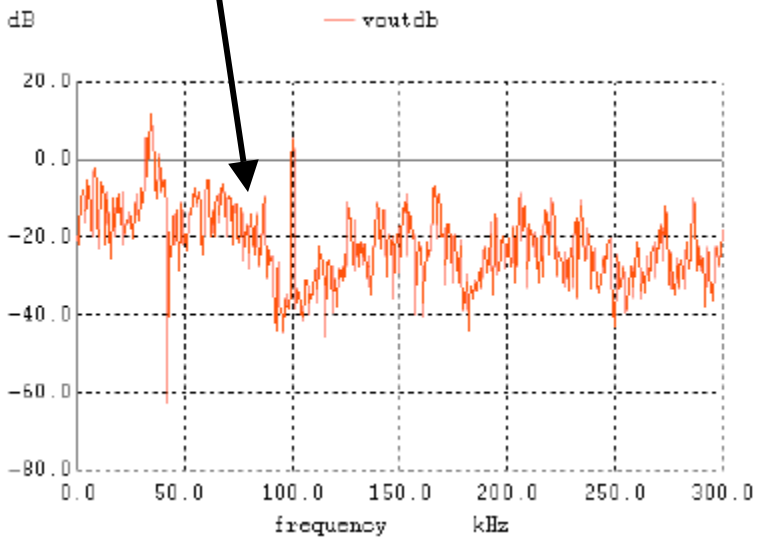
Digital output

Simulation Results

Digital filter removes the modulation noise.

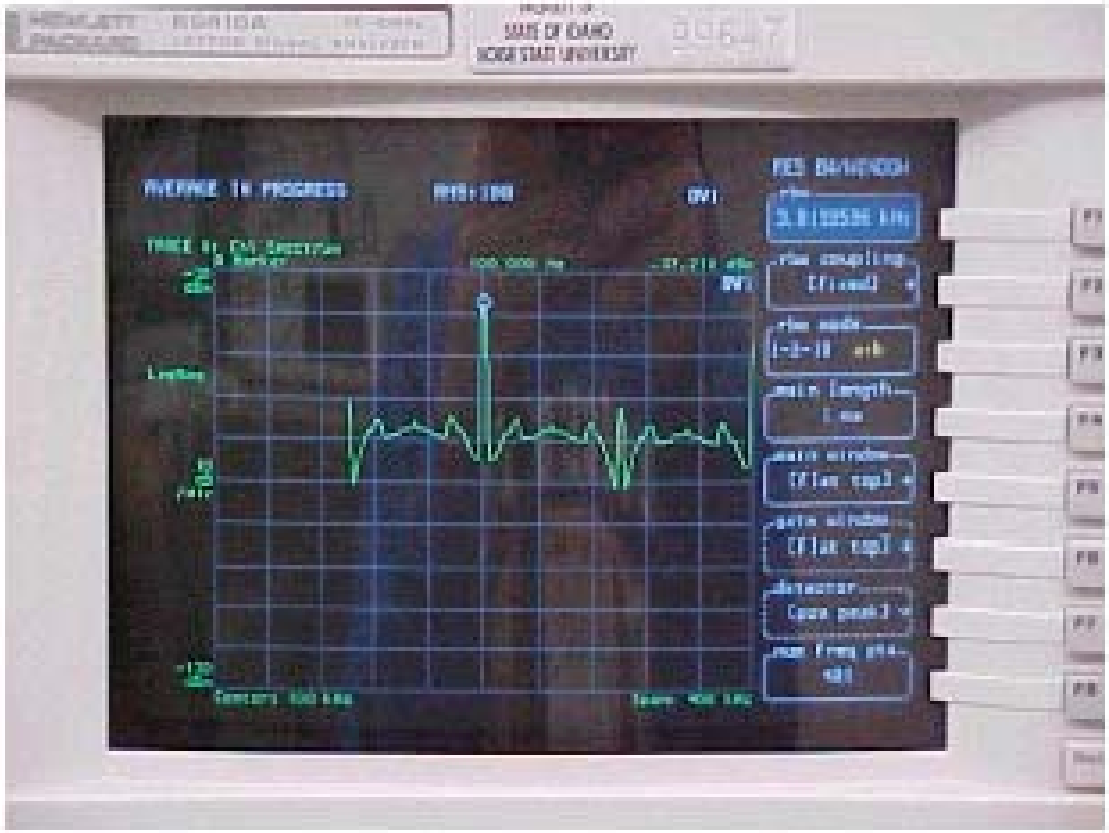


Time domain response



Frequency domain response

Experimental Results



Comments on Noise Shaping

- Robust technique with wide dynamic range possible.
- Will take up more chip area than the circuits using Schottky diodes and amplifiers.
- Requires a digital filter (even more area).
- Won't measure very high frequencies like the Schottky diode circuits.
- Challenging design, may not be portable from one process to another.

Conclusions for Noise Shaping

- Overall not an attractive solution when compared to the Schottky diode-based circuits.
- Will not pursue this area of research further at the present time.
- Shift resources to gate-oxide reliability studies.

Gate Oxide Reliability

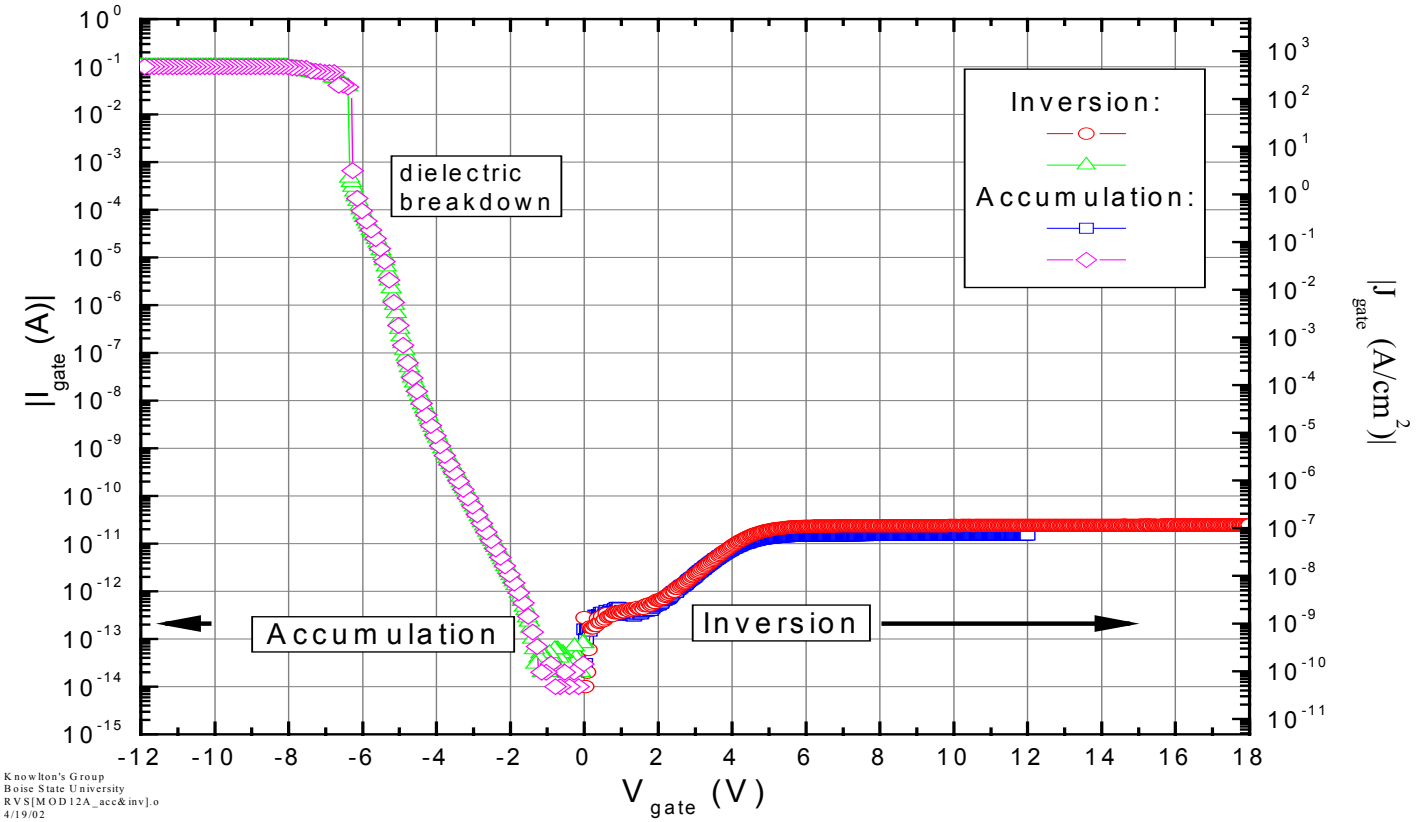
- Ultrathin (t_{ox} < 5nm) Gate Oxide reliability of nMOSCAPs:
  - Accumulation –vs- Inversion: Dielectric breakdown occurs at lower voltages in accumulation
  - Stress Testing Devices in Accumulation:
    - Lifetime
    - Degradation Mechanisms
  - Device Behavior:
    - Pulse Voltage Stressing (PVS) better mimics device behavior than Constant Voltage Stressing (CVS)

- STUDY: Compare PVS and CVS

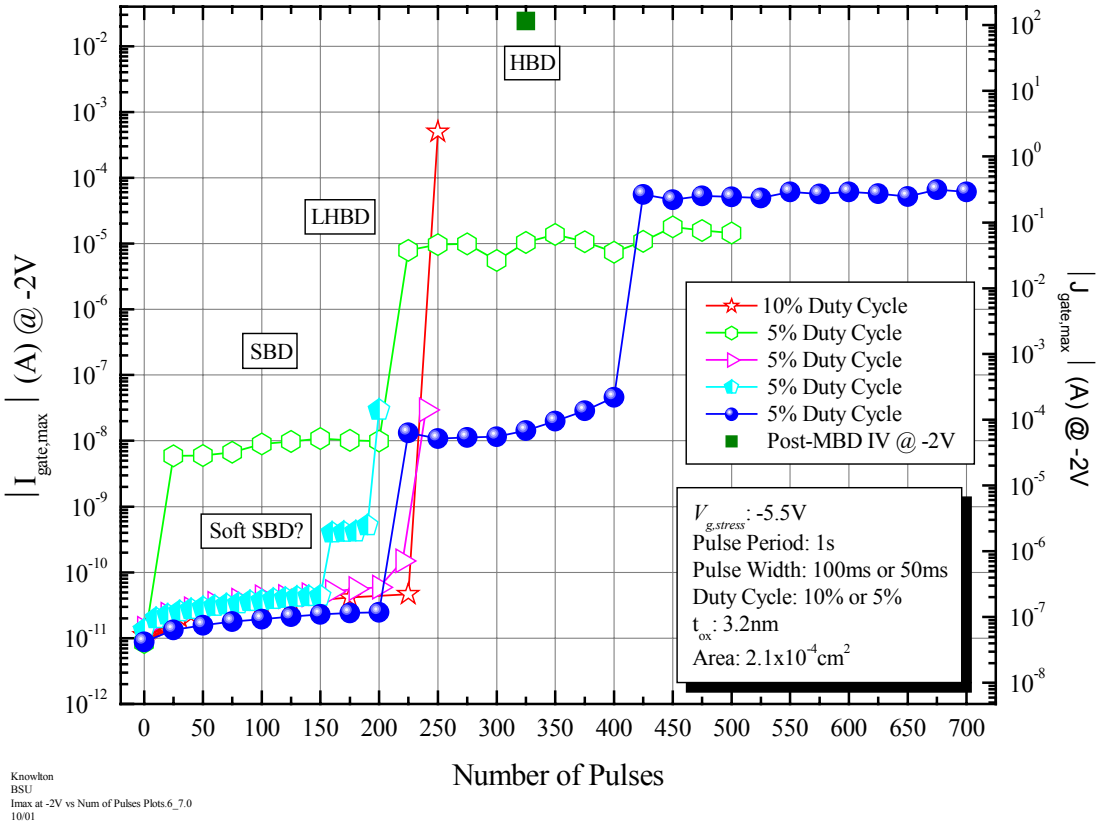
Motivation for the Study

- PVS (Pulse Voltage Stressing): No known studies yet performed for nMOS devices in accumulation
  - PVS –vs- CVS:
    - Lifetime:
      - PVS: Frequency –vs- time
    - Degradation Mechanisms
    - Breakdown Mechanisms
  - Other PVS Studies:
    - Duty cycle: A factor in digital and analog circuits? Yes.
      - e.g., charge pump (output)
    - Mixed signals: Do simultaneous multiple Frequencies and Voltage amplitude signals appear/exist in digital or analog circuits? Perhaps.
      - Simultaneous Multiple Frequencies –vs- time
    - Circuit level reliability: What is the effect of a degraded device on circuit output?

Accumulation-vs-Inversion



PVS, Sense Results and Breakdown Mechanisms



Summary – Directions for Measuring RF Noise On-Chip

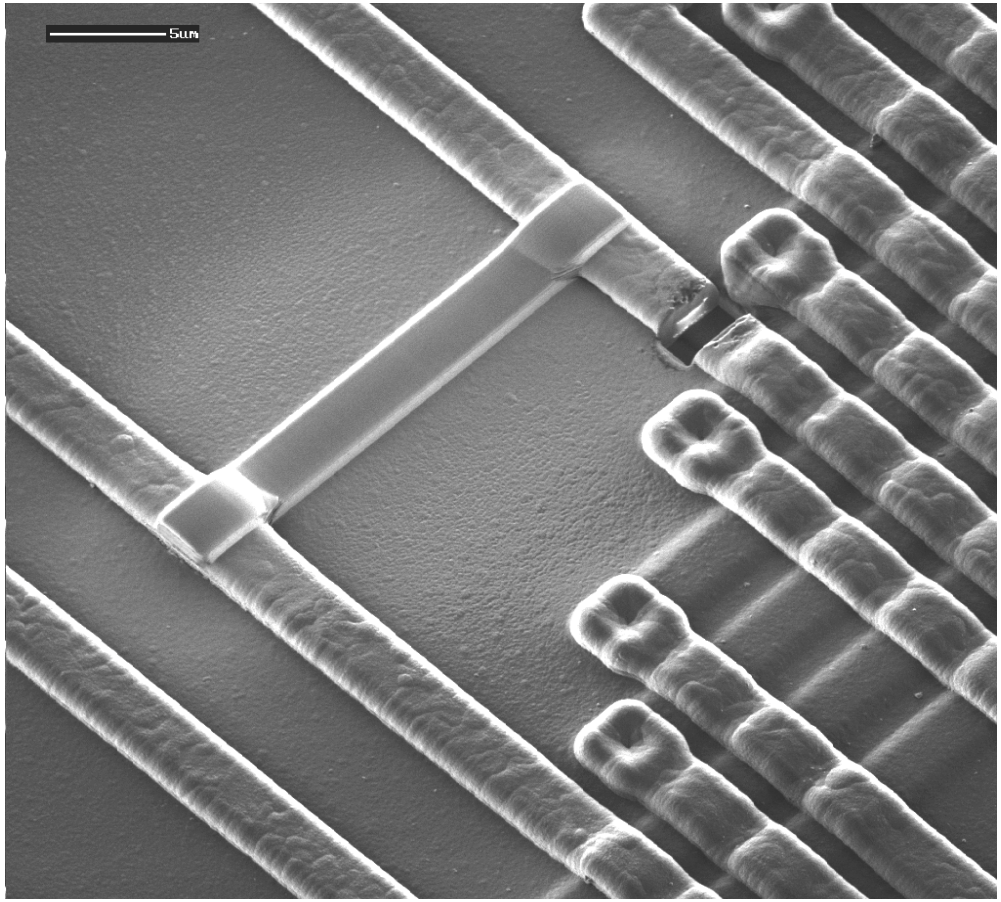
- Over the last year we have designed, fabricated, and characterized Schottky diodes in CMOS (three CMOS test chips with various structures).
- Developing a method of fabricating very high-frequency Schottky diodes using FIB techniques.
- We currently have test chips with various Schottky diodes and amplifier “modules” in production.
- We anticipate full characterization of the modules during Fall 2002.
- This will provide a needed element for the design and implementation of experiments during 2003 and beyond.

What we're after by the end of the year

- Enough data to indicate the weaknesses and vulnerability points in modern CMOS integrated circuits.
- An idea for the direction of the research, do we concentrate on improving the design of the circuits or devices themselves or the protection on the I/O paths?
- Ideas for how we can develop a quantitative benchmark for measuring the improvement in the proposed designs.

End of Slide Show

Example of FIB Circuit Rewiring: Cut and Jumper



FIB-Milled Circuit Cross Section